Digital Offset Calibration of an OPAMP Towards Improving Static Parameters of 90 nm CMOS DAC

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Abstract. *In this article, an on-chip self-calibrated 8-bit R-2R digital-to-analog converter (DAC) based on digitally compensated input offset of the operational amplifier (OPAMP) is presented. To improve the overall DAC performance, a digital offset cancellation method was used to compensate deviations in the input offset voltage of the OPAMP caused by process variations. The whole DAC as well as offset compensation circuitry were designed in a standard 90 nm CMOS process. The achieved results show that after the self-calibration process, the improvement of 48% in the value of DAC offset error is achieved.*

Keywords

Self-calibration, digital to analog converter, input offset voltage trimming.

1. Introduction

Design of analog and mixed-signal integrated circuits (ICs) in nanotechnologies becomes quite difficult due to presence of imperfections in the manufacture process. Unfortunately, ICs designed in advanced nanoscale technologies exhibit a high sensitivity to significant process parameter variations. Therefore, in these technologies, it is rather difficult to design high performance integrated circuits using standard design techniques and approaches [1], [2].

Analog-to-digital converters (ADC) and their digital-to-analog counterparts are probably the most commonly used mixed-signal circuits. Usually, these circuits represent only subcircuits of complex integrated systems, containing both digital and analog signal domains. However, undesired deviations in the value of devices and parameters of circuits used in the converters (ADC and DAC) might seriously influence their static parameters. In some PVT (power, voltage, temperature) corners, even the overall functionality of a DAC might be disrupted. Additionally, standard calibration methods usually require usage of Automatic Test Equipment (ATE) that can be rather expensive. Therefore, development of new alternative calibration/trimming approaches, which help to improve parameters of a designed integrated system (a DAC in our case), is a rather important task and challenging issue.

The important DC parameter of operational amplifiers (which are commonly used in binary-weighted R-2R ladder DACs) is the input offset voltage, and its deviation may be greater than ± 20 mV in a standard CMOS nanometer technology. The input offset voltage of the OPAMP presented in [3] exhibits a value in the range from -50 mV to +50 mV that is not acceptable for high-performance DACs. To solve this problem and to make the design robust and resistant to the process variations, a programmable biasing network was introduced and used in [4]. The other solution is a digital calibration of the OPAMP essential parameters [5]. In [6], an adaptive self calibration test was used in order to improve the linearity of a DAC.

In this paper, a digital offset trimming method has been used to compensate the input offset voltage of an OPAMP in order to improve the overall static parameters of an 8-bit binary-weighted R-2R ladder DAC designed in standard 90 nm CMOS technology. Another method for additional correction of the input offset voltage was presented in [7], where the offset mean value was reduced. Using this method, the mean value of the input voltage offset is kept near zero volts, which is a typical result of analog offset compensation methods.

2. Preliminary Work

Calibration techniques are frequently used to compensate the undesired deviation in the value of circuit's parameters. Currently, many techniques such as special layout techniques, dynamic element matching, error correction as well as analog or digital calibrations have been used to improve the accuracy of the data converters. However, each of them has certain limitations. Dedicated layout techniques are easy to implement because they do not require additional circuitry but they increase the area overhead and interconnection complexity, and might influence dynamic linearity of the converter. Dynamic element matching techniques are usually used in low-bit DACs because the complexity of the encod-

ing circuits becomes significant for higher number of bits [8]. Self-trimming error correction techniques presented in [9], [10] require several additional circuits (ADC, digital correction circuit, memory storage, etc.), and, therefore, are not the suitable solution in terms of the chip area. Digital calibration techniques for improving the accuracy of ADCs and DACs are presented in [11]. In [12], digital calibration techniques for sigma-delta (Σ-Δ) data converters were introduced.

Calibration techniques for the input offset voltage of an OPAMP, which is a basic building block of the DAC, are presented in [13]. Chopper stabilization technique used in [14], [15] is based on the transposition of the signal to a higher frequency, where the effect of the input voltage offset is negligible. After the transposition to higher frequencies, the signal is amplified and demodulated back to the baseband. Basic principle of so-called *auto-zero technique* is to sample the undesired effect and then to subtract it during the second phase, when the input signal is processed by an imperfect amplifier [15]. A similar method is also *correlated double sampling* (CDS) used in [16]. However, both the autozero and CDS techniques are nor suitable for applications where a continuous-time output is required because during the sampling process the system must be disconnected from the signal path. This disadvantage can be eliminated by *ping-pong* technique [17], [18], which is used in [18] to calibrate a rail-to-rail amplifier. The amplifier is duplicated and one of them is calibrated while the other is amplifying the input signal. After calibration the role of both amplifiers is exchanged. An improved ping-pong technique that reduces the undesired glitches during the transition from one amplifier to another is presented in [19]. However, digital techniques represent the best alternative for calibration of different analog and mixed-signal systems, because of their versatility. Therefore, these techniques are usually used for calibration of the input offset voltage of the OPAMP.

Digital offset trimming techniques usually use the binary-weighted current network, described in [5], [20], [21]. The output current of such a converting network is used to compensate the undesired influence (e.g. offset voltage) of process parameter variations. Methods based on digital trimming principles have compensation limitations determined by the converting network resolution [7]. Therefore, also the value of the OPAMP input offset voltage achieved using the compensation is a function of the converting network resolution and the offset level to be compensated. The resolution can be expressed as follows:

$$\text{Resolution} = \frac{\text{Full Scale}}{\text{1.LSB}} \leq \frac{V_{off\_uncomp}}{V_{off\_comp}} \qquad (1)$$

where V_{off_uncomp} and V_{off_comp} is the input offset voltage of the OPAMP before and affter the calibration process, respectivelly.

Depending on the used converting network, the different network resolution can be achieved, since it is given by the number of bits and weight type of the converting network. Using the redundance R, the resolution can be expressed by (2).

$$\text{Resolution} = \frac{b_1 + \sum_{i=1}^{n} b_i}{b_1} = \frac{R^n}{R-1}. \qquad (2)$$

Redundancy parameter R of the binary weighted M-2M converting network is $R = 2$. In the case of a 6-bit converter, it corresponds to resolution of 64 steps. This is, at the same time, the maximum resolution for a 6-bit converter. Linearity and sensitivity, influenced mainly by components mismatch, are the most critical characteristics of the binary weighted converting network. Therefore, redundant converting networks described in detail in [5], [20], [21] are often used. Redundancies $R = 1.77$ and $R = 1.86$ are achieved for the converting networks of M-3M and M-2.5M types, respectively. Resolution of M-2.5M converting network type is 48 steps.

For the digital trimming, one thing is always common independently of the used converting network type. Maximum to minimum offset voltage ratio is always given by the network resolution, and the offset mean value is near half of that ratio. The mean value of the offset voltage is obviously different from zero volts. Therefore, a correction circuit was developed and used to reduce this feature [7]. After its intervention, the mean offset value can be kept close to zero volts. Similar result can be achieved using analog compensation methods [7].

3. Self-Calibrated DAC

Basic block diagram of the proposed self-calibrated DAC, designed in 90 nm CMOS technology, is shown in Fig. 1. The whole system consists of the converter itself (yellow parts) and on-chip additional hardware necessary for the self-calibration process (blue blocks), including control logic and the trimming block. Compensation of the OPAMP input offset voltage as well as additional circuitry needed for this purpose are described in more details in the next Section.

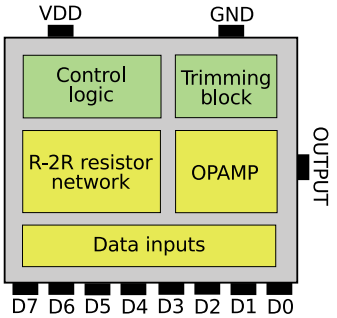

Fig. 1. Block diagram of the self-calibrated R-2R DAC.

3.1 OPAMP Offset Compensation

The circuit diagram of the OPAMP (representing the basic building block of the DAC) is shown in Fig. 2. Input stage together with the folded cascode represent the first

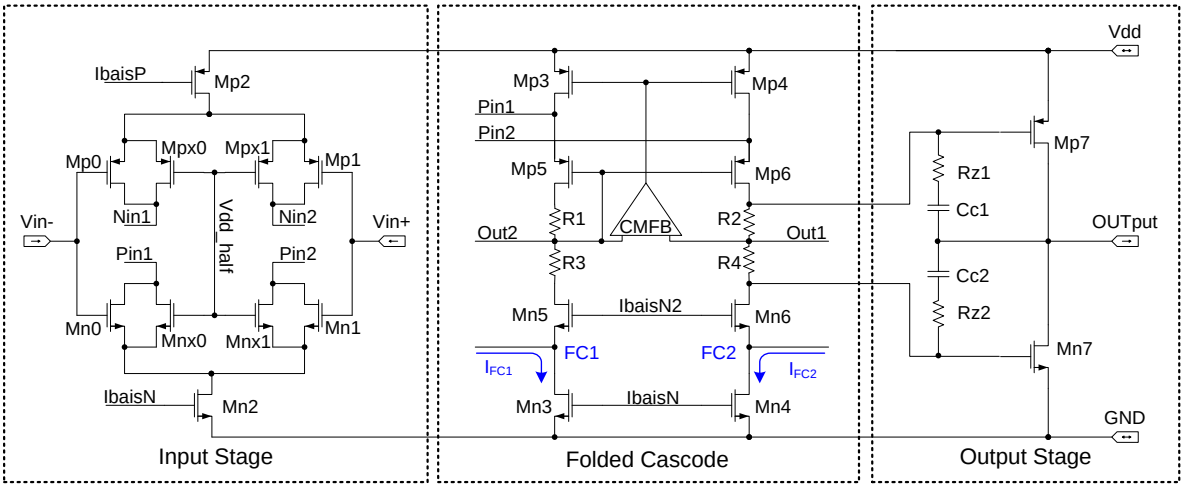

Fig. 2. Schematic diagram of the OPAMP used in DAC.

stage, while the push-pull inverter forms the output stage of the OPAMP. Rail-to-rail input and output stages allow the OPAMP to operate within the input and output voltages near to the voltage supply rails. Folded cascode stage was used to achieve high gain. To stabilize the operational point of the folded cascode and the push-pull inverter as well as to achieve a high gain of the output stage, the Common-Mode Feedback (CMFB) network was used. Detailed description of individual parts of the OPAMP can be found in [22].

Since device mismatch may influence the operational point of all transistors forming the OPAMP, it has to be taken into account that the input offset voltage represents a critical parameter of the OPAMP and thus, also the whole DAC. To improve this parameter, the digital compensation of the OPAMP's input offset was employed.

The offset compensation process is based on generation of compensation currents that are pumped into the respective branch of the folded cascode structure of the OPAMP. Such compensation currents can be generated by a converting network. Two different topologies for digital offset trimming based on the converting network, one using successive approximation register (SAR) and the other employing a simple counter have been used in [7]. Results presented in [7] indicate that M-2M converting network (depicted in Fig. 3) is more appropriate to digital trimming. However, the main drawback of the M-2M structure is the imbalance in the current division [5]. Since the compensation currents (I_{FC1} and I_{FC2}) in the M-2M compensating network (Fig. 3) will never be identical, an extra correction circuit (to be described later in Section 3.3) was employed to make them equal.

3.2 DAC Circuit Diagram

The circuit diagram of the whole 8-bit self-calibrated R-2R DAC with additional circuitry necessary for the OPAMP input offset compensation (within the DAC design) is shown in Fig. 4. Transmission gates or so-called T-gates

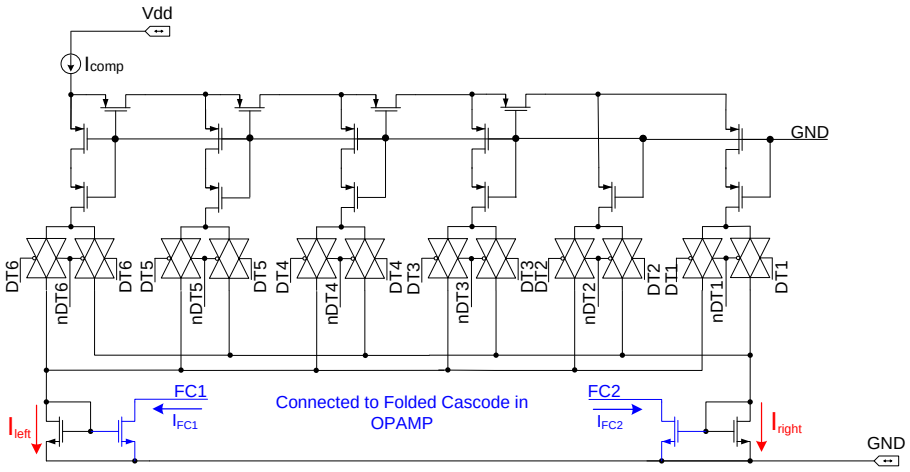

Fig. 3. M-2M converting network.

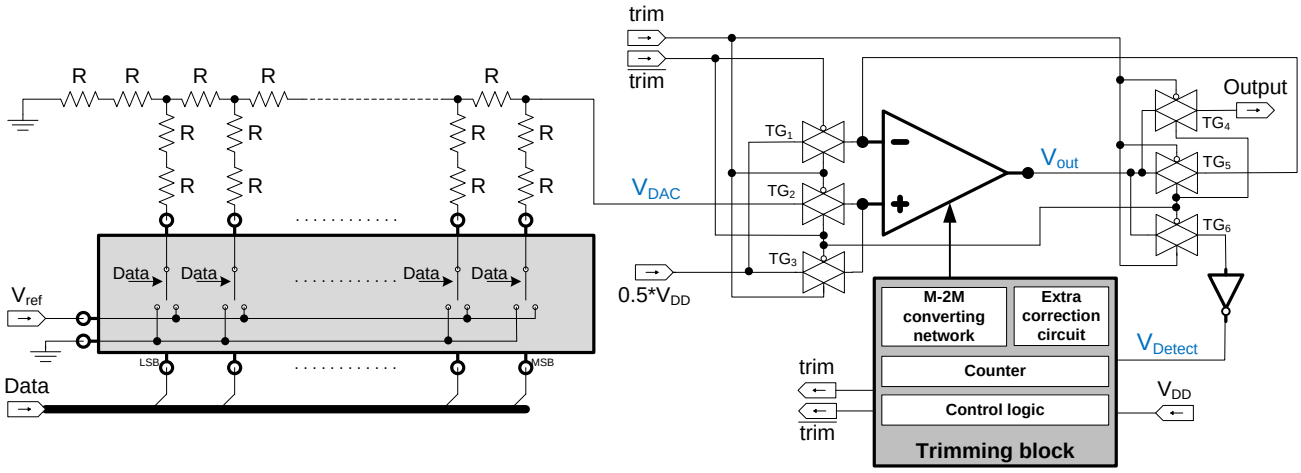

Fig. 4. Circuit diagram of the self-calibrated 8-bit R-2R DAC.

(TG) are used to switch the OPAMP from functional mode to trimming mode and to disconnect the OPAMP from the R-2R resistor network (a part of the DAC). Another extra hardware is the trimming block, which includes also control logic that is realized using a serial counter and converting network that generates the compensating current for the respective side of the folded cascode stage. Control logic together with the counter generates control signals for T-gates used in both the M-2M converting network and extra correction circuits. A voltage comparator is used to compare the OPAMP output voltage to the reference voltage and to indicate the completion of the trimming process [7]. In this case, a simple invertor plays the role of the voltage comparator.

When the supply voltage (V_{DD}) is turned on, control logic generates control signals ($trim$ and $\overline{trim}$) for trimming circuitry and starts the process of the digital compensation of the OPAMP input offset voltage. During the calibration process, the OPAMP is disconnected from the rest of the system. When the OPAMP output voltage (V_{detect}) is equal to $V_{DD}/2$, control logic terminates the calibration process. As soon as the calibration process is completed, control logic turns off the trimming block and the DAC is ready for use.

3.3 Extra Correction Circuit

The whole philosophy of the proposed extra correction circuit is based on the manual equalization of the compensation currents that are then injected into the respective side of the OPAMP's folded cascode. In the situation that the OPAMP offset voltage is zero, offset compensation current equivalent to 1 LSB would be generated. Since according to (3), the standard offset compensation currents in the two branches of the compensating network will never be identical, as already mentioned above. Therefore, a correction circuit was proposed and applied (4), to shift the mean offset value close to zero (Fig. 5).

No correction:

$$I_{left} = 32.\text{LSB}, \quad I_{right} = 31.\text{LSB},$$

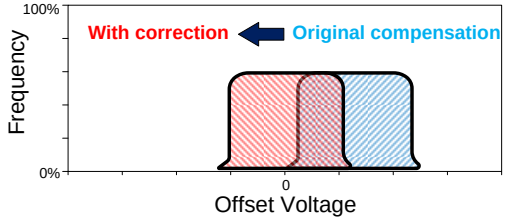

Fig. 5. Principle of the offset mean value shift by a correction circuit.

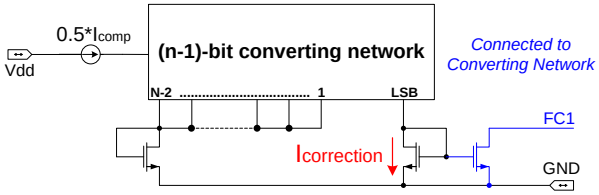

Fig. 6. Correction circuit generating the correction current.

$$I_{left} \neq I_{right}. \tag{3}$$

With correction:

$$I_{left} = 32.\text{LSB}, \quad I_{right} = 31.\text{LSB} + I_{correction},$$
$$I_{left} = I_{right}. \tag{4}$$

With the extra correction circuit, standard trimming procedure is used. Differential current, generated by the converting network, is stepwise injected in the left and right sides of the folded cascode, till the output voltage is dissimilar to the reference voltage. Standard trimming procedure is finished when the output voltage value is equal to the reference voltage. When the trimming process ends, 1 LSB correction current $I_{correction}$ will be kept injecting in one side the folded cascode. To provide this, it was necessary to employ one additional converting network (Fig. 6). Taking into account the energy saving aspect, it was sufficient to use one order lower converter with half the maximum compensation current.

	Not trimmed circuit	**Counter**		**SAR**	
		No correction	correction circuit	No correction	correction circuit
sd [μV]	5517	343.15	343.55	333.97	331.07
mu [μV]	2	688.95	78.82	480.92	-113.16
Min [mV]	-17.357	0.055	-0.695	-0.012	-0.668
Max [mv]	18.216	1.547	0.945	1.396	0.754
Improvement	—	**95.81**%	**95.84**%	**96.04**%	**96**%

Tab. 1. Comparison of the OPAMP digital offset trimming based on the M-2M converting network using SAR and a simple counter.

The binary weighted M-2M converting network is very suitable for the presented correction approach since in this type of networks, the compensation current values for two succeeding states are approximately identical. On the other hand, redundant converting networks exhibit a difference between two succeeding states, and therefore, such topologies are not optimal for the offset compensation according to Fig. 5.

Generally, control signals that switch T-gates used in the M-2M converting network can be generated by a binary counter or by the successive approximation register (SAR). Comparison of results achieved for the OPAMP digital offset trimming based on the M-2M converting network using SAR and a simple counter is summarized in Tab. 1, and it was presented in [7]. It can be observed that the application of the correction circuit has no negative effect on the standard deviation of the offset voltage. On the other hand, the offset mean value is near the value of untrimmed circuit. The combination of M-2M type converting network and the control logic realized with SAR can achieve the best results, however, the version with control logic realized by a counter provides the lowest mean value of the offset.

4. Achieved Results

The proposed self-calibrated DAC was simulated and evaluated in CADENCE design environment for the power supply voltage of 2.5 V and temperature of 25°C, while performing 200 runs of Monte Carlo (MC) analysis. The value of main static parameters such as integral nonlinearity (INL), differential nonlinearity (DNL), offset error (OE), gain error (GE) and full scale error (FSE) of the designed DAC have been analyzed before and after applying trimming process. The obtained results are presented in this section.

Fig. 7 shows the deviation of INL parameter as a function of the DAC input data code. One can observe that in the worst case, deviation of INL (caused by process fluctuation) before the trimming process is in the range from -2.292 LSB to 2.286 LSB. After running the trimming, the deviation of INL is kept within the range from -1.298 LSB to 1.341 LSB, which represents about 42% improvement in comparison to the original circuit parameter. In the best case, six times better value of the INL parameter can be achieved that is an excellent result with respect to significant fluctuation of the process parameters expected in 90 nm technology.

Dependence of DNL parameter on the DAC input data code is shown in Fig. 8. The best improvement was achieved for low values of the input data code. The obtained results also show that with the OPAMP offset trimming process, the improvement of only 18% is achieved for DNL. This is due to the fact that the DNL parameter does not directly depend on the input offset voltage of the OPAMP.

Fig. 9 shows the OE parameter of the DAC before and after calibration process obtained by MC analysis. With no calibration process being applied, the OE deviation was in the range from -1.67 LSB to 2.29 LSB. After the calibration, the OE value falls into the range from -1.02 LSB to 1.04 LSB, which represents improvement of 48% of the

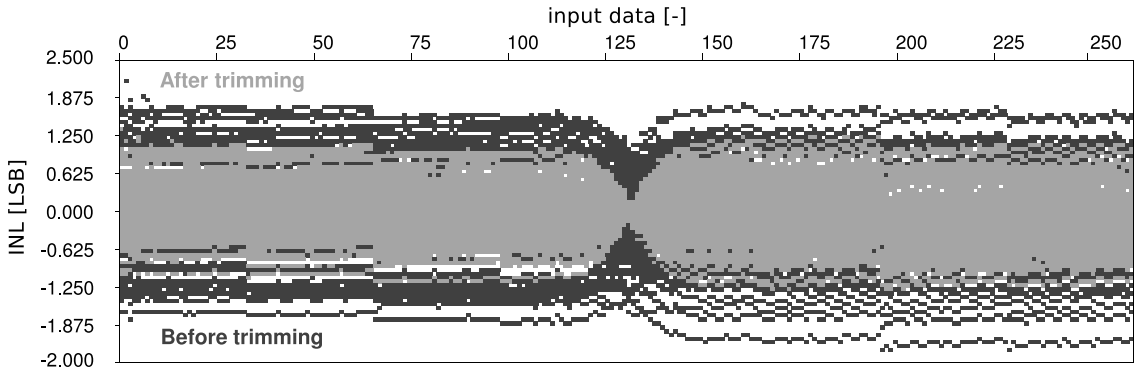

Fig. 7. Deviation of INL versus the DAC input data code.

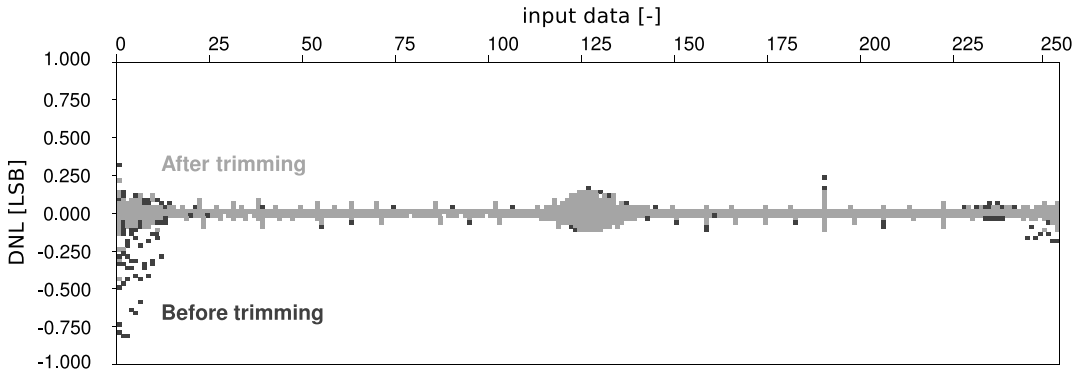

Fig. 8. Deviation of DNL versus the DAC input data code.

DAC offset error. We would like to note that for the offset error, the best improvement can be reached since this parameter of the proposed DAC directly depends on the OPAMP's input offset voltage.

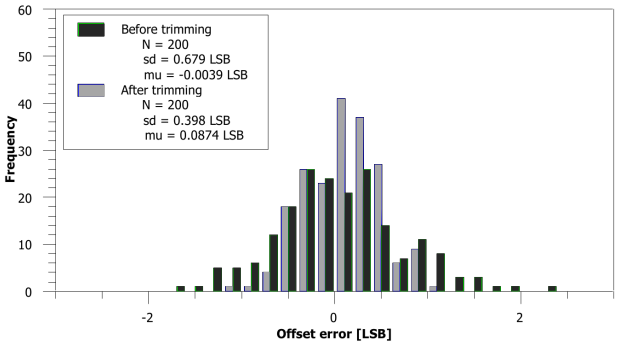

Fig. 9. Deviation of the offset error.

Similarly, the improvement of 38% and 31% can be achieved for GE and FSE, respectively. Deviation of gain error before and after calibration process obtained by MC analysis is depicted in Fig. 10. Before calibration, the deviation of GE was in the range from -5.48 LSB to 1.5 LSB, while the calibration process brings improvement of 38% of the DAC gain error. Similarly, the improvement of 31% can be achieved for FSE after calibration process. Deviation of FSE obtained by MC analysis is shown in Fig. 11.

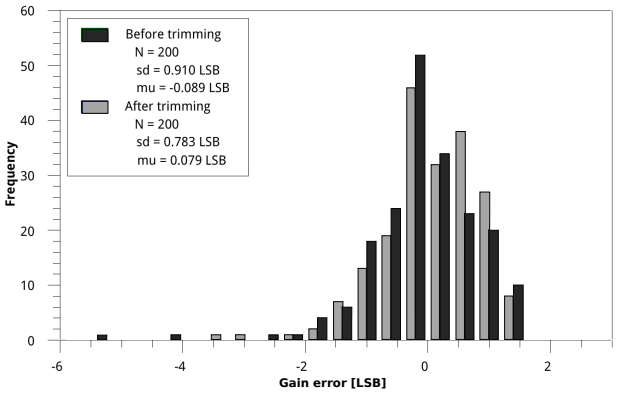

Fig. 10. Deviation of the gain error.

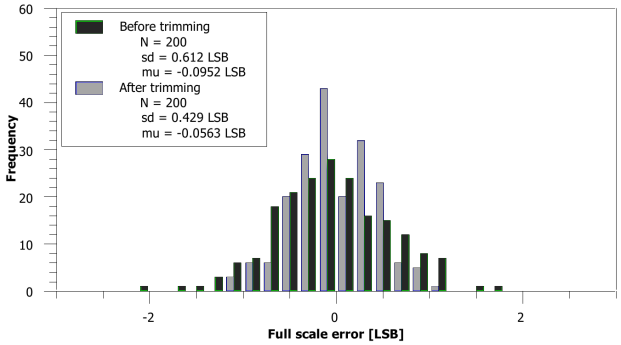

Fig. 11. Deviation of the full scale error.

The main static parameters of the designed DAC are summarized in Tab. 2, which also presents the worst case improvement of these parameters achieved by performing on-chip self-calibration of the converter. The best improvement of 48% was obtained for the offset error. Good results were also obtained for INL (42.4%), gain error (38.1%) and full scale error (31.1%) parameters. The less improved parameter is the differential nonlinearity (DNL), where the improvement of 18.6% was achieved.

Parameter	**Before trimming**	**After trimming**	**Improvement** (worst case)
INL [LSB]	-2.29 ÷ 2.29	-1.30 ÷ 1.34	**42.4%**
DNL [LSB]	-0.81 ÷ 0.67	-0.56 ÷ 0.64	**18.6%**
OE [LSB]	-1.67 ÷ 2.29	-1.02 ÷ 1.04	**48.0%**
GE [LSB]	-5.48 ÷ 1.50	-3.26 ÷ 1.55	**38.1%**
FSE [LSB]	-2.08 ÷ 1.60	-1.18 ÷ 1.10	**31.1%**

Tab. 2. Main static parameters of the DAC.

5. Discussion and Conclusion

The comparison of the achieved results to other works in terms of the INL parameter improvement is presented in Tab. 3. Nevertheless, this comparison might not be quite relevant because approaches presented in the other publications are based on calibration of the whole DAC, while this work

utilizes the OPAMP offset voltage trimming only. As one can observe, only by 7.6% lower improvement of the INL parameter was achieved with respect to [23]. On the other hand, in [24], up to 30% higher improvement was reported. However, it is important to note that a DAC published in [24] has a higher resolution (12-bit) and has been calibrated completely as a whole system.

	Before trimming	**After trimming**	**Improvement**
This work	-2.29 ÷ 2.29	-1.30 ÷ 1.34	**42.4%**
[23] *8-bit*	-0.4 ÷ 0.4	-0.2 ÷ 0.2	**50.0%**
[24] *12-bit*	-1.4 ÷ 1.5	-0.4 ÷ 0.4	**74.4%**

Tab. 3. Comparison of INL parameter to other works.

Tab. 4 presents the comparison of the proposed DAC to other published works in terms of area overhead. Although DACs presented in [9], [24], [25] have a higher resolution, additional calibration hardware brings a larger area overhead, while in our case, the area overhead is only 8%. Moreover, the proposed DAC was designed in 90 nm CMOS technology were the chip area is rather expensive, and therefore, the area overhead of only 8% represents a significant result.

Parameter	**This work**	**[9]**	**[25]**	**[24]**
Technology	90 nm	0.13 μm	0.18 μm	0.25 μm
Area [mm^2]	0.01	0.1*	1.00	1.14
Overhead	8%	-	50%	25%

* only active area reported

Tab. 4. Comparison in terms of area overhead .

From the results presented in Tab. 3 and Tab. 4, it can be observed that only the DAC published in [24] is comparable to the DAC presented in this work. However, the DAC presented in [24] has a higher resolution and was designed in 0.25 μm technology, where the process parameter fluctuation is significantly smaller than in 90 nm technology. Therefore, the proposed approach based on calibration of the OPAMP input offset voltage represent a proper solution for calibration of DAC in nanoscale technologies.

The main advantages of the proposed self-calibrated DAC design include mainly easy implementation and possible fully on-chip realization of the self-calibration. Since the calibration process runs automatically with each turn-on of the DAC, deviation in the value of the OPAMPs input offset voltage caused by aging effects might be compensated as well. The proposed self-calibration offers the improvement of all static parameters of the DAC up to at least 30%, except for the DNL parameter. Drawback of the proposed approach is that dynamic parameters of the DAC are not improved since they do not directly depend on the input offset voltage of the OPAMP. Therefore, it is important to underline that the achieved results can be improved further if calibration of the R-2R ladder resistor network is carried out as well.

To summarize the performed work and achieved results, it can be stated that the on-chip digital offset compensation of the OPAMP has been used to improve the static parameters of the 8-bit binary weighted R-2R ladder DAC designed in a standard 90 nm CMOS technology. For this purpose, additional hardware including control logic has been inserted into the DAC, with no extra pins needed. Add-on hardware requires the area of 330 μm^2, which represents the overhead of 8% (with respect to the whole DAC). Nevertheless, if the DAC is used in a complex mixed-signal system this area overhead will become negligible.

The future work will be focused on the minimization of the area requirements for additional hardware as well as on the investigation of the undesired influence of the additional hardware on the DAC parameters in its functional mode.

Acknowledgements

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References

[1] LEWYN, L., YTTERDAL, T., WULFF, C., MARTIN, K. Analog circuit design in nanoscale CMOS technologies. *Proceedings of the IEEE*, 2009, vol. 97, no. 10, p. 1687 - 1714.

[2] KARMANI, M., KHEDHIRI, C., HAMDI, B. Design and test challenges in nano-scale analog and mixed CMOS technology. *International Journal of VLSI design and Communication Systems (VLSICS)*, 2011, vol. 2, no. 2, p. 33 - 43.

[3] MACHOWSKI, W., JASIELSKI, J. Offset compensation for voltage- and current amplifiers with CMOS inverters. In *Proceedings of the 19th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*. 2012, p. 382 - 385.

[4] DELA CRUZ, S., DELOS REYES, M., GAFFUD, T., ABAYA, T., GUSAD, M., ROSALES, M. Design and implementation of operational amplifiers with programmable characteristics in a 90 nm CMOS process. In *European Conference on Circuit Theory and Design (ECCTD)*. 2009, p. 209 - 212.

[5] PASTRE, M., KAYAL, M. Methodology for the digital calibration of analog circuits and systems using sub-binary radix DACs. In *16th International Conference on Mixed Design of Integrated Circuits Systems (MIXDES)*. 2009, p. 456 - 461.

[6] JIANG, W., AGRAWAL, V. D. Built-in adaptive test and calibration of DAC. In *Proceedings of 18th IEEE North Atlantic Test Workshop*. 2009, p. 124 - 127.

[7] NAGY, G., ARBET, D., STOPJAKOVA, V. Digital methods of offset compensation in 90 nm CMOS operational amplifiers. In *IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*. 2013, p. 124 - 127.

[8] SAEEDI, S., MEHRMANESH, S., ATARODI, M. A low voltage 14-bit self-calibrated CMOS DAC with enhanced dynamic linearity. *Analog Integrated Circuits and Signal Processing*, 2005, vol. 43, no. 2, p. 137 - 145.

[9] CONG, Y., GEIGER, R. A 1.5-V 14-bit 100-MS/s self-calibrated DAC. *IEEE Journal of Solid-State Circuits*, 2003, vol. 38, no. 12, p. 2051 - 2060.

[10] BUGEJA, A., SONG, B.-S. A self-trimming 14-b 100-MS/s CMOS DAC. *IEEE Journal of Solid-State Circuits,* 2000, vol. 35, no. 12, p. 1841 - 1852.

[11] MOON, U.-K., TEMES, G., STEENSGAARD, J. Digital techniques for improving the accuracy of data converters. *IEEE Communications Magazine*, 1999, vol. 37, no. 10, p. 136 - 143.

[12] SILVA, J., WANG, X., KISS, P., MOON, U., TEMES, G. Digital techniques for improved ΔΣ data conversion. In *Proceedings of the IEEE Custom Integrated Circuits Conference.* 2002, p. 183 - 190.

[13] PASTRE, M., KAYAL, M. *Methodology for the Digital Calibration of Analog Circuits and Systems: With Case Studies*, 1st ed. Springer, 2009.

[14] ENZ, C., VITTOZ, E., KRUMMENACHER, F. A CMOS chopper amplifier. *IEEE Journal of Solid-State Circuits*, 1987, vol. 22, no. 3, p. 335 - 342.

[15] ENZ, C., TEMES, G. Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, 1996, vol. 84, no. 11, p. 1584 - 1614.

[16] WHITE, M., LAMPE, D., BLAHA, F., MACK, I. Characterization of surface channel CCD image arrays at low light levels. *Solid-State Circuits, IEEE Journal*, vol. 9, no. 1, Feb 1974, p. 1–12.

[17] YU, C.-G., AND GEIGER, R. An automatic offset compensation scheme with ping-pong control for CMOS operational amplifiers. *IEEE Journal of Solid-State Circuits*, 1994, vol. 29, no. 5, p. 601 - 610.

[18] OPRIS, I., KOVACS, G. T. A. A rail-to-rail ping-pong op-amp. *IEEE Journal of Solid-State Circuits*, 1996, vol. 31, no. 9, p. 1320 - 1324.

[19] KAYAL, M., SAEZ, R., DECLERCQ, M. An automatic offset compensation technique applicable to existing operational amplifier core cell. In *Proceedings of the IEEE Custom Integrated Circuits Conference*. 1998, p. 419 - 422.

[20] SCANDURRA, G., CIOFI, C., CAMPOBELLO, G., CANNATA, G. On the Calibration of DA Converters Based on R/βR Ladder Networks. *IEEE Transactions on Instrumentation and Measurement*, 2009, vol. 58, no. 11, p. 3901 - 3906.

[21] CIOFI, C., SCANDURRA, G., CAMPOBELLO, G., CANNATA, G. On the calibration of AD and DA converters based on R/βR ladder networks. In *13th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2006, p. 958 - 961.

[22] ARBET, D., NAGY, G., GYEPES, G., STOPJAKOVA, V. Design of rail-to-rail operational amplifier with offset cancelation in 90 nm technology. In *International Conference on Applied Electronics (AE)*. 2012, p. 17 - 20.

[23] VARGHA, B., ZOLTAN, I. Calibration algorithm for current-output R-2R ladders. *IEEE Transactions on Instrumentation and Measurement*, 2001, vol. 50, no. 5, p. 1216 - 1220.

[24] RADULOV, G., QUINN, P., HEGT, H., VAN ROERMUND, A. An on-chip self-calibration method for current mismatch in D/A converters. In *Proceedings of the 31st European Solid-State Circuits Conference (ESSCIRC)*. 2005, p. 169 - 172.

[25] TIILIKAINEN, M. A 14-bit 1.8-V 20-mW 1-mm2 CMOS DAC. *IEEE Journal of Solid-State Circuits*, 2001, vol. 36, no. 7, p. 1144 - 1147.

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