Simple Floating Voltage-Controlled Memductor Emulator for Analog Applications

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Abstract. The topic of memristive circuits is a novel topic in circuit theory that has become of great importance due to its unique behavior which is useful in different applications. But since there is a lack of memristor samples, a memristor emulator is used instead of a solid state memristor. In this paper, a new simple floating voltage-controlled memductor emulator is introduced which is implemented using commercial off the shelf (COTS) realization. The mathematical modeling of the proposed circuit is derived to match the theoretical model. The proposed circuit is tested experimentally using different excitation signals such as sinusoidal, square, and triangular waves showing an excellent matching with previously reported simulations.

Keywords

Memristor, memductor, mem-element, memristive circuits, emulator, mutator.

1. Introduction

The history of mem-elements was initiated by postulating the existence of the memristor (M) by Chua in his seminal paper in 1971 [1] despite the fact that the memristive behavior was experimentally discovered two centuries ago [2]. Then the basic concept of the memristive devices was introduced by Chua and Kang in 1976 [3]. Later in 2008, a team in HP labs announced that the first solid state memristor was discovered and they introduced the first model of the memristor based on the measurements [4]. The memristor represents the missing relation between the charge q(t) and the flux linkage $\varphi(t)$ that has different characteristics than the well-known elements: resistor (R), capacitor (C) and inductor (L).

Memristive based circuits can participate in very vital applications such as nonvolatile resistive random access memory (ReRAM) [5], [6], analog circuits [7], [8], digital circuits [9], [10], relaxation oscillators [11], [12], [13], chaotic generators [14], and neuromorphic synaptic networks [15]. SPICE models of memristor are essential to design and analyze the complex circuits [16], [17], [18]. New memristive circuit ideas are commonly validated using SPICE models of the memristors first before doing any measurements using solid-state samples [16], [18], [19]. These models study the effect of the boundary of the memristor which models the real solid state memristors.

Due to the lack of commercially available solid state samples, emulator circuits are used to physically mimic the nonlinear dynamics of the mem-elements in various applications. Although, there are many SPICE models which are very useful only for circuit simulation, emulators are needed to be realized in labs in order to enable experimental measurements. Recently, there has been a very intensive research on mem-elements emulators for example, the memristor emulator [20], [21], memcapacitor emulator [22], [23] and meminductor [24]. These emulators were introduced depending on current-, charge- and current-controlled models respectively. The previously published memristor emulators are developed based on current-controlled models but there is no potential research on voltage-controlled models. So, in this work, we are introducing the voltage-controlled memductor emulator for the first time in addition to validation using different excitation signals. In addition, the previous emulators are built using bulky components such as current mirrors, multipliers and dividers. In this work, however, the emulator is built using two simple discrete components and some resistors and capacitors.

This paper is organized as follows: Section 2 discusses the voltage-controlled model of the memductor based on previously reported models as well as the basic building blocks of the memductor. In Section 3, the circuit realization of the memductor is presented with the mathematical modeling of the circuit. In Section 4, the PSPICE simulation and experimental measurements of the proposed circuit are introduced for different voltage excitation signals.

2. Memductor Model

The current-controlled memristor model was discussed in [4] where the constitutive relationship is between the charge q and the flux-linkage φ ; and the memristance is a function of the state variable, current and time. Similarly the model of the memductor was discussed in [25] where the transconductance G_m changes depending on the the accumulated flux so it is called memductor (short for memory + conductance). The change rate of memductance G_m is given as follows:

$$\dot{G}_m(\mathbf{\varphi}) = \mathbf{\alpha} H(\mathbf{\varphi}) \mathbf{v}_m \tag{1}$$

where α is the proportionality constant $(\Omega^{-1}V^{-1}s^{-1})$ and $H(\varphi)$ is considered as a normalized window function having the non-idealities of the memductance change rate. For the sake of simplicity, let's assume that $H(\varphi) = 1$ representing the linear model of the memductor. By integrating both sides relative to time, the memductance is given by

$$G_m = G_{mo} + \alpha \varphi(t) \tag{2}$$

where G_{mo} is the initial memductance. The memductance is linearly proportional to the accumulated flux.

Besides, in [20], the authors introduced a simple double hysteresis model for the mem-elements where the voltage controlled memductor equation is given by

$$i_m = G_s v_m + \frac{G_s v_m}{T V_{ref}} \varphi(t) \tag{3}$$

(4)

where G_s is the initial transconductance, T is the integration factor, and V_{ref} is an arbitrary reference. So the memductance is given by



Fig. 1. I-V hysteresis of the memductor for $G_{mo} = 1 \text{ m}\Omega^{-1}$ for different a) frequencies at $\alpha = 0.01$ and b) α at 1 Hz frequency.

Obviously, both models give the same modeling equation for the memductor where $\alpha = G_s/(TV_{ref})$.

Numerical simulations up on changing different parameters of the memductor are shown in Figs. 1 and 2 for sinusoidal input voltage v(t) with 1 V amplitude and $G_{mo} =$ $10^{-3} \Omega^{-1}$. Fig. 1a shows the current-voltage characteristics of the memductor for three different frequencies where the area inside the hysteresis loops decreases by increasing the applied signal frequency. Moreover, Fig. 1b shows the current-voltage characteristics for three different values of α . Also, it is noted that the hysteresis loops size is dependent on the value of α where the hysteresis loops shrink by decreasing α until it tends to zero and the memductance tends to its initial value G_{mo} . Otherwise, the maximum memductance is given by $G_m = G_{mo} + 2\alpha \frac{A}{\omega}$ for sinusoidal input. The maximum value of the memductance G_m is shown in Fig. 2, for a range of α spanning from 0.001 to 0.1 and for the frequency range of the input signal from 0.01 Hz to 100 Hz.



Fig. 2. The maximum memductance for different frequencies and α .

In oder to implement the memductor in which the behavior of memductance is controlled by flux-linkage, a voltage controlled transconductance is needed in addition to a differential voltage integrator to integrate the voltage across the transconductance and generate the flux which controls the transconductance as shown in Fig. 3.



Fig. 3. Behavioral model of linear memductor.

Otherwise, the non-ideal model of the memductor can be implemented by adding a window function $H(\phi)$ after the integrator to reshape the control voltage and boundary effect of the model.

3. Proposed Emulator Realization

The voltage-controlled transconductance is implemented using LM13700 [26] which is connected as shown in Fig. 4 to implement a floating voltage controlled transconductance G_m where G_m is proportional to the control voltage V_c where its transconductance is given by

$$G_m = 9.6 I_{ABC} \frac{R_A}{R} \tag{5}$$

where I_{ABC} represents the transconductance amplifier bias current. From the PSPICE simulation, it is found that I_{ABC} is linearly proportional to the control voltage ($I_{ABC} = aV_c + I_o$) where *a* represents the reciprocal of the control resistance R_c and I_o is the initial current. The data sheet of the transconductance [26] states that it is recommended to use $R_c = 15 \text{ k}\Omega$ and as a result the corresponding initial current $I_o = 905.057 \ \mu\text{A}$ (These values might vary due to the output offset of the OPAMP). Substituting by I_{ABC} into (5). The transconductance G_m is given by

$$G_m = \frac{0.64R_A}{R}V_c + 8.6885\frac{R_A}{R}(\mathrm{m}\Omega^{-1}).$$
 (6)



Fig. 4. Floating voltage controlled transconductance implementation using LM13700, adopted from [26].

By comparing (2) and (6), the control voltage V_c should represents the flux linkage of the memductor. The flux linkage can be obtained by integrating the difference voltage of the memductor terminals (V_p , V_n) and is given as follows:

$$V_c = \frac{1}{R_1 C_1} \int_{-\infty}^t (V_p - V_n) d\tau = \frac{1}{R_1 C_1} \varphi_{pn}(t).$$
(7)



Fig. 5. Generation of the flux control circuit of the memductor.

The integrator circuit is built as shown in Fig. 5, where an inverting integrator is used and two buffer amplifiers to prevent the loading effect of the integrator on the transconductance circuit. By substituting into G_m , the transconductance is given by

$$G_m = 0.64 \frac{R_A}{RR_1 C_1} \varphi(t) + 8.6885 \frac{R_A}{R} (\mathrm{m}\Omega^{-1}).$$
(8)

The previous equation emulates the memductor's equation where $G_{mo} = 8.6885 \frac{R_A}{R} (m\Omega^{-1})$ and $\alpha = 0.64 \frac{R_A}{RR_1C_1} (m\Omega^{-1}V^{-1}s^{-1})$.

4. Experimental Results

The circuit is practically assembled on a printed circuit board using LM13700 and TL084 (OPAMP) shown in Fig. 6 where C_1 , R_1 , R and R_A equal 1 μ F, 1 k Ω , 100 k Ω and 10 k Ω respectively. The emulator is tested using NI ELVIS Kit and the voltage results are taken to MATLAB to plot current-voltage hysteresis (as NI ELVIS doesn't plot Lissajous curves). In order to obtain the input current of the emulator, a series resistor is connected where the input current is proportional to the voltage difference across it V_R with gain equals to the inverse of the resistor's value R as shown in Fig. 6(c). In the following measurements, a 1 k Ω resistor is used.





Fig. 6. Printed circuit board of voltage-controlled memristor emulator and circuit setup.

In case of the memductor series with a resistor R, the voltage across the memductor $v_m = V_{in}/(1+G_mR)$ where v_{in} is the input voltage, and G_m is the memducatance. By substituting into (2), integrating both sides, and simplifying the resulting equation. The memducatance is given as follows:

$$G_m = -\frac{1}{R} + \sqrt{\left(\frac{1}{R} + G_{mo}\right)^2 + \frac{2\alpha}{R}}\varphi(t).$$
(9)

The memductance is a function of the time integral of the applied voltage signal, flux, so it is very important to study the effect of the basic analog signals: sinusoidal signal and periodic signal such as square and triangular waveforms. Then, substituting the flux to (9) leads to a closed form expression for the instantaneous memductance. In case of applying a sinusoidal signal with amplitude A_o and frequency ω , the flux is given by

$$\varphi(t) = \frac{2A_o}{\omega}\sin^2(\frac{\omega}{2}t) + \varphi_o.$$
(10)

Moreover, in the case of a square signal with A_1 amplitude for positive half cycle and A_2 amplitude for negative half cycle with zero average value, the flux is given by

$$\varphi(t) = \varphi_o + \begin{cases} A_1 \tau & \tau \leq T_h, \\ (A_1 + A_2)\tau - A_2 T_h & T_h < \tau \leq T \end{cases}$$
(11)

where $\tau = mod(t, T)$. These equations give similar results to the experimental results using appropriate values of G_{mo} and α .



Fig. 7. Emulator response under sinusoidal signal at frequencies 10 Hz and 50 Hz.

The proposed emulator is tested using different voltage excitation signals: sinusoidal signal with frequency 10 Hz and 50 Hz, square wave signal with frequency 10 Hz and triangular wave signal with frequency 10 Hz. Figures 7(a) and 7(b) show the transient voltage V_m (blue line) and current V_R (green line) of the emulator for sinusoidal signal with amplitude 1 volt, also Figs. 7(c) and 7(d) show the corresponding double-loop pinched I-V hysteresis of the memductor which shrinks with increasing the input frequency.

Besides, It is very important to study the effect of periodic signal on the proposed emulator especially square wave signal because of hard switching effect. So a square wave signal with amplitude ± 0.5 Volt with 10 Hz frequency is applied as shown in Fig. 8 where the transient voltage v_m (blue line) and current (V_R/R) (green line) showing a high functionality of the emulator to be used in memristor based relaxation oscillators [12], [13]. The voltage across the memductor increases / decreases for positive / negative pulse where the memductance decreases / increases respectively. Moreover, Fig. 9 shows the response of the triangular wave excitation with amplitude ± 1 Volt with 10 Hz frequency and I-V hysteresis in case of triangular excitation.



Fig. 8. Emulator response under square wave signal at frequency 10 Hz; a) transient voltage and current, and b) corresponding I-V hysteresis.



Fig. 9. Emulator response under triangular wave signal at frequency 10 Hz; a) transient voltage and current, and b) corresponding I-V hysteresis.

5. Conclusion

This paper discussed a new simple voltage-controlled memductor emulator circuit where its mathematical model was derived. The effect of changing the emulator parameters was discussed. Moreover, the emulator was assembled experimentally and its functionality was verified for different excitation signals.

References

 CHUA, L. Memristor-the missing circuit element. *IEEE Transac*tions on Circuit Theory, 1971, vol. 18, no. 5, p. 507 - 519.

- [2] PRODROMAKIS, T., TOUMAZOU, C., CHUA, L. Two centuries of memristors. *Nature Materials*, 2012, vol. 11, no. 6, p. 478.
- [3] CHUA, L., KANG, L. Memristive devices and systems. Proceedings of the IEEE, 1976, vol. 64, no. 2, p. 209 - 223.
- [4] STRUKOV, D., SNIDER, G., STEWART, D., WILLIAMS, R. The missing memristor found. *Nature*, 2008, vol. 453, p. 80 - 83.
- [5] ESHRAGHIAN, K., CHO, K., KAVEHEI, O., KANG, S., AB-BOTT, D., KANG, S. Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2011, vol. 19, no. 8, p. 1407 1417.
- [6] VONTOBEL, P., ROBINETT, W., KUEKES, P., STEWART, D., STRAZNICKY, J., WILLIAMS, R. Writing to and reading from a nano-scale crossbar memory based on memristors. *Nanotechnol*ogy, 2009, vol. 20, no. 42, p. 425204.
- [7] PERSHIN, Y., DI VENTRA, M. Practical approach to programmable analog circuits with memristors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2010, vol. 57, no. 8, p. 1857 - 1864.
- [8] SHIN, S., KIM, K., KANG, S. Memristor applications for programmable analog ICs. *IEEE Transactions on Nanotechnology*, 2011, vol. 10, no. 2, p. 266 - 274.
- [9] XIA, Q., ROBINETT, W., CUMBIE, M., BANERJEE, N., CARDI-NALI, T., YANG, J., WU, W., LI, X., TONG, W., STRUKOV, D., et al. Memristor CMOS hybrid integrated circuits for reconfigurable logic. *Nano Letters*, 2009, vol. 9, no. 10, p. 3640 - 3645.
- [10] SHALTOOT, A., MADIAN, A. Memristor based carry lookahead adder architectures. In 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS). 2012, p. 298 - 301.
- [11] ZIDAN, M. A., OMRAN, H., RADWAN, A. G., SALAMA, K. N. Memristor-based reactance-less oscillator. *Electronics Letters*, 2011, vol. 47, no. 22, p. 1220 - 1221.
- [12] FOUDA, M. E., KHATIB, M., MOSAD, A., RADWAN, A. Generalized analysis of symmetric and asymmetric memristive two-gate relaxation oscillators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2013, vol. 60, no. 10, p. 2701 - 2708.
- [13] FOUDA, M., RADWAN, A. Memristor-based voltage-controlled relaxation oscillators. *International Journal of Circuit Theory and Applications*, 2013, DOI: 10.1002/cta.1907.
- [14] BUSCARINO, A., FORTUNA, L., FRASCA, M., GAMBUZZA, L. V. A gallery of chaotic oscillators based on HP memristor. *International Journal of Bifurcation and Chaos*, 2013, vol. 23, no. 5, p. 1330015.
- [15] KOZMA, R., PINO, R. E., PAZIENZA, G. E. Advances in Neuromorphic Memristor Science and Applications, vol. 4. Springer, 2012.
- [16] BIOLEK, Z., BIOLEK, D., BIOLKOVA, V. SPICE Model of memristor with nonlinear dopant drift. *Radioengineering*, 2009, vol. 18, no. 2, p. 210 - 214.
- [17] PERSHIN, Y. V., DI VENTRA, M. SPICE Model of memristive devices with threshold, *Radioengineering*, 2013,vol. 22, no. 2, p. 485 - 489.
- [18] BIOLEK, D., DI VENTRA, M., PERSHIN, Y. Reliable SPICE simulations of memristors, memcapacitors and meminductors. *Radio*engineering, 2013, vol. 22, no. 4, p. 945 - 968.
- [19] JUNTANG YU, XIAOMU MU, XIANGMING XI, SHUNING WANG A memristor model with piecewise window function. *Radioengineering*, 2013, vol. 22, no. 4, p. 969 - 974.
- [20] ELWAKIL, A., FOUDA, M., RADWAN, A. A simple model of double-loop hysteresis behavior in memristive elements. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2013, vol. 60, no. 8, p. 487 - 491.

- [21] KIM, H., SAH, M., YANG, C., CHO, S., CHUA, L. Memristor bridge synapses. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012, vol. 59, no. 10, p. 2422 - 2431.
- [22] YU, D., LIANG, Y., CHEN, H., IU, H., Design of a practical memcapacitor emulator without grounded restriction. *IEEE Transactions* on Circuits and Systems II: Express Briefs, 2013, vol. 60, no. 4, p. 207 - 211.
- [23] FOUDA, M., RADWAN, A. Charge controlled memristor-less memcapacitor emulator. *Electronics Letters*, 2012, vol. 48, no. 23, p. 1454 - 1455.
- [24] LIANG, Y., CHEN, H., YU, D. S. A practical implementation of a floating memristor-less meminductor emulator. *IEEE Transactions* on Circuits and Systems II: Express Briefs, 2014, vol. 61, no. 5, p. 299 - 303.
- [25] SHIN, S., ZHENG, L., WEICKHARDT, G., CHO, S., KANG, S. Compact circuit model and hardware emulation for floating memristor devices. *IEEE Circuits and Systems Magazine*, 2013, vol. 13, no. 2, p. 42 - 55.
- [26] National Semiconductor. LM13700 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers, datasheet.

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