An Offset Cancelation Technique for Latch Type Sense Amplifiers

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Abstract. *An offset compensation technique for a latch type sense amplifier is proposed in this paper. The proposed scheme is based on the recalibration of the charging/discharging current of the critical nodes which are affected by the device mismatches. The circuit has been designed in a 65 nm CMOS technology with 1.2 V core transistors. The auto-calibration procedure is fully digital. Simulation results are given verifying the operation for sampling a 5 Gb/s signal dissipating only 360 μW.*

Keywords

Offset cancelation, sense amplifiers, clocked comparators, latch circuits.

1. Introduction

Latch type sense amplifiers are commonly used in integrated circuits for communications and computer peripherals. They are important timing elements on a system that operates with tight timing restrictions, they need to take fast decisions in limited time window and give a fast output. This type of sense amplifiers are clocked circuits with high sensitivity in order to sense low level signal and high gain to be able to generate an amplified output signal. The required high input sensitivity makes them prone to design issues, technology mismatches and process variations.

There are two main types of latches, current mode and voltage mode. The voltage mode latch-type sense amplifiers are usually preferred because of their low static power consumption and high input impedance. One of the most commonly used latch type sense amplifier with several modifications is the so called StrongARM comparator [1], which is shown in Fig. 1 with several variations. Some of variations include complementary versions of this topology, or with the additional transistors, as depicted with the dashed lines. This circuit is a pre-charged differential sense amplifier followed by a pair of cross-coupled NAND gates. The concept behind its operation is based on charging-discharging of the differential pair and the corresponding nodes. The comparison of the discharging speed, between the nodes, gives a decision to the output stage. In that application [1] it is referred that there is no need for a well balanced amplifier because the input signal is in standard CMOS levels. However, many other applications, like 5 Gb/s serializers/deserializers use lower signal amplitude and sometimes this is only a few tens of milivolts. In this case, it is very important for the total differential pair circuitry, including the total capacitance load on the corresponding nodes, to be well balanced. Otherwise, wrong decision may be taken concerning the input signal. The transistor mismatch is an important issue that can affect the balanced capacitive load reducing circuit's input sensitivity. Using transistors with larger dimensions could reduce the mismatch effect [1], but as the bit rate in modern applications is usually high, the transistor size is critical and should be kept low [2], making the mismatch effect even worse. This effect is equivalent to an input-referred offset created by the difference between the two inputs of the differential input and sometimes could be as high as 50 mV. The offset must be compensated in order to ensure the proper sampling of the sense amplifier.

Several techniques have been proposed for offset cancelation. Most of them are based on capacitance recalibration on the charging-discharging nodes [3]-[5] by adding capacitance on the specific node that shows the less capacitive load. The control is digital, selecting capacitor-transistors among an array in order to rebalance the capacitive load. The concept is shown in the circuit of Fig. 2. Although, this is the most common configuration with the capacitors connected on the nodes *A* and *B*, in some other cases the capacitors have been added on the nodes *C* and *D* [6]. The drawback of this approach is that the capacitance of the transistor is varied with the gate voltage [5], reducing the speed or reducing the linearity of the compensation [6]. So the compensation may become inaccurate while the voltage varies between V_{DD} and ground. In [7]-[10] the offset cancelation is realized by the injection of current in nodes *A* and *B* using parallel connected transistors with the input transistors *M1* and *M2*. These extra transistors that have been added at the input can increase the kickback charge and worsen the CMRR [4]. This design requires Digital to Analog Converters (DACs) for switching on/off the parallel transistors making the final topology too complex. A recent work utilizes charge-pump and bulk control [11], while some older techniques used preamplifiers in a unity-gain closed loop, to create input and output offset storage [12].

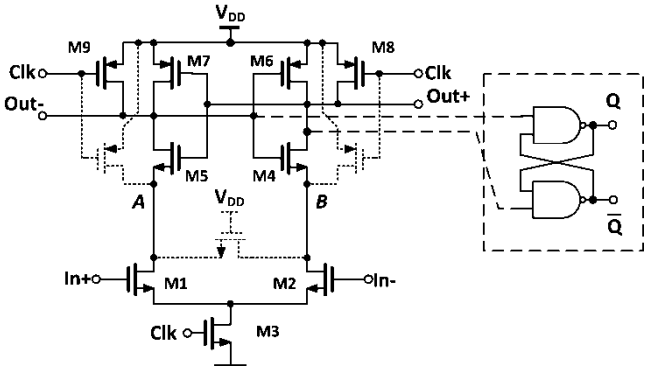

Fig. 1. StrongARM Latch type sense amplifier.

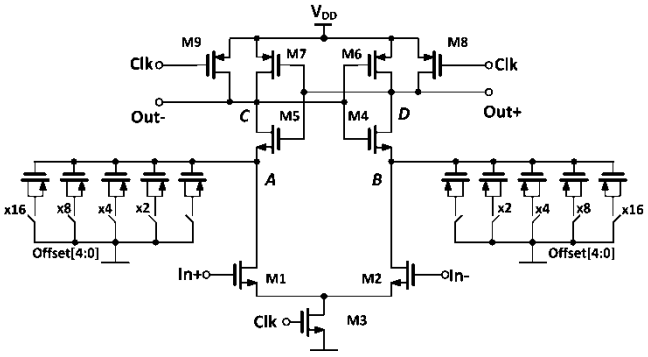

Fig. 2. Offset cancelation scheme based on capacitance control.

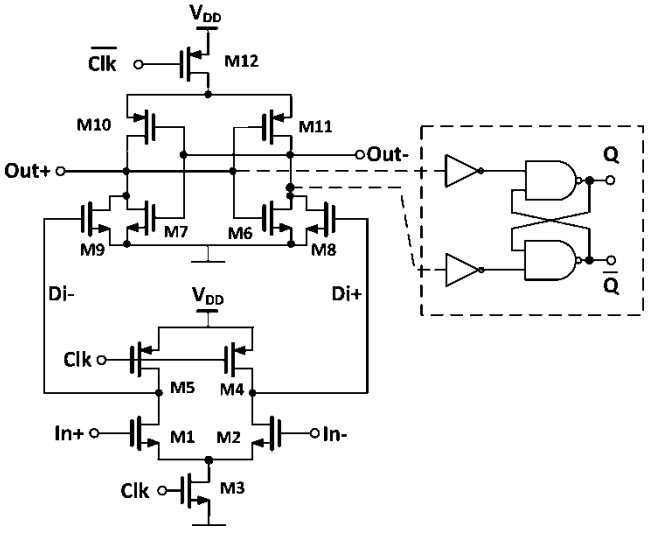

Fig. 3. Improved latch type sense amplifier.

A new accurate technique for the offset cancelation is proposed in this paper. This is based on the current injection in the comparison nodes, without affecting the differential input pair and it is applied on a low voltage latch-type sense amplifier [13]. The result is an accurate offset compensation technique using a low supply voltage, with a very simple and area efficient circuit. In addition, it does not significantly affect the kickback noise and the output delay of the latch-type comparator, while shows smaller power consumption comparing with other proposed topologies.

2. Latch-Type Sense Amplifier

A latch type sense amplifier suitable for a 5 Gb/s deserializer is the double-tail-latch-type sense amplifier, shown in Fig. 3 [13]. Comparing it with the Strong-Arm clocked comparator, this sense amplifier has fewer transistors stacked from rail to rail, has better isolation between input and output and is less sensitive to common mode variation. Though, it needs positive and negative clock.

The Strong-Arm comparator has some drawbacks, as thoroughly analyzed in [14] due to the placement of the cross-coupled inverters in series with the differential pair and because there is only a very short time within one period in which the differential pair has actually gain. This makes it sensitive to common mode input signal, especially when, like in our application, this is close to V_{DD}. Also, the total current is identical for latch and differential pair leaving no space for optimization. The double-tail comparator improves these drawbacks by separating the differential pair with the cross-coupled latch [13]-[16]. The performance under low supply conditions is improved due to fewer transistors stacked. The tail current in the differential pair (through transistor *M3*) is significantly lower than the current of the latching stage (through transistor *M12*) providing high differential gain with fast latching. Then, the decision time can be significantly small while the gain of the operational amplifier is still high, resulting to decreased probability of metastability errors. The fact that the high current flows only in the second stage, which is isolated by the intermediate stage formed by *M8* and *M9*, provides additional shielding to the first stage thus exhibiting less kickback noise. For the aforementioned reasons the double tail sense amplifier has been chosen for our application.

The latch operation of the circuit in Fig. 3 is based on the comparison of the charge between the nodes *Di+* and *Di-* as shown in Fig. 4. It operates in four phases: reset, sample, regeneration and decision. During the reset phase, when *clk* is 0, as shown in Fig. 4a, the input signal goes close to its final logic state (Fig. 4b). The transistors *M4* and *M5* pre-charge the *Di* nodes to V_{DD} as depicted in Fig.4c and transistors *M8* and *M9* discharge the nodes *Out+* and *Out-* to ground, as shown in Fig. 4d. During the sample phase, at the positive edge of the clock, both transistors *M3* and *M12* are turned on. Nodes *Di* start discharging with a rate, approximately, of $I_{M3}/2C_{Di}$. Because of the differential input voltage V_{In}, transistors *M1* and *M2* give different drain current, and the transistor with the higher input voltage help the corresponding drain to discharge slightly faster. A ΔV_{Di} is created, during the sample phase, which is passed by *M8* and *M9* to the cross-coupled inverters, formed by transistors *M6*, *M11* and *M7*, *M10* during the regenerating phase. During this phase, the

two inverters start generating the output decision. The role of the transistors *M8* and *M9* is important not only transferring the differential voltage to the next stage but also, minimizing the kickback effect to the input. An SR-latch is connected after *Out+* and *Out-* to create a static output *Q*, as shown in Fig.4e. The SR-latch is always used in latch-type sense amplifiers to keep the final output *Q* constant during the reset phase where both nodes *Out+* and *Out-* return to zero voltage.

Depending on the application, the output stage can be developed by a more sophisticated SR-latch instead of the common SR-latch in order to improve the symmetry in crossing points, rice and fall times, duty cycle, etc [17].

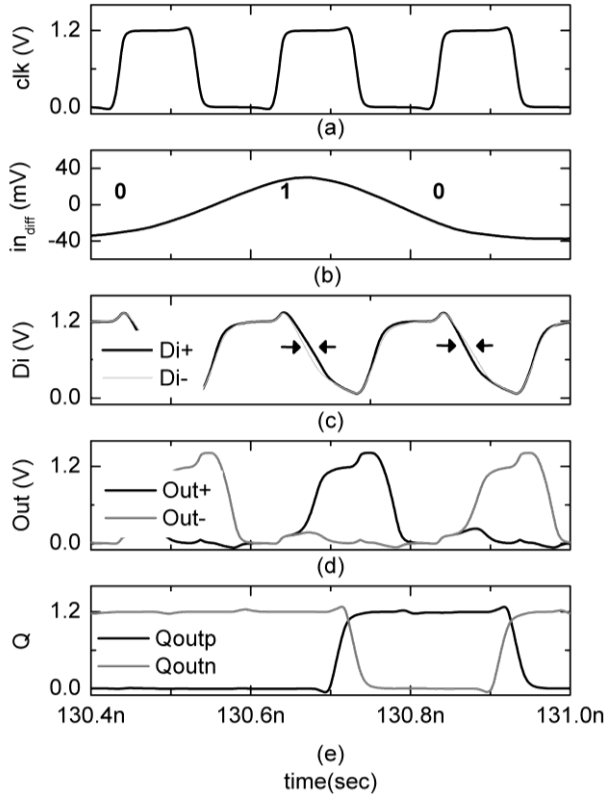

Fig. 4. Signaling of the latch type sense amplifier a) clock, b) differential input, c) charging nodes *Di*, d) pre-output and e) final output Q.

In our design the common SR-latch was selected among other, more advanced topologies that showed, however, high sensitivity on process variations derived from Monte-Carlo simulations. The reason for this high sensitivity is the increased complexity which although improves the operation, at the same time makes the circuit vulnerable to transistor mismatches. The decision phase takes place during the positive edge of the *clk* signal. The drain current I_{D3} of *M3* becomes, then, high and all transistors operate in saturation region. Depending on the input voltage V_{In} the drain currents of the identical transistors *M1* and *M2* are, respectively,

$$I_{D1} = \beta\left(V_{In+} - V_T\right)^2, \tag{1}$$

$$I_{D2} = \beta\left(V_{In-} - V_T\right)^2 \tag{2}$$

where β is the technology transconductance parameter $\beta = \mu_o C_{ox} W/2L$, $V_T = V_{S1} - V_{th}$, W and L is the width and length of *M1* and *M2*, V_{S1} is the *M1* and *M2* source voltage and V_{th} the threshold voltage of the transistors. The current difference is [18],

$$\Delta I = 2\beta\left(V_{CM} - V_T\right)\Delta V_{In} \tag{3}$$

where V_{In} is the differential input voltage and V_{CM} the common mode input voltage, as given in (4) and (5)

$$V_{In} = V_{In+} - V_{In-}, \tag{4}$$

$$V_{CM} = \left(V_{In+} + V_{In-}\right)/2. \tag{5}$$

From (3) it is obvious that the common mode input must be greater than the threshold voltage depending on the process and the source voltage of *M1*, *M2*. Some important currents and voltages on the internal nodes of the amplifier consisting of the transistors *M1-M5* are shown in Fig. 5. The period of time where the three phases, sample, regeneration and decision take place after reset, is illustrated in the shaded area. During the positive edge of the clock, shown in Fig. 5a, the input signal is already at the logic state of either 0 or 1. Its amplitude may be as low as 40 mV differential, as shown in Fig. 5b. Also, during the positive clock edge the differential pair consisting by transistors M1 and M2 becomes active very fast, as shown in Fig. 5c and Fig. 5d, but they have a small difference between their drain currents, which depends on the logic level of the input signal. The absolute current difference is shown in Fig. 5e. At the same time the nodes *Di* discharge at a slightly different rate, as shown in Fig. 5f and according to the current difference of the differential pair, generating a differential voltage between the nodes Di, as shown in Fig. 5g. The high gain of the differential pair *M1-M2* is important for creating a high differential voltage ΔV_{Di}. The differential amplifier's gain is given by,

$$A_d = g_m r_o \tag{6}$$

where g_m is the transconductance of the transistors *M1*, *M2* and r_o is the equivalent resistance on the nodes *Di*. Large transistors not only aim to create high transconductance but keep the mismatch at low levels which is important to create proper output decisions, particularly if the input is of an extremely low amplitude as in the case shown in Fig. 5, where the differential input amplitude is less than 40 mV. On the other hand the wide transistors reduce the operating frequency as they add higher capacitive load on the nodes *Di*. This can deteriorate the aperture time and leave a small time window for the reset phase, resulting to a higher number of decision errors.

3. The Proposed Offset Compensation Technique

The mismatch between the symmetric transistors is a significant effect that can lead the latch to completely false decisions, especially if the input voltage level is very small. The mismatch creates an equivalent offset which must be compensated. The offset V_{off} created by the switching differential pair with mismatch transistors is studied in details in [18] and is found equal to

$$V_{off} = \Delta V_{th} - \frac{\Delta\beta}{2\sqrt{2\beta}}\sqrt{\frac{I_{D3}}{\beta}}, \tag{7}$$

$$\beta = \frac{\beta_1 + \beta_2}{2} = \frac{1}{2}\left(\frac{\mu C_{ox} W_1}{2L_1} + \frac{\mu C_{ox} W_2}{2L_2}\right) \tag{8}$$

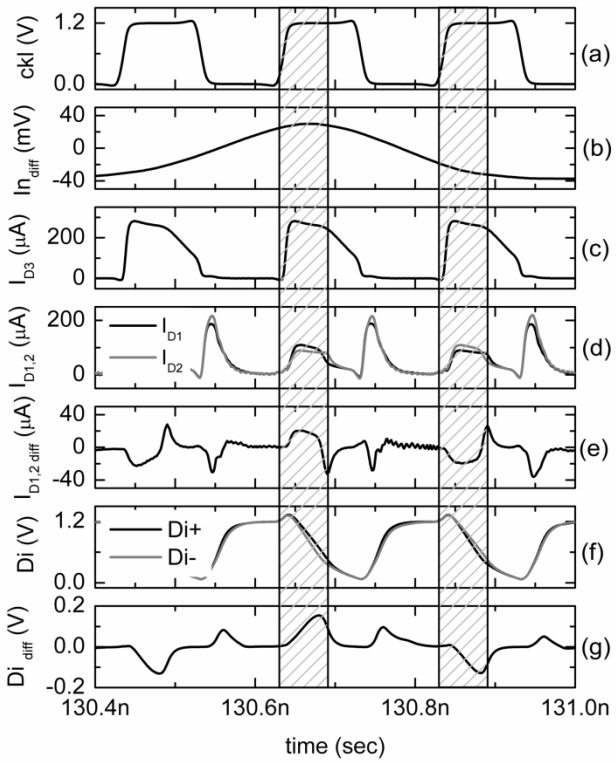

Fig. 5. Current and voltage in transistors M1-M5 a) clock b) differential input c) drain current of M3, d) drain current of M1 and M2, e) difference of drain currents of M1 and M2, f) voltage on charging nodes *Di*, g) differential voltage of *Di+*/*Di-* nodes.

where $\Delta\beta=\beta_1-\beta_2$ is the difference between the technology transconductance parameters of the two transistors and ΔV_{th} is the difference of the threshold voltage.

The proposed compensation technique was implemented mainly due to the common mode signal sensitivity of the capacitor compensation approach. A detailed analysis including simulation results of that method is given in [5]. Also, the additional capacitors affect the slew rate of the differential pair and may worsen the aperture time, limiting the operation of the clocked comparator. The operating frequency can be estimated by

$$f = \frac{1}{2\pi C_{Di} r_o} \tag{9}$$

where, C_{Di} is the total capacitance on node *Di* and r_o is the equivalent resistance on those nodes. Above this frequency the gain of the differential pair is gradually reduced.

The discharging rate on each branch of *M1* and *M2* can be controlled not only by the capacitive load but also by the current flowing through these transistors. While some proposed methods use calibrated differential pair to cancel the offset, in our case the discharging current can be controlled by the transistors *M4* and *M5*. Connecting transistors in parallel with *M4* and *M5* the total mismatch influence on the discharging rate can be compensated. The proposed topology is shown in Fig. 6. Although these transistors add load on the clock path, this is not important for two reasons: firstly, because the clock is connected on the transistors through switches and secondly, because the standard high swing CMOS signal is strong enough to drive any block in the system through buffers from the clock tree. In this case, it is preferable to slightly load the clock path over loading any other critical signal nodes coming from the input.

The detection of the mismatches takes place during the training phase of the system. If the pairs *M1-M2* and *M4-M5* are perfectly matched, then the transistors from both sides of the transistor arrays are disconnected. In the case where a mismatch exists, then a proportional number of the weighted transistors are set to on in order to compensate for the mismatch effect. During the training phase there is no data transmission and the two inputs (positive and negative) of the latch type sense amplifier are tied on the same common mode voltage, around 0.9 V, generated by the previous stage. The accurate value of the common mode voltage is not critical for the offset compensation because of the differential nature of the topology, although, it might be critical for the output delay in normal operation [13], depending on the specific topology of the latched comparator. At first, only the transistors of one side are enabled. This enforces the output *Q* at ground potential. A counter starts disabling the transistors from one side to the other. The counting takes place with a clock running at lower speed than the maximum available. This ensures that the compensation procedure will be performed in lower speed, giving all the required time to the counter and to sense amplifier to find accurately the right selection. During this process, whenever the output *Q* changes state from ground to V_{DD}, as shown in Fig. 7b, the counting stops, as shown in Fig. 7a and the selected compensating transistors are locked in their final state using memory latches. The recalibration could be restarted if required by setting the reset signal from 0 to 1, as shown in Fig. 7c. The merit here is that there is no need for recalibration until the next power-on of the system. A possible temperature variation during the operation has

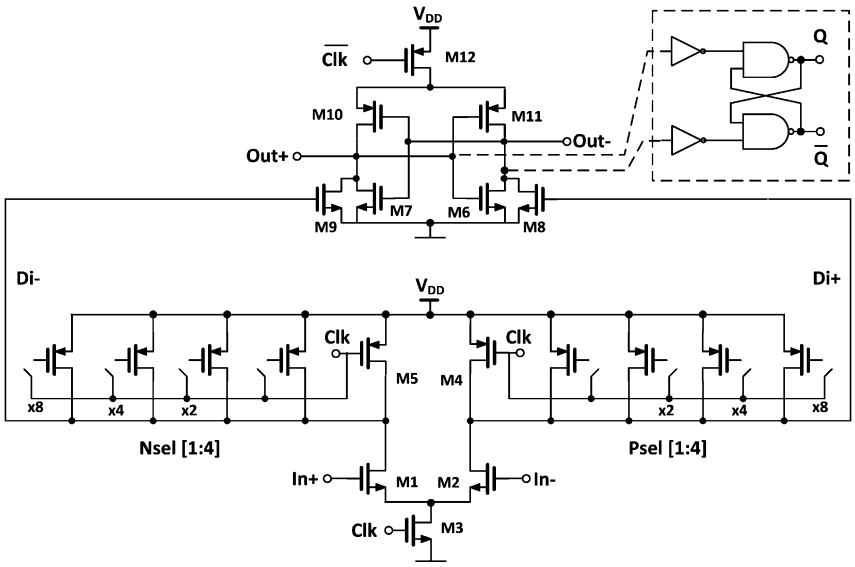

Fig. 6. Improved latch type sense amplifier with offset compensation.

not a potential effect, in first order, due to the differential nature of the circuit.

This compensation technique could be combined with other comparators, as for example with modified versions of the Strong-Arm taking advantage of the transistors with the dashed lines, shown in Fig. 1. These transistors already used to better reset the *Di* nodes and they could be used to control the offset. However, this requires a major redesign of the sense amplifier including the transistors in order to optimize its operation and therefore this design procedure has not been performed.

4. Simulation Results

The double tail latch type sense amplifier with the proposed offset compensation method has been designed in 65 nm CMOS technology and the postlayout simulation results demonstrate the operation before and after the compensation. Only standard threshold transistors (SVT) and not low V_{th} transistors (LVT) were used in this design. The transistors aspect ratio is depicted in Tab. 1. The supply voltage is 1.2 V and the input voltage used for demonstration and verification was less than 20 mV single-ended input. In reality the signal expected at this point on a full system implementation is greater than this value. The data input rate was 5 Gb/s.

Monte-Carlo analysis was performed for the same input with and without compensation. A differential rising ramp voltage is applied to the input in order to test the offset. If the sense amplifier is perfectly matched, then the output changes its state from low to high, when the differential input voltage is zero. In Fig. 8a the switching output *Q* is shown for multiple Monte-Carlo runs without compensation and in Fig. 8b with compensation, when the rising ramp voltage feeds the input in a corresponding time,

Transistor	W (nm) / L (nm)
M1,M2	3120 / 120
M3, M8, M9	600 / 60
M4, M5	1200 / 120
M6, M7	780 / 60
M10, M11	3120 / 60
M12	6240 / 120

Tab. 1. The transistors' aspect ratio.

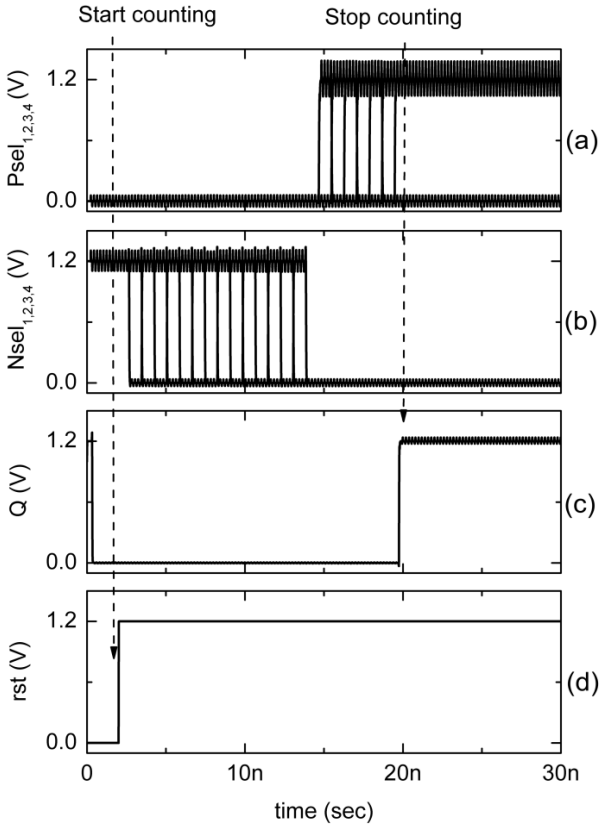

Fig. 7. Counting select bits of a) right side transistors, b) left side transistors and c) reset signal.

as shown in Fig. 8c. Without the compensation, the offset is found to be within the range of ±40 mV, as shown in Fig. 8a. After the compensation the offset is limited into the range of ±2.5 mV. The output *Q* is shown in Fig. 8a and Fig. 8b to change state in quantized values due to clocked operation.

Although the range could be further improved, the obtained° result is good enough for almost any application and therefore no more effort has been given to improve it. However, possible improvement can be accomplished by achieving better resolution of the compensation transistors and increasing the number of control bits. Running 30 Monte-Carlo runs the offset deviations without and with the compensation, respectively, are shown in Fig. 9a and Fig. 9b.

When the offset cancelation process is finalized, some extra transistors stay connected in parallel with *M4* or *M5* in Fig. 6 to create an actual balance in charging/discharging process. After the calibration and under high temperature variation a new small input offset may be regenerated due to varied unbalanced g_m of the correspond transistors. Simulations showed that this is negligible and it is about 2 mV. However, it does not affect the operational ability of the circuit, as the input signal is always much higher than this level. This effect is even smaller in the case of supply voltage variations. The simulation showed negligible offset for supply voltage from 1.1 V to 1.3 V.

The kickback noise in the clocked comparators is important and should not only be kept low, but also to be as invariant from the compensation as possible. The parallel connected transistor in *M4* and *M5* create the current balance between the two branches of *M1* and *M2*, but the total current tail, which finally is responsible for the higher amount of kickback effect, is controlled by *M3*. The current between the two branches has only a small difference, as shown in Fig. 5. The influence of the compensating transistors into the total kickback is small because they only rebalance the available current and they do not increase the total current. For testing purposes, this can be shown by applying common mode signal in the latched-comparator and starting the counting process as doing to find the offset voltage. All the left transistors are initially connected and gradually disconnected. The results are shown in Fig. 10 where in Fig. 10a the counting-down of the switches is depicted and in Fig. 10b the differential input voltage with kickback noise. Fig. 10c and Fig. 10d depict individually the kickback noise in the two inputs *In+* and *In-*, respectively showing the small effect of the compensating on the kickback noise.

The output delay was measured with and without the proposed compensation technique. The results are shown in Fig. 11 where an insignificant additional delay of 5.7°ps is observed (Fig.°11a) due to the connected compensating transistors. This delay is shown when all the compensating transistors are off, but it worsens only 3 ps, when the one side of the transistors are on to compensate an offset of about 25°mV. The delay without the compensation is 39°ps measured from the positive edge of the clock, as shown in Fig. 11b and Fig. 11c, respectively. The active transistors add current helping the slower node to discharge faster. Therefore, there is no significant additional delay. The main difference with the commonly used capacitance-compensation technique is the capacitance added in order to equalize the faster discharging node *Di* with the slower discharging node giving additional total delay to the decision phase.

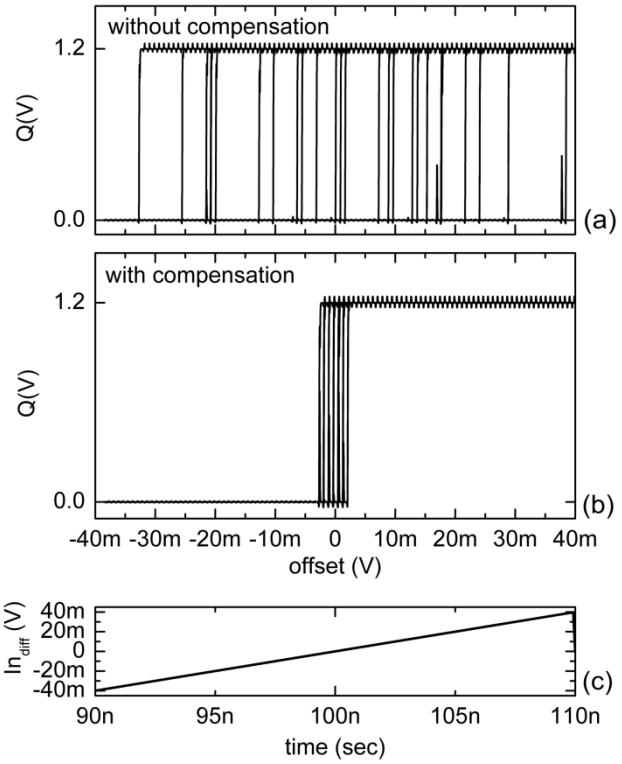

Fig. 8. Offset demonstration a) before and b) after compensation c) with a ramp input signal.

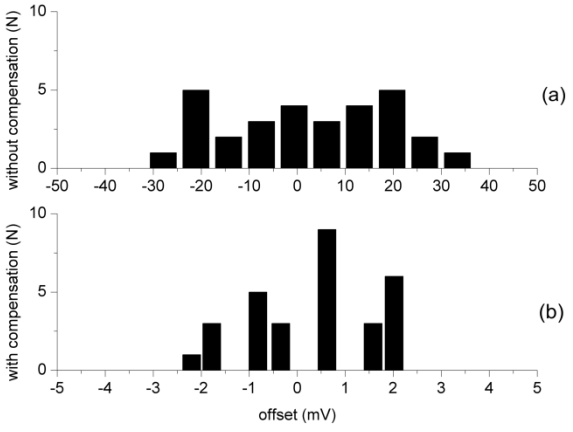

Fig. 9. Offset deviations from Monte-Carlo simulations a) before and b) after compensation.

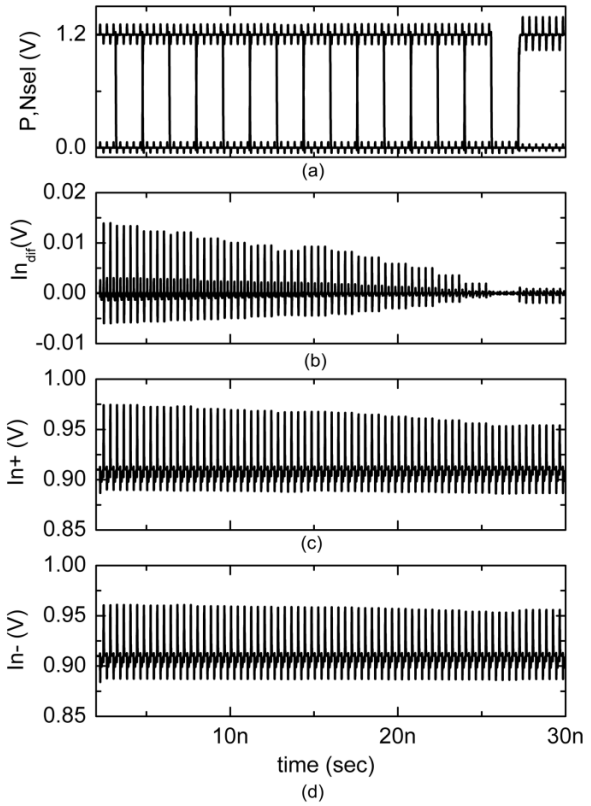

Fig. 10. Kickback noise during the offset compensation process a) right side transistors counting, b) kickback on differential input signal, c) kickback on positive input and d) kickback on negative input.

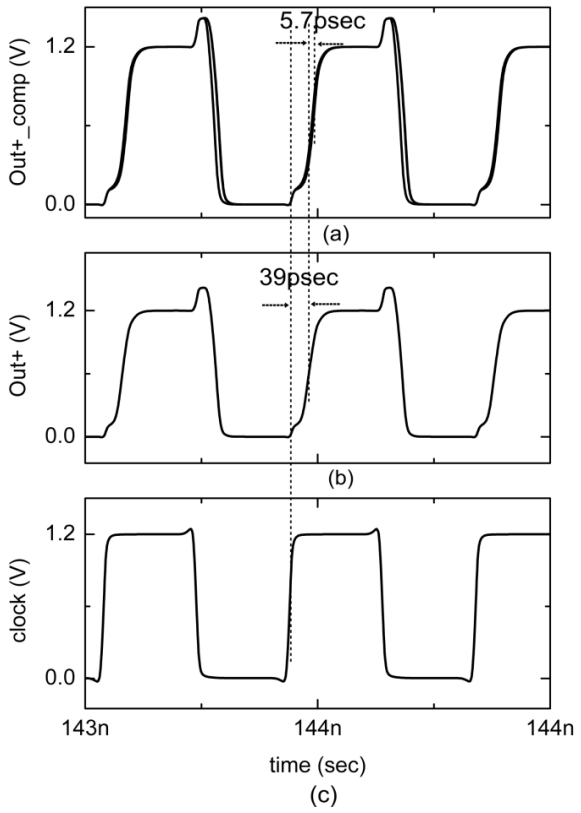

Fig. 11. Output delay a) after the offset compensation, b) before the compensation and c) the clock reference.

The layout of the latch type sense amplifier is shown in Fig. 12. The total area is 31 μm x 33 μm, including the additional SR-latch of the output and the digital counter which is used to select the correct number of the compensating transistors.

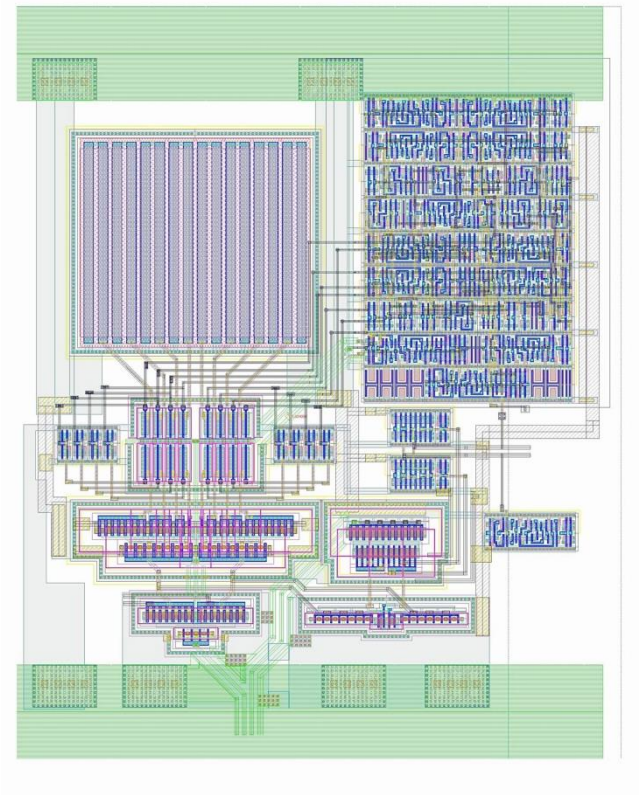

Fig. 12. The layout of the latch type sense amplifier.

The key characteristics of the proposed technique, together with these of some previously published offset compensation topologies are presented in Tab. 2. It should be noted that most of the tabular data in Tab. 2 are measurement results, but in our case the reported findings are based on post-layout simulations and Monte-Carlo analysis. One important point in the proposed technique is that the delay is not affected by the compensation. This is because no capacitive load is added on any of the internal nodes, as in [3], [4], [6] and the current injection in the proposed method is performed in the PMOS clock transistors. Also, that means that the differential pair remains untouched and small in size, without overloading the preceding stage that could be sensitive. This assures that the proposed topology has the minimum power consumption over frequency as shown in Tab. 2. Furthermore, the suggested method is immune to common mode voltage unlike other similar methods, which use mos-capacitors. The layout area is the smallest compared with other techniques and the power consumption is the best compared with the high speed comparators, due to the absence of the compensating capacitors.

Although the residual offset is not the minimum found in the relevant literature, is not far off and is good enough for our application, as the input signal must be

Work	CMOS feature size (nm)	Sample rate (Gb/s) or clock (GHz)	Offset before compensation (mV)	Type of compensation	Area (μm x μm)	Supply Voltage (V)	Power consumption (mW)	P/f (mW/ GHz)	Residual offset (mV)
[3]	250	1.6 GS/s	±70	Capacitive	80 x 50	2.5	3	1.875	±6
[4]	90	3.2 GHz	±70	Capacitive	N.A.	1.0	N.A.	N.A.	±1.5
[6]	90	1.5 Mb/s	18	Capacitive	N.A.	0.5	N.A.	N.A.	±1
[7]	65	1.5 GS/s	19	Current injection in diff. pair	N.A.	1.1	N.A.	N.A.	4.75
[8]	180	1.4 GHz	95	Current injection in diff. pair	N.A.	1.8	0.35	0.25	13
[9]	90	250 MHz	13.7	Current injection in diff. pair	120 x 4.5	1.0	0.04	0.16	1.69
[11]	180	200 MS/s	29.9	Charge pump and bulk driven	N.A.	0.5	0.034	0.17	0.3
This work	65	5 GS/s	40	Current injection in clock transistors	31 x 33	1.2	0.36	0.072	±2.5

Tab. 2. Key characteristics of the different offset compensation techniques.

always greater than 30 mV differential according to the system specifications. The performance in terms of speed and supply voltage can be improved significantly by taking advantage of the low threshold voltage transistors (LVT) offered by the selected process. However this will require additional masking costs when comes to fabrication. For all the reasons described above the proposed technique outperforms all of the previously reported schemes, especially when the output delay performance is important.

5. Conclusions

A new offset compensation technique for latch-type sense amplifier has been presented. The proposed topology controls the bias current of the clocked transistors instead of changing the capacitance on the internal nodes of the sense amplifier. Therefore, it does not need any preamplifier, the linearity does not depend on the voltage of the capacitor transistors which usually are used for the compensation and the calibration process is in a fully digital way. It can operate at 5 Gb/s data rate with 1.2 V voltage supply using typical CMOS transistors (SVT) consuming only 360 μW. The final offset is reduced from ±40 mV to only ±2.5 mV which is much better than the required for most of high speed applications.

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