Low Voltage Floating Gate MOS Transistor Based Four-Quadrant Multiplier

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Abstract. *This paper presents a four-quadrant multiplier based on square-law characteristic of floating gate MOSFET (FGMOS) in saturation region. The proposed circuit uses square-difference identity and the differential voltage squarer proposed by Gupta et al. to implement the multiplication function. The proposed multiplier employs eight FGMOS transistors and two resistors only. The FGMOS implementation of the multiplier allows low voltage operation, reduced power consumption and minimum transistor count. The second order effects caused due to mobility degradation, component mismatch and temperature variations are discussed. Performance of the proposed circuit is verified at ±0.75 V in TSMC 0.18 μm CMOS, BSIM3 and Level 49 technology by using Cadence Spectre simulator.*

Keywords

FGMOS, low-voltage, low-power, four-quadrant, multiplier.

1. Introduction

Increasing density of components on chip and growing demand of battery-powered portable equipments have directed the research towards the development of low-voltage low-power analog signal processing circuits. Such research involves finding new and promising design techniques so that the complete system could meet the specified design constraints. Threshold voltage is one of the most important design parameter for low voltage analog circuit designers. Threshold voltage reduction not only helps in reducing the supply voltage requirement but also the power consumption in many analog applications. Various low-voltage low-power techniques reported in literature include sub-threshold MOSFETs, level shifters, self cascode, bulk-driven and FGMOS techniques [1–10]. In the last few years, FGMOS transistor has gained wide popularity because of its ability to reduce or remove the threshold voltage requirement of the circuit. Recently number of publications showing the application of FGMOS in various analog signal processing circuits such as voltage squarer and multiplier have been reported [7–11].

Four-quadrant multiplier is an important and very useful building block in many analog signal processing circuits such as modulators, frequency doublers, adaptive filters etc. The Gilbert six transistor cell based on variable transconductance technique is very popular in bipolar technology [12], [13]. The proposed configuration uses exponential characteristic of bipolar transistor and is useful for the frequency ranging from DC to unity gain frequency of BJT. Although the Gilbert multiplier has been the most widely used bipolar multiplier, it is not suitable for low voltage applications. Kimura [14] has proposed a bipolar multiplier which can operate at lower supply voltage (< 3 V) and can replace Gilbert multiplier for low voltage operation. The results of the multipliers based on MOS square-law characteristic are not as good as that produced by using exponential characteristic of BJT. Hence, several linearization techniques have been used to improve the performance of MOS based multipliers [15–19]. The multiplier proposed by Qin and Geiger [16] is based upon MOS version of Gilbert cell and uses differential active attenuators to increase the input signal swing. Soo and Meyer [17] have used cascaded MOS differential pair to implement four-quadrant multiplier with linearity comparable to bipolar circuits over a wide input range. The simplest form of four-quadrant analog multiplier consists of a pair of MOSFETs, a pair of current/voltage convertors and a subtractor. The multiplier based on this concept employs various resistive components and leads to serious problems such as large power consumption and large offset error. To overcome these issues, the four-quadrant multiplier based on switched capacitor technique has been proposed by Yasumoto and Enomoto [20]. The multiplier exhibits excellent characteristics such as low THD, large dynamic range and high-speed operation. Most of the multipliers based on MOS square law characteristics have low input range and small bandwidth. To overcome this issue, various BiCMOS based multipliers have been reported in [21–23]. These multipliers combine the high input impedance property of MOS transistor along with the linearity and high speed of bipolar transistors. Another technique to implement analog multiplier is the use of active blocks [24], [25] such as operational amplifiers, current conveyors, and second generation current-controlled conveyors. Recently, the multipliers based on FGMOS transistors [26–29] have gained wide popularity because of their high

input range. But most of these designs operate at high supply voltage and have complex structure. This paper presents a very simple four-quadrant multiplier based on square law characteristic of FGMOS, consisting of eight FGMOS transistors and two resistors only.

This paper is organized as follows: The basic structure and operation of FGMOS transistor is described in Section 2. The principle of operation of the proposed multiplier is presented in Section 3. Second order effects over the proposed configuration are discussed in Section 4. Section 5 deals with the simulation results. Finally the conclusions are drawn in the last section.

2. FGMOS Transistor

FGMOS is a multiple-input floating-gate transistor whose floating gate is formed by the first polysilicon layer and multiple-input gates are formed by the second polysilicon layer. Symbol of N-input FGMOS with input voltages V_1, V_2…..V_N and its equivalent circuit are shown in Fig. 1a and 1b respectively.

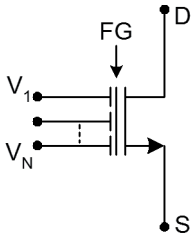

Fig. 1a. Symbol of N-input FGMOS.

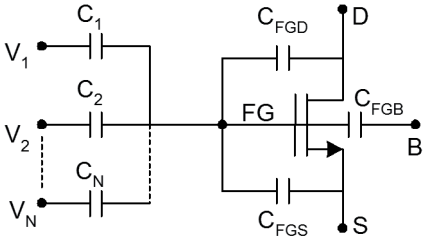

Fig. 1b. Equivalent circuit of FGMOS.

The drain current (I_D) of the FGMOS transistor operating in saturation region is given by [10]

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N}\frac{C_i}{C_T}V_{is} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} + \frac{Q_{FG}}{C_T} - V_T\right)^2 \quad (1)$$

where C_i is the set of input capacitors associated with effective inputs and the floating gate; C_{FGD}, C_{FGS} and C_{FGB} are the parasitic capacitances of floating gate with drain, source, and bulk respectively; V_D, V_S and V_B denote the drain, source and bulk voltages respectively. Q_{FG} is the residual charge trapped in the oxide-silicon interface during fabrication process, β is the transconductance parameter and V_T stands for the threshold voltage.

$C_T\left(=\sum_{i=1}^{N}C_i + C_{FGS} + C_{FGD} + C_{FGB}\right)$ is the total floating gate capacitance. Assuming $C_i >> C_{FGD}$, C_{FGB} and $Q_{FG} = 0$ [28], the drain current of FGMOS transistor in saturation region can be expressed as

$$I_D = \frac{\beta}{2}\left(\sum_{i=1}^{N}k_i V_{iS} - V_T\right)^2 \quad (2)$$

where $k_i = C_i/C_T$. It can be seen from (2) that the multiple input voltages along with capacitance ratio can be used to cancel the threshold voltage term so as to get the perfect squaring function which in turn is used to realize the proposed multiplier.

2.1 Analysis of Two-Input FGMOS Transistor

Two-input FGMOS transistor with inputs V_b (bias voltage) and V_{in} (input signal) is shown in Fig. 2.

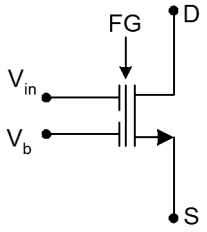

Fig. 2. Two input FGMOS transistor.

For 2-input FGMOS (with source grounded), the drain current equation (2) is modified as

$$I_D = \frac{\beta}{2}\left(\frac{C_1}{C_T}V_b + \frac{C_2}{C_T}V_{in} - V_T\right)^2. \quad (3)$$

From (3) the effective threshold voltage is given as [30]

$$V_{Teff} = \frac{V_T - k_1 V_b}{k_2} \quad (4)$$

where $k_1 = C_1/C_T$, $k_2 = C_2/C_T$, are the capacitive coupling ratios and $C_T = C_1 + C_2$ is the total capacitance after neglecting the parasitic capacitances.

Equation (4) shows that the threshold voltage of the FGMOS transistor can be tuned and made much lower than the threshold voltage of the standard MOSFET by choosing proper values of V_b, k_1, k_2.

Fig. 3 shows the DC transfer characteristic of FGMOS and standard MOS transistor. For the FGMOS transistor, the value of bias voltage $V_b = 0.75$ V and the capacitive coupling ratio $k_1 = k_2 = 0.5$. It is observed that in case of FGMOS transistor the threshold voltage is completely removed from signal path by choosing proper value of bias voltage.

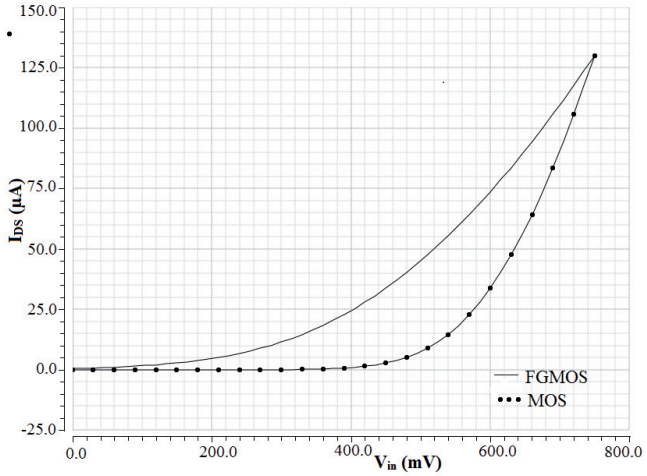

Fig. 3. Transfer characteristic of standard MOS and FGMOS transistor.

3. Proposed Four-Quadrant Multiplier

The principle of operation of the proposed multiplier is based on well known square-difference identity and is given by

$$V_{out} = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2 . \quad (5)$$

It is evident from (5) that in order to implement the multiplier function, square of the sum and difference of two voltages V_1 and V_2 are needed. The squarer circuit (proposed by Gupta et al.) used to implement the squared sum and difference of two inputs V_1 and V_2 is shown in Fig. 4 [31].

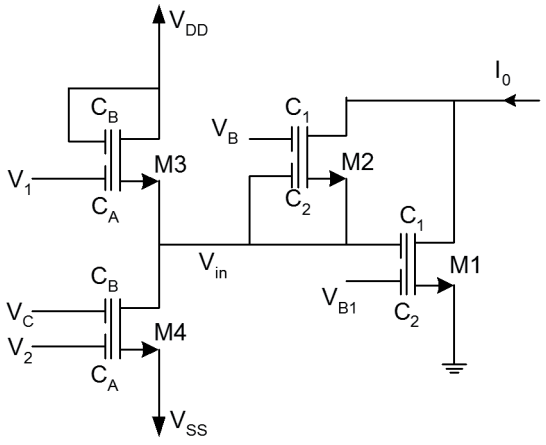

Fig. 4. Squarer circuit [31].

The output current of the basic squarer [32] (formed by transistors M1 and M2) after neglecting the parasitic capacitances, channel-length modulation, mobility degradation and the body effect is given by

$$I_o = \frac{\beta_1}{2}(k_1V_{BS1} + k_2V_{inS1} - V_{T1})^2 \quad if\ V_{in} > 0 , \quad (6)$$

$$I_o = \frac{\beta_2}{2}(k_1V_{BS2} + k_2V_{inS2} - V_{T2})^2 \quad if\ V_{in} < 0 . \quad (7)$$

If $\beta_1 = \beta_2 = \beta$, $V_{T1} = V_{T2} = V_T$, $k_1 = k_2 = k$ and $kV_B = V_T$ then the output current of the squarer can be approximated as [32]

$$I_o = \frac{\beta}{2}(kV_{in})^2 . \quad (8)$$

The input voltage V_{in} of the squarer is generated by voltage attenuator formed by FGMOS transistor M3 and M4. The output voltage of the attenuator is given by [26],

$$V_{in} = \alpha(V_1 - V_2) + \frac{k_AV_{SS} - k_BV_C}{k_A + k_B} \quad (9)$$

where $k_A = C_A/(C_A + C_B)$, $k_B = C_B/(C_A + C_B)$ are the capacitive coupling ratios and $\alpha = k_A/(k_A + k_B)$, is the attenuation factor which can be tuned by choosing proper values of k_A and k_B. From (9) it can be seen that the offset voltage term $(k_A V_{ss} - k_B V_C) / (k_A + k_B)$ can be cancelled by the proper choice of the bias voltage V_C. For offset cancellation, the bias voltage V_C must be equal to

$$V_C = \frac{k_A}{k_B}V_{SS} . \quad (10)$$

Assuming zero-output offset for the voltage attenuator, the output current of the squarer using (8) and (9) is given as

$$I_o = \frac{\beta}{2}\{k\alpha(V_1 - V_2)\}^2 . \quad (11)\backslash$$

If $k\alpha = k_{eq}$, (11) can be written as

$$I_o = \frac{\beta}{2}\{k_{eq}(V_1 - V_2)\}^2 . \quad (12)$$

It can be seen from (12) that the squarer (Fig. 4) gives the output current proportional to the difference of input voltages V_1 and V_2 and the voltage range of the squarer can be determined by the factor k_{eq}.

The proposed multiplier (Fig. 5) has been implemented by using two squarers shown in Fig. 4. The first squarer (Fig. 5) has been formed by transistors M1, M2, M3, M4 with inputs V_1 and V_2; the second squarer has been formed by transistors M1d, M2d, M3d, M4d with inputs V_1 and $-V_2$. Since the inputs are applied at the gates of FGMOS transistor, so the proposed configuration has very high input impedance. The output impedance of the proposed multiplier can be given as

$$R_{out} = R_1 \| r_{Ox} = R_2 \| r_{Oy} \quad (13)$$

where R_1 and R_2 are the load resistances and $r_{ox,y}$ is the small signal output resistance of the transistor (where $x = 1$ or 2 and $y = 1$d or 2d).

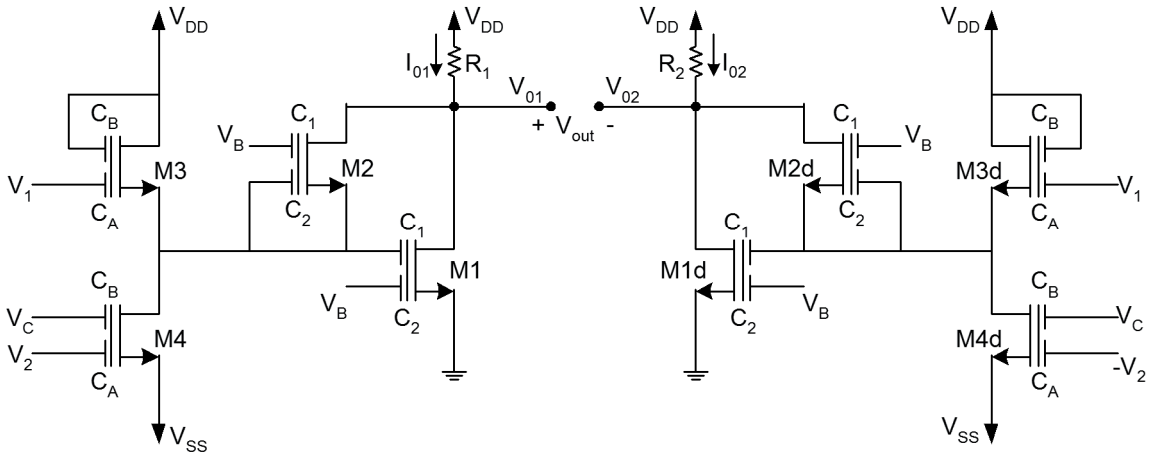

Fig. 5. Proposed four-quadrant multiplier.

The output of the squarer with inputs V_1 and V_2 is given by (assuming $R_1 = R_2 = R$)

$$V_{o1} = V_{DD} - R\frac{\beta}{2}\left\{k_{eq}\left(V_1 - V_2\right)\right\}^2. \quad (14)$$

The output of the squarer with inputs V_1 and $-V_2$ is given by

$$V_{o2} = V_{DD} - R\frac{\beta}{2}\left\{k_{eq}\left(V_1 + V_2\right)\right\}^2. \quad (15)$$

Thus the output of the multiplier using (14) and (15) is given as

$$V_{out} = V_{o1} - V_{o2} = 2\beta R k_{eq}^2 V_1 V_2. \quad (16)$$

It is evident from (16) that the output voltage V_{out} is equal to the four quadrant multiplication of input voltages V_1 and V_2 and the voltage range being determined by the factor k_{eq}. Therefore, the factor k_{eq} should be chosen properly so as to maximize the input range.

4. Second Order Effects

The operation of the multiplier has been analyzed by neglecting the deviations from ideal square-law characteristics due to component mismatch, mobility degradation and temperature dependence. These non-ideal effects are the basic source of discrepancy between the ideal and simulated output voltage of the proposed multiplier.

4.1 Component Mismatch

Assuming that the load resistors of multiplier are R_1, R_2 and the mismatch between these resistors is ΔR_L, the output voltage of the multiplier considering this mismatch is given by

$$V_{out} = R_1\frac{\beta}{2}\left\{k_{eq}\left(V_1 + V_2\right)\right\}^2 - R_2\frac{\beta}{2}\left\{k_{eq}\left(V_1 - V_2\right)\right\}^2. \quad (17)$$

Equation (17) can be simplified as

$$V_{out} = \frac{\beta}{2}k_{eq}^{\ 2}\left\{\Delta R_L\left(V_1^2 + V_2^2\right) + 2V_1V_2(R_1 + R_2)\right\}. \quad (18)$$

It can be seen from (18) that the mismatch in load resistors R_1 and R_2 produces an error voltage proportional to the square of the two input voltages V_1 and V_2.

4.2 Mobility Degradation

Drain current equation including the mobility degradation effect can be modeled as

$$I_{DS} = \frac{1}{2}\left\{\frac{\mu_O}{1 + \theta\left(V_{GS} - V_T\right)}\right\}C_{OX}\left(\frac{W}{L}\right)\left(V_{GS} - V_T\right)^2 \quad (19)$$

where θ is the mobility degradation parameter whose value is 0.1~0.001 V^{-1}. Using Taylor series expansion equation (19) can be rewritten as

$$I_{DS} = \frac{1}{2}K_n\left(\frac{W}{L}\right)\left(V_{GS} - V_T\right)^2 \left\{1 - \theta\left(V_{GS} - V_T\right) + \theta^2\left(V_{GS} - V_T\right)^2 - \theta^3\left(V_{GS} - V_T\right)^3 + \ldots\right\} \quad (20)$$

where $K_n = \mu_o C_{ox}$. Considering mobility degradation effect and using (20) the output voltage of the multiplier can be modeled as

$$V_{out} = R_1 k_{eq}^{\ 2}\beta V_1 V_2 + \varepsilon \quad (21)$$

where the error in output voltage is given by

$$\varepsilon = -\theta\beta R_1 k_{eq}^{\ 2} V_2\left(V_2^2 + 3V_1^2\right). \quad (22)$$

Due to extremely small value of θ the output voltage of the multiplier will be slightly affected by the errors introduced due to mobility degradations.

4.3 Temperature Effect

The output of the proposed multiplier will vary because of the temperature dependence of its gain factor (βR), as can be seen from (16).

The temperature dependence of resistance R for any crystalline metal is given as

$$R_T = R_{ref}\left[1+\alpha\left(T-T_{ref}\right)\right] \tag{23}$$

where R_T is the resistance at any temperature T, R_{ref} is the resistance at reference temperature (usually 20°C but sometimes it is 0°C) and α is the temperature coefficient of resistance.

Assuming $R = 20\ \text{k}\Omega$ at $20°C$, $\alpha = .004$ (copper), from (23) the value of resistance R at $30°C$ is 20.8 kΩ and the percentage increase in resistance is approximately 4 %.

The transconductance parameter β depends upon mobility of carriers; the temperature dependence of the mobility is given as

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{\gamma} \tag{24}$$

where T is the absolute temperature (300 K), T_r is the temperature at which the mobility is to be calculated, and γ is a constant between 1.5 and 2.0. According to (24), for temperature variation of 10°C around room temperature the percentage decrease in mobility is 4.7 % (for $\gamma = 1.5$) and 6.3 % (for $\gamma = 2$).

For 10°C variation in temperature, increase in resistance R is 4 % and decrease in mobility is 4.7 % or 6.3 % for $\gamma = 1.5$ and 2 respectively.

According to (16), the output voltage variations caused due to temperature changes will be cancelled up to some extent. But for wider temperature range gain variations can be compensated to large extent by implementing load resistor using diode connected PMOS transistor. The resistance of diode connected MOS transistor is given by

$$R_{MOS} \propto \left\{\mu_0 C_{ox}\left(V_{GS}-V_T\right)\right\}^{-1}. \tag{25}$$

It can be seen from (25) that for large value of the gate to source voltage the variation in threshold voltage with temperature can be neglected [18]. Above equation shows that for the temperature variation of 10°C around room temperature if decrease in mobility is 4.7 % as discussed above, the variation in resistance R_{MOS} is just inverse and therefore, the variation in output voltage is cancelled out.

5. Simulation Results

The designed circuits are simulated using Cadence Spectre simulator in TSMC 0.18 µm CMOS technology using ±0.75 V power supply. The design parameters of the proposed circuit are given in Tab. 1. The approximate value of V_B (Tab. 1) is chosen by using equation $kV_B = V_T$. The value of threshold voltage V_T has been taken from the TSMC 180 nm CMOS model file specified in Spectre simulator of Cadence and $k = C_1/C_2 = 1/2$. At $V_B = 750$ mV, the threshold voltage is being cancelled out in simulations. By using equation $V_C = (k_A/k_B)V_{SS}$ the value of V_C (Tab. 1) is chosen, where, $k_A/k_B = C_A/C_B = 1/3$ and $V_{SS} = -750$ mV.

Design parameters	Values
Transistor sizes (µm)	M1,M2,M1d,M2d : W=4.4, L=0.18
	M3,M4,M3d,M4d: W=0.54, L=0.18
R_1=R_2 (kΩ)	20
FGMOS capacitances(fF)	C_B= 432, C_A= 144 C_1= C_2= 100
Bias voltages (V)	V_C= -0.25, V_B= 0.75

Tab. 1. Design parameters of the proposed multiplier.

Since the floating gate (FG) of FGMOS does not have any connection to ground, the simulator cannot understand the floating gate and reports dc convergence problem during simulation. To avoid dc convergence error during simulation, model suggested in [10] has been used in this work. This model is based on connecting large value resistors in parallel with the input capacitors as shown in Fig. 6.

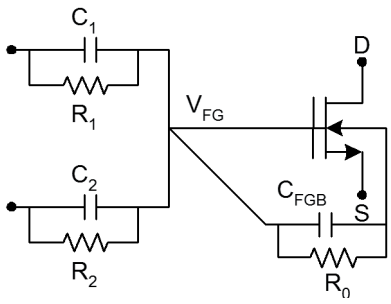

Fig. 6. Simulation model of two input FGMOS.

In this model the relation between resistances and capacitances can be given as follows: $R_i = 1/(kC_i) = 1000$ GΩ.

The DC response of the multiplier is shown in Fig. 7.

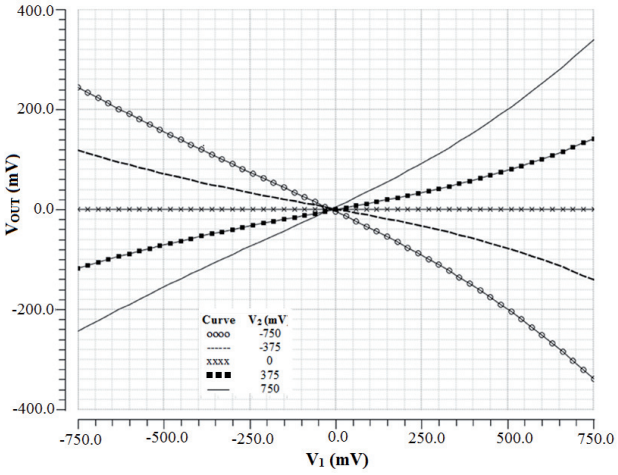

Fig. 7. DC response of the multiplier.

The figure shows that for input varying from -750 mV to 750 mV the output of the multiplier varies linearly up to ±250 mV but significant nonlinearities occur for input

voltages higher than ±250 mV. The proposed multiplier operates at low supply voltage (±0.75 V) with total quiescent power consumption of only 35.28 µW. The linearity error corresponding to $V_1 = 750$ mV and $V_2 = 500$ mV is 4.1 %.

The input and output impedance plots for the proposed multiplier are shown in Fig. 8a and 8b respectively. It is observed from the figures 8a and 8b that the suggested topology has the high input impedance of 192 GΩ and moderate output impedance of 19 kΩ respectively.

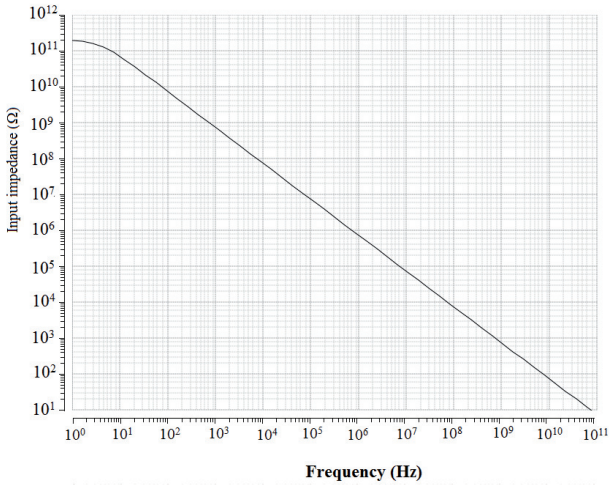

Fig. 8a. Input impedance.

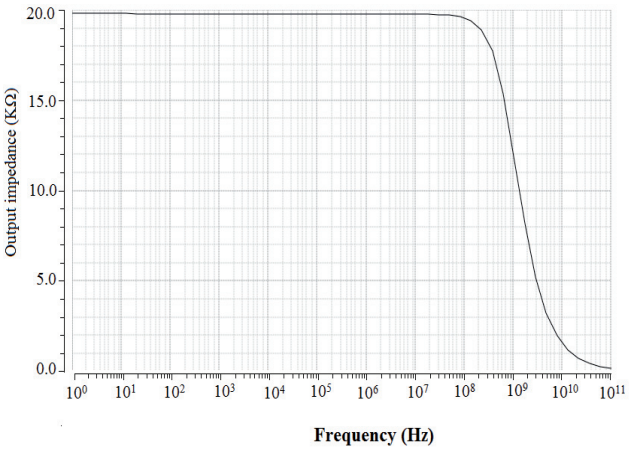

Fig. 8b. Output impedance.

The Total Harmonic Distortion (THD) for the proposed multiplier with V_1 as 1 kHz sinusoid while V_2 as 750 mV is shown in Fig. 9. The maximum THD due to second order effects, such as component mismatch, mobility degradation and temperature variation is about 6.8 %. In the proposed circuit for input voltage up to 90 mV, THD is less than / equal to 1% and the input noise is 457.5 μV_{rms}. Using these values the input dynamic range is found to be 45.8 dB.

The dynamic range of the circuit can be increased by varying both the capacitive coupling ratios and the aspect ratios of the transistors. Fig. 10a shows the DC response of the proposed multiplier for the capacitor values of $C_B = 432$ fF, $C_A = 54$ fF and the corresponding THD plot is shown in Fig. 10b. In the proposed circuit for input voltage up to 130 mV, THD is less than / equal to 1 % and input noise is 389.4 μV_{rms}. Using these values the input dynamic range is found to be 50.4 dB. The dynamic range of the proposed circuit increases at the cost of reduced output voltage range.

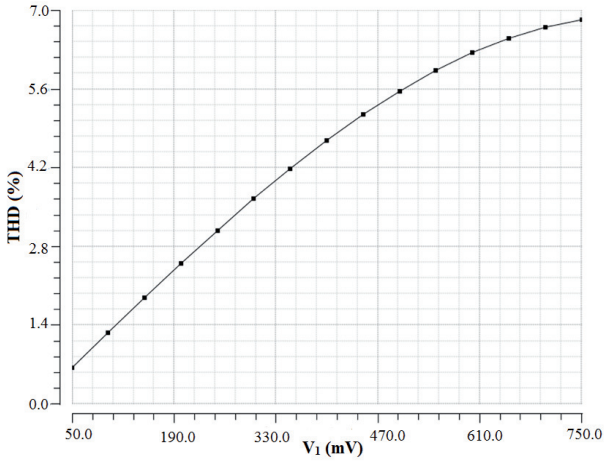

Fig. 9. THD plot.

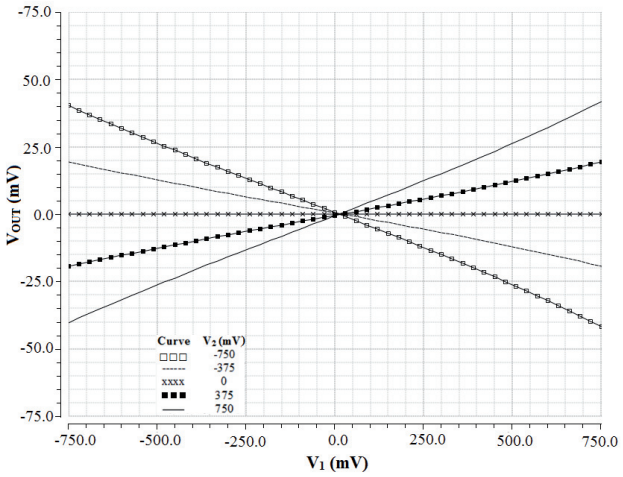

Fig. 10a. DC response of the multiplier for $C_B = 432$ fF and $C_A = 54$ fF.

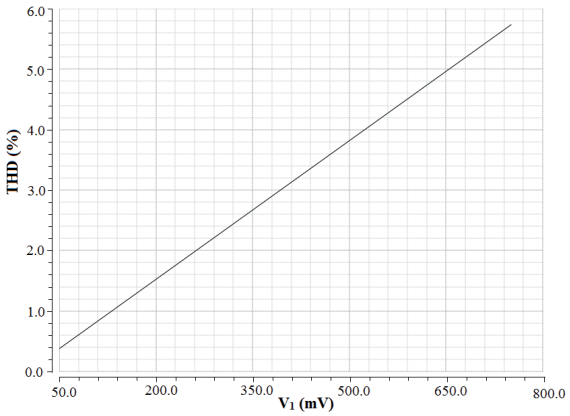

Fig. 10b. Percentage THD for $C_B = 432$ fF and $C_A = 54$ fF.

Fig. 11a shows the DC response of the proposed multiplier for the aspect ratios $(W/L)_1 = (W/L)_2 = (W/L)_{1d} = (W/L)_{2d} = (24\ \mu m / 6\ \mu m)$ and the corresponding THD plot is shown in Fig. 11b. In the proposed circuit for input voltage range up to 170 mV, THD is less than or equal to 1 % and input noise is 484.8 μV_{rms}. Using these values the input dynamic range is found to be 50.8 dB.

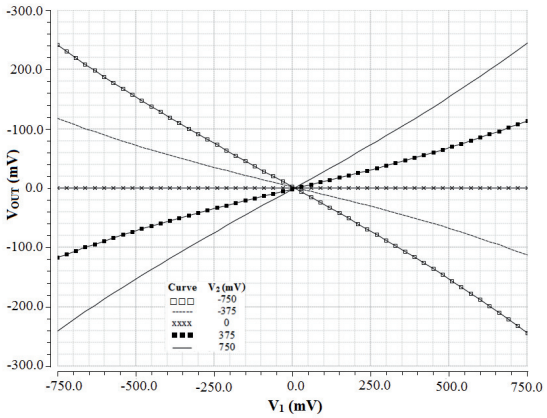

Fig. 11a. DC response of the multiplier for $(W/L)_1 = (W/L)_2 = (W/L)_{1d} = (W/L)_{2d} = (24\ \mu m / 6\ \mu m)$.

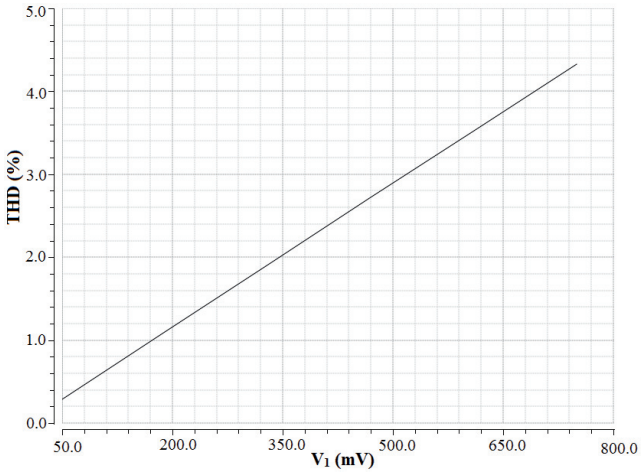

Fig. 11b. Percentage THD for $(W/L)_1 = (W/L)_2 = (W/L)_{1d} = (W/L)_{2d} = (24\ \mu m / 6\ \mu m)$.

The frequency response of the multiplier at different values of temperature is shown in Fig. 12a. It can be seen that as the temperature varies from -50°C to 50°C the gain of the multiplier varies from -25.2 dB to -13.9 dB and the pole frequency varies from 205.6 MHz to 168.9 MHz respectively.

The frequency response of the multiplier with temperature compensated gain is shown in Fig. 12b. For temperature compensation the load resistors R_1, R_2 are replaced by diode connected PMOS transistors with $W = 10.8\ \mu m$ and $L = 0.18\ \mu m$. The frequency response of the temperature compensated multiplier shows that as the temperature varies from -50°C to 50°C the variation of gain is very small (-19.0 to -19.5 dB) and the pole frequency varies from 77.7 MHz to 155.5 MHz respectively.

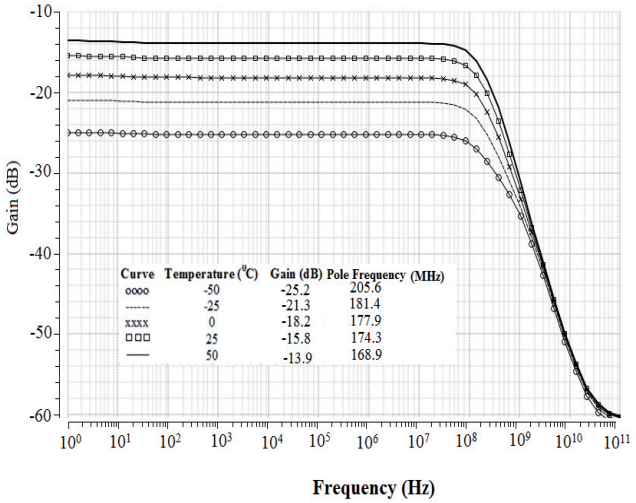

Fig. 12a. Frequency response of the multiplier at different temperatures.

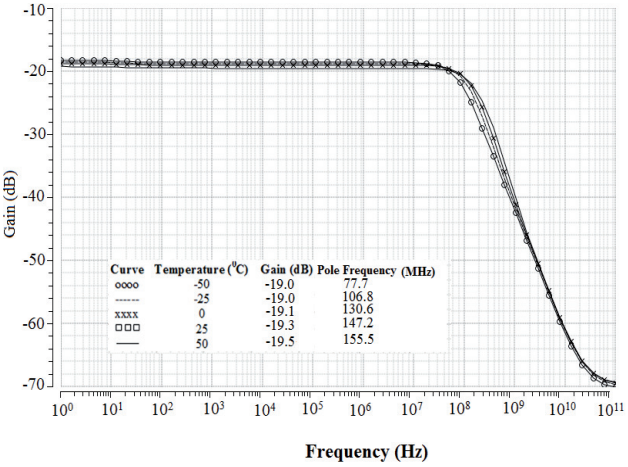

Fig. 12b. Frequency response with temperature compensated gain.

Finally, to demonstrate the effectiveness of the proposed configuration the circuit has been employed as an amplitude modulator, as shown in Fig. 13. The carrier

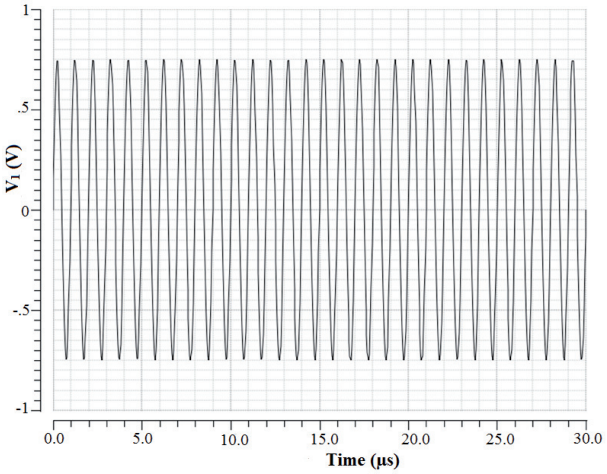

Fig. 13a. Carrier input signal V_1.

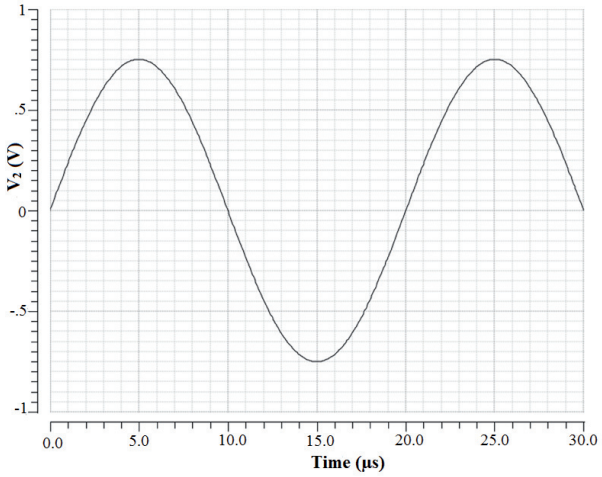

Fig. 13b. Modulating input signal V_2.

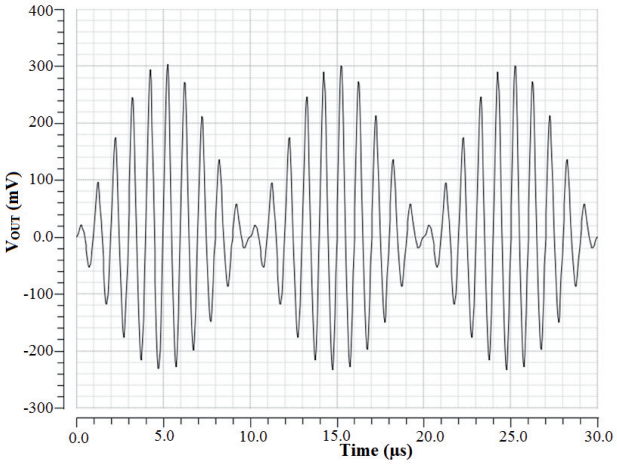

Fig. 13c. Output of the amplitude modulator.

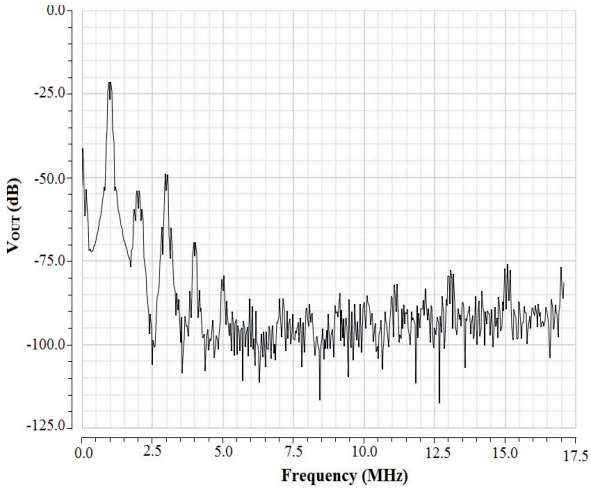

Fig. 13d. Spectrum of the output of the amplitude modulator.

input V_1 with frequency 1 MHz, amplitude 750 mV and the modulating input V_2 with frequency 50 kHz, amplitude 750 mV are shown in Fig. 13a and 13b respectively. The modulated output waveform is shown in Fig. 13c and its spectrum is shown in Fig. 13d. From Fig. 13d it can be seen that the maximum distortion peak is 20 dB below the desired modulation

Tab. 2 compares the performance parameters of the proposed circuit with various commercially available multipliers (AD633, AD734, AD835) and the multipliers based on CMOS/BJT/FGMOS technology.

It is observed that among all the multipliers mentioned in Tab. 2, the proposed configuration has the highest input impedance of 192 GΩ which makes the signal source loading effect negligible in the circuit. Apart from this, the

Parameters	AD633	AD734	AD835	[22]	[23]	[27]	[28]	[29]	Proposed
Technology (µm)	NA	NA	NA	0.35	1	2	0.8	0.35	0.18
Maximum Supply Voltage (V)	±18	±16.5	±5.5	1.5	±1.5	±2.5	±1	2	±0.75
Input range	±10 V	±12.5 V	±1 V	±60 mV	±0.8 V	100 % of supply voltage	100 % of supply voltage	100 % of supply voltage	100 % of supply voltage
Linearity error (%)	±1 (X=±10 V) (Y =+10 V)	0.05 (X=±10 V) (Y =+10 V)	0.5 (X=±1V, Y=1V)	< 3.2 (for input range ±60 mV)	< 2 (for input range ±0.8 V)	< 0.5 (for input range ±2.5 V)	NA	0.0081	4.1 (V_1=750mV, V_2=500 mV)
No. of Components	NA	NA	NA	8 PMOS, 2 Resistors, 4 Biasing current sources	8 NMOS, 4 BJT, 2 Resistors	9 FGMOS, 2 Resistors, 3 biasing current sources	4 FGMOS, 2 MOS, 1 OTA	6 FGMOS, 6 MOS, 3 biasing current sources	8 FGMOS, 2 Resistors
Power consumption	NA	NA	NA	6.7 µW (Maximum)	50 µW (Static)	NA	Large power consumption	NA	35.28 µW (Static)
Input resistance	10 MΩ	50 kΩ	60 kΩ	NA	NA	NA	NA	NA	192 GΩ
Output resistance	NA	NA	NA	NA	NA	NA	NA	NA	19 kΩ
Bandwidth (MHz)	1	10	250	0.26	10	NA	NA	1400	173
THD (%)	NA	NA	NA	4.2	NA	NA	1.4	2.6	6.8

Tab. 2. Comparison of various conventional and proposed multipliers.

proposed multiplier has the simplest structure, operates at the lowest supply voltage of ±0.75 V and has low quiescent power consumption of 35.28 µW at the cost of low linearity.

The layout of the proposed multiplier is shown in Fig. 14 and the associated layout-level simulations are given in Figs. 15–17. Fig. 14 shows that the designed multiplier occupies an area of 69.9 × 26.4 µm^2. All the DC responses (Fig. 15a, 16a, 17a) have been obtained by varying V_1 from -750 mV to 750 mV and V_2 = -750 mV.

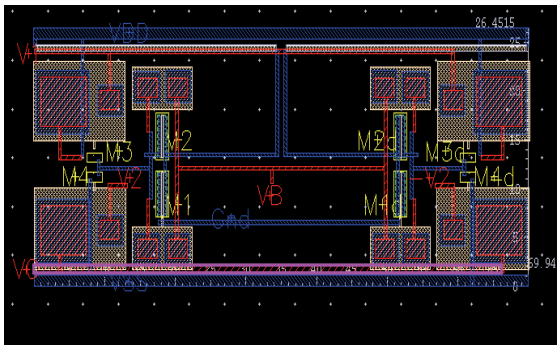

Fig. 14. Layout of the proposed multiplier.

The proposed multiplier is based on only NMOS transistors; therefore it has three process corners i.e. Typical (T), Fast (F) and Slow (S). The simulated DC and AC responses of the proposed circuit (Fig. 5) at different process corners are shown in Figs. 15a and 15b respectively. Fig. 15a shows that at V_1 = -750 mV and V_2 =-750 mV the output voltages are 243.9 mV, 399.5 mV and 152 mV for the process corners T, F and S respectively. Similarly, at V_1 = 750 mV and V_2 = -750 mV the output voltages are -334 mV, -419 mV and -138 mV at process corners T, F and S respectively. The AC response (Fig. 15b) shows that at process corners T, F and S the gain varies from -15.6 dB to -4.9 dB and the corresponding pole frequency varies from 173.3 MHz to 282.4 MHz.

The simulated DC and AC responses of the proposed circuit (Fig. 5) while considering the mismatch between the load resistances are shown in Figs. 16a and 16b respectively. The DC response (Fig. 16a) shows that as one of the load resistances varies from 18 kΩ to 22 kΩ (keeping other load resistance constant at 20 kΩ); the output voltage of the multiplier varies from -362 mV to -300 mV respectively. The frequency response (Fig. 16b) shows that as one of the load resistance varies from 18 kΩ to 22 kΩ the gain of the multiplier varies from -16.25 dB to -14.9 dB and the pole frequency varies from 163 MHz to 173 MHz respectively.

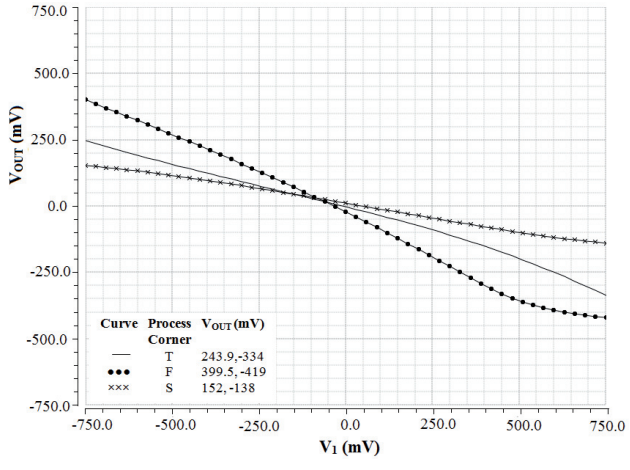

Fig. 15a. DC response at different process corners.

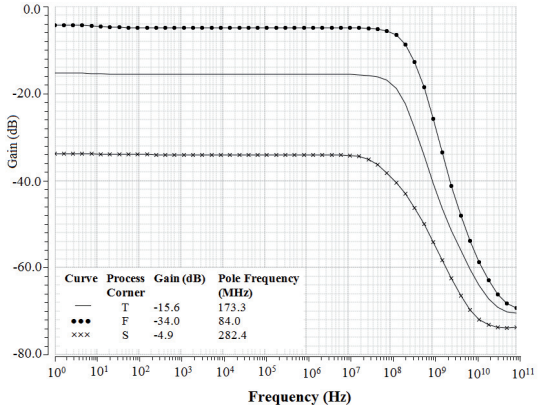

Fig. 15b. Frequency response at different process corners.

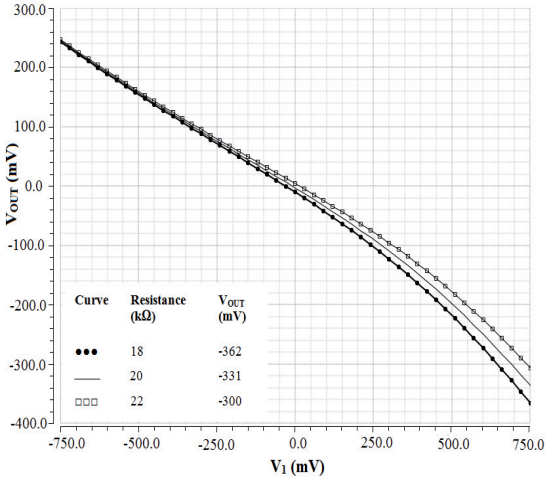

Fig. 16a. DC response at different values of load resistance.

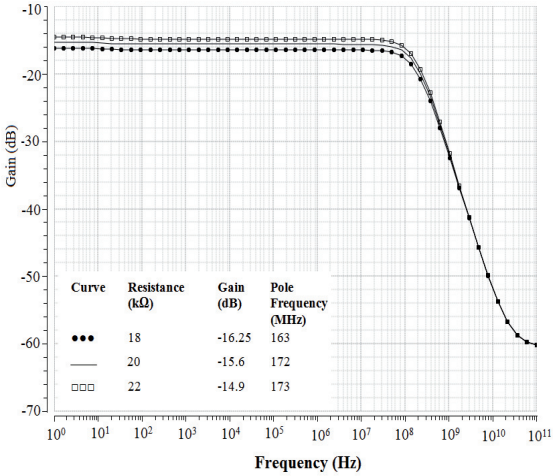

Fig. 16b. Frequency response at different values of load resistance.

The simulated DC and AC responses of the proposed circuit at different temperatures are shown in Figs. 17a and 17b respectively. The DC response (Fig. 17a) shows that as the temperature varies from -50°C to 50°C the output voltage of the multiplier varies from 109 mV to 277 mV for V_1 = -750 mV and V_2 = -750 mV. Similarly, as the temperature varies from -50°C to 50°C the output voltage of the multiplier varies from -113 mV to -395 mV for V_1 = 750 mV and V_2 = -750 mV. The frequency response (Fig. 17b) shows that as the temperature varies from -50°C to 50°C the gain of the multiplier varies from -27.4 dB to -13.4 dB and the pole frequency varies from 155.2 MHz to 125.8 MHz respectively.

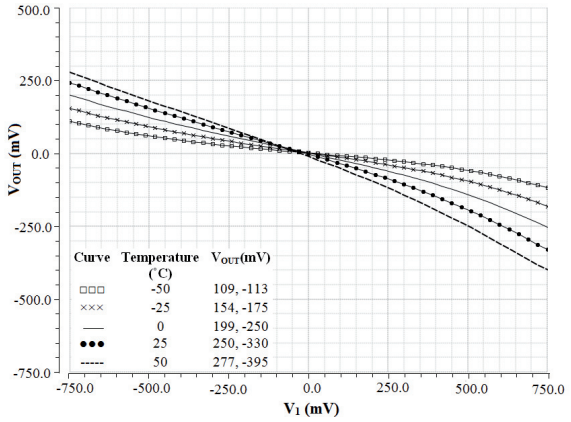

Fig. 17a. DC response at different temperatures.

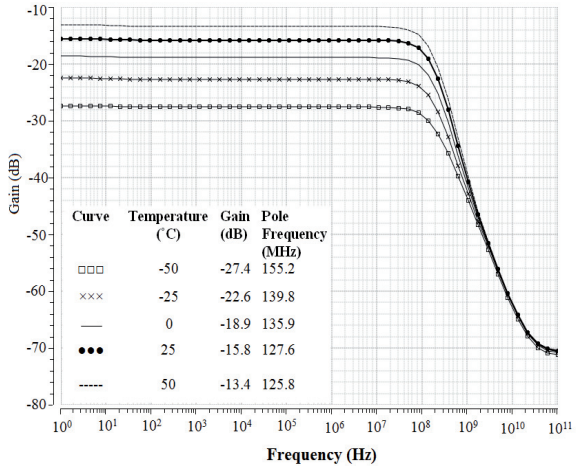

Fig. 17b. Frequency response at different temperatures.

6. Conclusions

In this paper, a simple FGMOS transistor based four-quadrant multiplier has been proposed. First the sum and difference of the input voltages are squared and then their difference is taken so as to generate the four quadrant multiplier function. The proposed circuit operates at ±0.75 V with quiescent power consumption of only 35.28 µW and the bandwidth of approximately 173 MHz. Thus the newly developed four-quadrant multiplier is one of the best choices for low voltage/low power analog signal processing applications.

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