# Multi-Core DSP Based Parallel Architecture for FMCW SAR Real-Time Imaging

*Chengfei GU* [1], *Wenge CHANG* [1], *Xiangyang LI* [1], *Zhaohe LIU* [2]

[1] College of Electronic Science and Engineering, National University of Defense Technology, Deya Street 109, Changsha, P. R. China
[2] Science and Technology on Near-Surface Detection Laboratory, West Tonghui Road 160, Wuxi, P. R. China

hafeigu_2006@126.com, changwenge@nudt.edu.cn, lxyniu@sina.com, Lzhh@vip.sina.com

**Abstract.** *This paper presents an efficient parallel processing architecture using multi-core Digital Signal Processor (DSP) to improve the capability of real-time imaging for Frequency Modulated Continuous Wave Synthetic Aperture Radar (FMCW SAR). With the application of the proposed processing architecture, the imaging algorithm is modularized, and each module is efficiently realized by the proposed processing architecture. In each module, the data processing of different cores is executed in parallel, also the data transmission and data processing of each core are synchronously carried out, so that the processing time for SAR imaging is reduced significantly. Specifically, the time of corner turning operation, which is very time-consuming, is ignored under computationally intensive case. The proposed parallel architecture is applied to a compact Ku-band FMCW SAR prototype to achieve real-time imageries with 34 cm × 51 cm (range × azimuth) resolution.*

## Keywords

Parallel processing, multi-core DSP, real-time imaging, FMCW SAR

## 1. Introduction

Frequency Modulated Continuous Wave Synthetic Aperture Radar (FMCW SAR) has made significant advancement in the last decade [1]–[2]. Benefiting from low-mass, low-power and low-cost, it is widely applied in different remote sensing fields, whereas one of the main challenges of FMCW SAR is the realization of real-time imaging. In the past decades, kinds of SAR imaging algorithms aiming high quality imagery have been proposed. All these algorithms are classified as frequency-domain algorithms and time-domain algorithms. Undoubtedly, the latter one is not a good choice for real-time processing. The popular frequency-domain SAR algorithms, specifically, include Range-Doppler Algorithm (RDA), Chirp-Scaling Algorithm (CSA), Nolinear Chirp-Scaling Algorithm (NCSA), Range Migration Algorithm (RMA) and Frequency-Scaling Algorithm (FSA) [1]–[4]. In this paper, the extended FSA [2]–[3], which also contains two-order space-variant motion compensation and autofocus processing, is selected to verify the feasibility of the proposed parallel processing strategy.

Up to now, the simplified algorithm and multi-processor board have been applied to realize the real-time processing of SAR system. However, using simplified algorithm will drastically reduce the image quality, and using multiple processors will occupy too much valuable load and space resources of FMCW SAR. For the resolution comparison, the work in [5]–[6] demonstrates a recently developed real-time imaging FMCW SAR system (named MIRANDA35) from Fraunhofer Institute for High Frequency Physics and Radar Techniques (FHR) in 2014. In order to reduce computation, MIRANDA35 has applied with the RD algorithm and lookup table leading to a real-time resolution of 2 m. For the time-consumption comparison, the work in [7] has simply evaluated the multi-core Digital Signal Processor's (DSP's) capability for SAR signal processing, but the corner turning is still an independent process which can not be fully optimized.

For the realization of miniature light, low power consumption and high-resolution real-time FMCW SAR system, only an eight-core DSP named TMS320C6678 is used in this paper. Owing to multi-core DSP's compact structure and high performance, it would be widely used in light-weight and real-time SAR system in near future. In this paper, we proposed an efficient multi-core DSP based parallel processing structure, which is propitious to realize the real-time imaging of FMCW SAR with high resolution. The proposed architecture could be applied in the realizations of all kinds of frequency-domain SAR imaging algorithms. With the application of this processing structure, the extended FSA is realized in a modular manner in this paper, and each module of the algorithm uses the same architecture. In each module, the data processing of different cores is executed in parallel, also the data transmission and data processing of each core are synchronously carried out, so that the processing time and corner turning time are considerably reduced. For computationally intensive case, not only the data is processed in parallel, but also the corner turning time is fully released. Furthermore, in order to validate the performance of real-time imaging, several airborne experiments

have been successfully performed. At the end of this paper, a 34 cm × 51 cm (range × azimuth) resolution SAR image of real-time processing is presented and analyzed.

The remainder of this paper is organized as follows. Section 2 reviews the imaging process of FMCW SAR, and the approach to modularization of the extend FSA is addressed. In Section 3, an efficient architecture for real-time processing is proposed, also the realization of the extend FSA is introduced in detail. Section 4 shows the results of real-time processing, also the qualities of imagery is analyzed specifically. Finally, Section 5 gives the conclusion of this paper.

# 2. Imaging Algorithm and its Modularizing

## 2.1 General FMCW SAR Imaging Model

As previously mentioned, FMCW SAR has the characteristics of compact structure and light weight. Consequently, the airborne based SAR imaging, which devotes to evaluate the performance of SAR system, can be facilely performed [11]–[12]. Without loss of generality, the imaging geometry of airborne test is shown in Fig. 1.

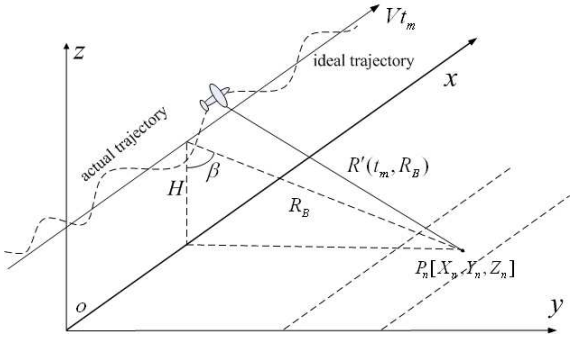



**Fig. 1.** Imaging geometry of airborne test.

In Fig. 1, the solid line and dashed curve stand for the ideal and actual trajectories, respectively. The aircraft moves along track in the direction of $Vt_m$, where $V$ is the velocity along the motion trail and $t_m$ stands for the slow time. Furthermore, $\beta$ and $H$ denote the pitching angle and height of platform, respectively. $R_B$ and $R'(t_m, R_B)$ stand for the closet range and the instantaneous range of point scatter $P_n$. The transmitted linear frequency modulated signal is assumed to be [1]–[2]

$$s_i(\hat{t}, t_m) = \text{rect}\left(\frac{\hat{t}}{T_p}\right) \cdot \exp\left[j2\pi(f_c t + \frac{1}{2}\gamma \hat{t}^2)\right], \quad (1)$$

where $\hat{t}$ is the fast time (also called the range time variable), $\text{rect}\left(\frac{\hat{t}}{T_p}\right)$ is the rectangular function with the duration $T_p$, which denotes the signal time width. $f_c$ and $\gamma$ stand for the carrier frequency and the chirp rate of transmitted signal, respectively. The variable $t$ is the summation of $\hat{t}$ and $t_m$. The deramped signal is [2]–[4]

$$\begin{aligned} s_{if}(\hat{t}, t_m) &= s_r(\hat{t}, t_m) \cdot {s_{ref}}^*(\hat{t}, t_m) \\ &= A \cdot \text{rect}\left(\frac{\hat{t} - 2R'/c}{T_p}\right) \cdot \exp\left(-j\frac{4\pi f_c}{c} R_\Delta\right) \\ &\cdot \exp\left[-j\frac{4\pi\gamma}{c}\left(\hat{t} - \frac{2R_{ref}}{c}\right) R_\Delta\right] \exp\left(j4\pi\gamma \frac{{R_\Delta}^2}{c^2}\right), \end{aligned} \quad (2)$$

in which, $R'$ is $R'(t_m, R_B)$ in Fig. 1 and $R' = \sqrt{R_B^2 + V^2 \cdot (\hat{t} + t_m)^2}$, $R_{ref}$ is the reference range, $c$ is the velocity of light, $A$ is the amplitude of the deramped signal. $s_r$ and $s_{ref}$ stand for the received signal and the reference signal, respectively. $R_\Delta$ denotes the difference between the instantaneous range and the reference range. In order to reduce the required sampling rate, the transmitted and received signals are generally mixed, which also called dechirp-on-receive [1]. Consequently, the intermediate frequency in (2) is simplified as

$$\begin{aligned} s_{if}(\hat{t}, t_m) =& A \cdot \text{rect}\left(\frac{\hat{t} - 2R'/c}{T_p}\right) \cdot \exp\left(-j\frac{4\pi f_c}{c} R'\right) \\ &\cdot \exp\left[-j\frac{4\pi\gamma\hat{t}}{c} R'\right] \cdot \exp\left(j4\pi\gamma \frac{R'^2}{c^2}\right). \end{aligned} \quad (3)$$

Using the Taylor approximation, the instantaneous range is simplified as

$$\begin{aligned} R'(\hat{t} + t_m) &\approx \sqrt{R_B^2 + V^2 \cdot {t_m}^2} + \frac{V^2 t_m}{\sqrt{R_B^2 + V^2 \cdot {t_m}^2}} \hat{t} \\ &= R(t_m) + \frac{\lambda}{2}\left(\frac{2V}{\lambda} \cdot \frac{V t_m}{R(t_m)}\right)\hat{t} \\ &= R(t_m) + \frac{\lambda}{2} f_d \hat{t}, \end{aligned} \quad (4)$$

where $\lambda$ is the wavelength, $R(t_m) = \sqrt{R_B^2 + V^2 \cdot t_m^2}$ is the azimuth-dependent distance to the point target, while $f_d$ denotes the Doppler frequency in azimuth, which is also expressed as [2]–[3]

$$f_d = \frac{2V}{\lambda} \cdot \frac{V t_m}{\sqrt{R_B^2 + V^2 \cdot t_m^2}} = \frac{2V}{\lambda} \cdot \sin\theta_m, \quad (5)$$

in which $\theta_m$ stands for the instantaneous aspect angle [2]. Substituting (4) and (5) into (3) yields

$$\begin{aligned} s_{if}(\hat{t}, t_m) &= A \cdot \text{rect}\left(\frac{\hat{t} - 2R'/c}{T_p}\right) \cdot \exp\left(-j\frac{4\pi}{\lambda} R(t_m)\right) \\ &\cdot \exp\left(-j2\pi f_d \hat{t}\right) \exp\left(-j\frac{4\pi\gamma\hat{t}}{c} R'\right) \exp\left(j4\pi\gamma \frac{R'^2}{c^2}\right), \end{aligned} \quad (6)$$

where the first exponential term represents the Doppler modulation in azimuth. The second exponential term, which brings a new range migration, is introduced by the antenna movement within a sweep. The third one represents the range signal and the last exponential term is the Residual Video Phase (RVP), which is essential for FSA [1]–[3].

## 2.2 Modularization of the Extended FSA

According to the frequency-domain algorithms, RDA is not suitable for high resolution and wide swath width SAR

imaging, and CSA is based on the linear frequency modulation signal, which is not feasible for deramped signal of FMCW SAR. RMA needs to execute time-consuming interpolation, which is not suitable for real-time processing. Consequently, in this paper, the extended FSA is selected as the real-time processing algorithm.

It is generally known that SAR imaging is a two-dimensional processing, i.e. the received data is processed both in range and azimuth direction. However, the SAR raw data is digitally recorded in range which means the data is separated in cross-range. Moreover, the processor favors the data with contiguous memory in burst access way [8]. Therefore, the data should be realigned into adjacent addresses before the azimuth processing. Furthermore, during the range dimension processing, e.g., the compensation factor is space-variant in azimuth, the data matrix must be processed completely before the azimuth dimension processing. Consequently, from a perspective of the real-time processing, it is recommended that the data should be processed in the same dimension. Based on the analysis above, the imaging algorithm is modularized in processing dimension way, and corner turning operation has been done after the processing of one dimension. The modularized processing flow of the extended FSA is shown in Fig. 2 [2].

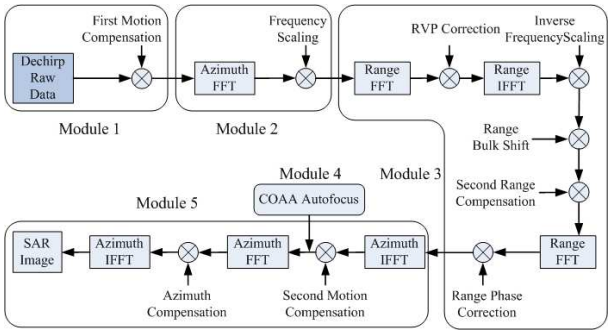



**Fig. 2.** Processing flow of FSA and its modularization.

As shown in Fig. 2, the extended FSA is divided into five serial modules, and in each module three-step operations are comprised, i.e. Data-getting, Data-processing and Data-storing, respectively. Module 1 and module 3 process the range data, and the azimuth data is processed by module 2 and module 5. Module 4 carries out the time-consumption autofocus. Each module is effectively serially processed by the same parallel processing architecture mentioned below.

# 3. Parallel Processing Architecture

## 3.1 Parallel Processing of Imaging Module

Considering of the finite board load and rigid time requirement, only an eight-core DSP TMS320C6678 chip is mounted on a FMCW SAR processing board as the real-time processing kernel. It has excellent performance of 320 GMACS for fixed point and 160 GFLOPS for floating point [8]. To process SAR data in a specified period, the data

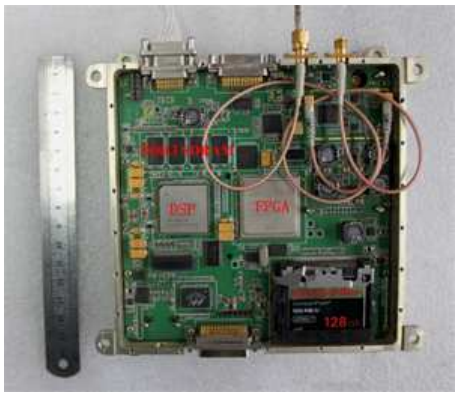



**Fig. 3.** The FMCW SAR processing board.

undergoes parallel processing on a compact processing board shown in Fig. 3.

As shown in Fig. 3, the size of FMCW SAR processing board is about 14 cm × 14 cm with an eight-core DSP chip (TMS320C6678), also four 256 MB Double Date Rate3 Synchronous Dynamic Random Access Memory (DDR3 SDRAM) chips are used as buffer memory during the real-time processing. It is known that, corner turning (matrix transposition) is a key step in SAR data processing, also a bottleneck of real-time SAR imaging. Thus improving the efficiency of corner turning is of great value for the real-time processing. TMS320C6678 uses Enhanced Direct Memory Access 3 (EDMA3) module to transfer data efficiently. It supports two addressing modes, which are constant addressing and increment addressing, respectively [8]–[9]. In the following parallel processing frame, EDMA3 constant addressing is used to fetch the data to be processed, and EDMA3 increment addressing is used to realize the corner turning. Based on the characteristics of the serial modularized algorithm and EDMA3 corner turning operation, we divide the pending-processing data into eight parts to realize the parallel mapping of each module in Fig. 2. The efficient parallel processing architecture is presented in Fig. 4.

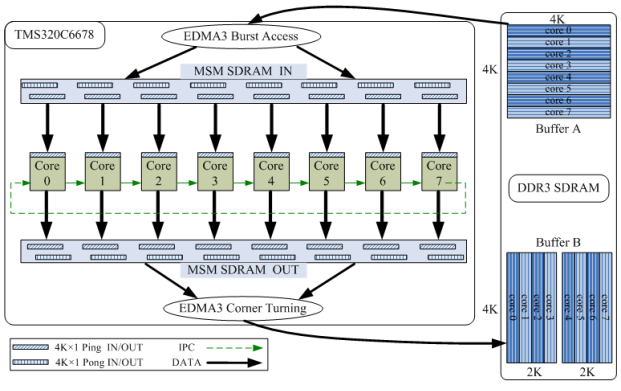



**Fig. 4.** Block diagram of parallel processing.

In this two-part parallel processing architecture, eight-core DSP is the processing unit, and DDR3 SDRAM buffers high-volume data. Buffer A in DDR3 SDRAM is used to house the pending-processing data, and Buffer B stores the processed and transposed data. In Fig. 4, the data size of

Buffer A is 4096 × 4096 (row × column) with the format of single-precision float-point leading to a data volume of 128 MB. The pending-processing data in Buffer A is equally divided into eight parts corresponding to eight cores of DSP chip. The size of each part is 0.5 K × 4 K, and each one is processed by a corresponding core. As mentioned in [10], the speed of EDMA3 corner turning increases with the decrease of Buffer B's column number. However, fewer columns lead more sub-matrixes to store the processed data, which will increase processing complexity of the next module. After comprehensive consideration, Buffer B is divided into two 4 K × 2 K sub-matrixes to store the processed data in EDMA3 corner turning way which tested speed is 478 MBps based on processor in Fig. 3 [10]. In Buffer B, the first sub-matrix stores the processed and transposed data of former four cores, and the data of the latter four cores is stored in the second sub-matrix.

As shown in Fig. 4, to realize efficient PingPong processing, each core is equipped with four 32 KB PingPong IN/OUT buffers in the Multicore Shared Memory (MSM) SDRAM. The data in PingPong IN buffers is fetched from Buffer A in EDMA3 burst access way with a rapid throughput of 5 GBps [10], and the processed data in PingPong OUT buffers is stored into Buffer B in EDMA3 corner turning way. The PingPong processing flow of a single core is shown in Fig. 5.

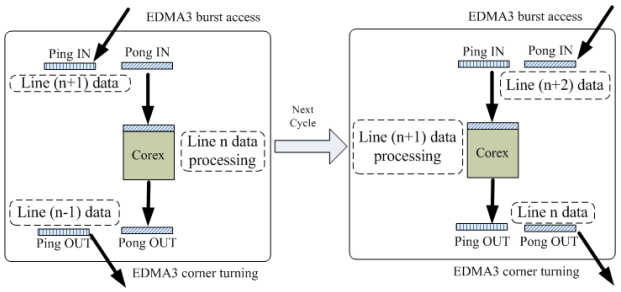



**Fig. 5.** Single core PingPong processing flow.

As shown in Fig. 5, the left half is the processing of Pong data, and the right half is the processing of Ping data. Before the Pong data processing, DSP core triggers the corner turning operation of the processed line $(n-1)$ data in Ping OUT buffer and the burst access operation of line $(n+1)$ data in Buffer A. After the triggers of data transmission, EDMA3 module transposes the processed line $(n-1)$ data from Ping OUT buffer to Buffer B, and transfers line $(n+1)$ data from Buffer A to Ping IN buffer. In the meantime, DSP core processes line $n$ data in Pong IN buffer, and the result is cached into Pong OUT buffer. The next cycle is the processing of Ping data, while the corner turning of the processed line $n$ data and the burst access of line $(n+2)$ data, DSP core processes the line $(n+1)$ data synchronously. Each core in Fig. 4 executes the PingPong operation shown in Fig. 5, and with the PingPong processing, the data transmission time in total time consumption is greatly reduced.

In order to avoid the bus conflict between the cores, the done signal of the former core's corner turning is used to trigger the next core's corner turning. And the done signal is defined as Inter-Processor Communication (IPC) in Fig. 4. On the whole, with the application of the proposed parallel processing architecture, not only the data processing of different cores is executed in parallel, but also the data transmission and data processing of each core are synchronously carried out for maximum time reduction.

## 3.2 Time Sequence of Parallel Processing

To have a better insight of the parallel processing architecture, the time-sequence diagrams of single core processing and N cores parallel processing are shown in Fig. 6 and Fig. 7, respectively.

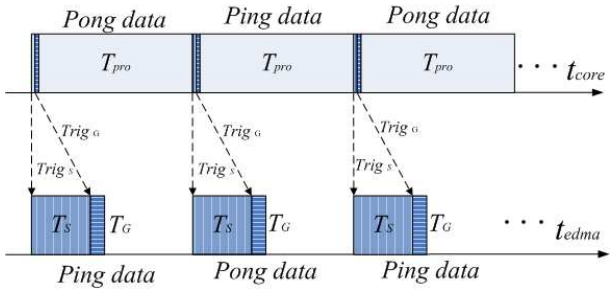



**Fig. 6.** Time sequence of single core processing.

where $T_{\text{Pro}}$ is the processing time of single line data, $T_G$ is the time of getting a line of pending processing data, $T_S$ is the time of storing a line of processed data in corner turning way. The time axis $t_{\text{core}}$ and $t_{\text{edma}}$ work synchronously. As depicted in Fig. 6, the Ping data transmission and Pong data processing are simultaneously proceed after the trigger of the Data-storing and Data-getting. The longer one of transmission time and processing time turns to be the total time consumption. The time sequence of N cores parallel processing is presented in Fig. 7.

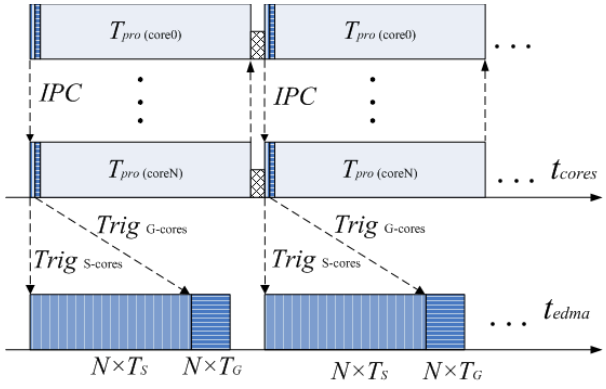



**Fig. 7.** Time sequence of N cores parallel processing.

Theoretically speaking, if $T_{\text{Pro}}$ is larger than $N$ times of data transmission time $N(T_G + T_S)$, the module time-consumption is $1/N$ of the total processing time. Otherwise, the module time-consumption is close to the total transmission time

$$T_N = \begin{cases} T_{\text{Pro}} \cdot N_a / N & T_{\text{Pro}} > N\,(T_G + T_S) \\ N_a\,(T_G + T_S) & T_{\text{Pro}} \le N\,(T_G + T_S), \end{cases} \tag{7}$$

where $N$ and $N_a$ present the number of processing core and the sample number in azimuth, respectively. $T_N$ denotes the module time under $N$ cores parallel processing. This characteristic is in favor of the sophisticated SAR algorithm, which pursues higher resolution imagery.

### 3.3 Time Consumption

To validate the proposed parallel architecture, the time-consumption under different condition is adequately tested on the FMCW SAR processing board shown in Fig. 3. The tested data size and data volume are $4096 \times 4096$ (range $\times$ azimuth) and 128 MB, respectively. As mentioned in [10], $T_G$ and $T_S$ of a 32 KB continuous data are 6.5 $\mu$s (microsecond) and 65.7 $\mu$s, respectively. Thus the total transmission time turns to be 0.296 s (second), which denotes the base line in Fig. 8.

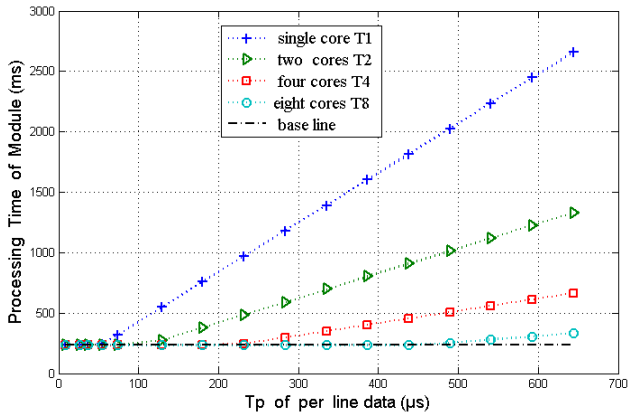



**Fig. 8.** Time consumption of parallel model.

In Fig. 8, $T_1$, $T_2$, $T_4$, $T_8$ denote the time consumption of single core, two cores, four cores and eight cores processing, respectively. As shown in Fig. 8, the time variation of processing module increases with the improvement of processing complexity. For $N$ cores parallel processing, if $T_{Pro}$ is larger than $N(T_G + T_S)$, the integral time-consumption is compressed as $(T_{\text{Pro}} \cdot N_a)/N$. Otherwise, the total time turns to be $(T_G + T_S) \cdot N_a$. The test result in Fig. 8 is commendably in keeping with (7). For comparison, the corner turning operation in [7] is a separate process, and each operation costs 100 ms with image size 4 K by 4 K. Four times of corner turning operations in the extended FSA will cost 400 ms in the real-time processing. The proposed processing architecture makes full use of the characteristic of EDMA [9]. Under computationally intensive case, the time-consumption of the corner turning operation is totally eliminated. However, even if $T_{\text{Pro}}$ is less than $N(T_G + T_S)$, we still could perform other operation (e.g. preprocessing, data compression) during the corner turning to increase the efficiency of the proposed architecture. In a word, with the application of the proposed parallel processing strategy, the data processing time is linearly reduced. Most importantly, the Data-getting time and corner turning time are totally ignored under computationally intensive case.

## 4. Experimental Validation

### 4.1 Real-Time Imaging for Airborne SAR

The airborne test has been performed with a compact FMCW SAR system. As shown in Fig. 9, this compact FMCW SAR system is mounted on a light airplane.

**Fig. 9.** Photograph of the airborne platform and the sensor.

| Parameter | Value | Unit |
|---|---|---|
| Signal Bandwidth | 600 | MHz |
| Swath Width | 800 | m |
| Center Slant Range | 1000 | m |
| Pulse Repetition Frequency | 1000 | Hz |
| Airplane Velocity | 40.2 | m/s |
| Real-time Limit | 3.072 | s |

**Tab. 1.** Summary of the main parameters.

The main parameters of airborne real-time imaging are listed in Tab. 1. The sample number of the data matrix in azimuth is 4096 with a Pulse Repetition Frequency (PRF) of 1000 Hz, so the recording time yields to be 4.096 s. To guarantee an entirely focused image, 25% overlapped data in azimuth is processed. Hence, the limitation of real-time processing turns to be 3.072 s.

As shown in Fig. 2, the entire real-time processing flow is divided into five serial modules. Module 1 only has first order motion compensation, and module 2 just contains FFT in azimuth and Frequency-Scaling operation. Module 3 and module 5 need FFT/IFFT and the compensation of space-variant factors many times. Module 4 is the time-consuming autofocus processing. In order to ensure processing precision, no lookup table is used. To illustrate the efficiency of the parallel strategy, the time-consumption of each module in single-core and eight-core case are listed in Table 2.

| Module | $T_1$ (s) | $T_8$ (s) |
|---|---|---|
| 1 | 0.556 | 0.301 |
| 2 | 0.873 | 0.307 |
| 3 | 2.140 | 0.317 |
| 4 | 4.635 | 0.774 |
| 5 | 3.195 | 0.479 |

**Tab. 2.** Time consumption summary of FS imaging modules.

As shown in Tab. 2, the time of module 1 and 2 have been compressed into the base time in Fig. 8. Module 3, 4 and 5 represent the computationally intensive task, and their eight-core processing results ($T_8$) have been largely reduced compared to the single-core results ($T_1$), e.g., the module 5 gains a speed-up ratio of 6.67. Considering the inter-cores synchronization and communication, this value denotes high efficiency of parallel processing. The processing time of the extended FS algorithm is significantly reduced from 11.399 s to 2.178 s, and the compressed result fully meets the real-time requirement.

## 4.2 SAR Imagery of Real-time Processing

Using the proposed parallel processing strategy, a real-time image of an island area overlaid onto an optical photograph is shown in Fig. 10.

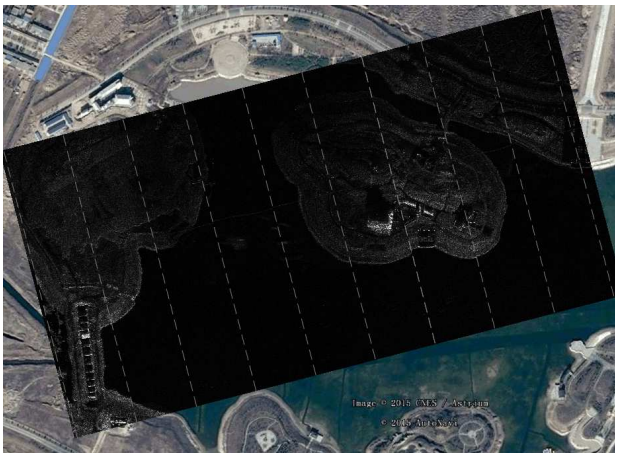


**Fig. 10.** The real-time image overlaid onto an optical photo.

In Fig. 10, the SAR imagery covers areas of 650 m × 1000 m (range × azimuth) island and the central slant range is about 1 km. The corresponding optical photograph is provided by Google Earth. The sub-image between the adjacent dashed line is a frame image of the real-time processing, and the integrated time of each sub-image is 3.072 s.

It can be seen that, the real-time processing experiment gains well results with perfect alignments of the imaging scene. Moreover, the characteristic targets, such as the roads and the buildings, are well focused. Based on the imagery above, we draw a conclusion that the efficiency of the improved approach for the real-time processing is proved.

## 4.3 Performance Analysis of Corner Reflectors

To evaluate the performance of real-time processed image, several corner reflectors are specifically scattered on an airport. The real-time imagery with the corner reflectors is shown in Fig. 11.

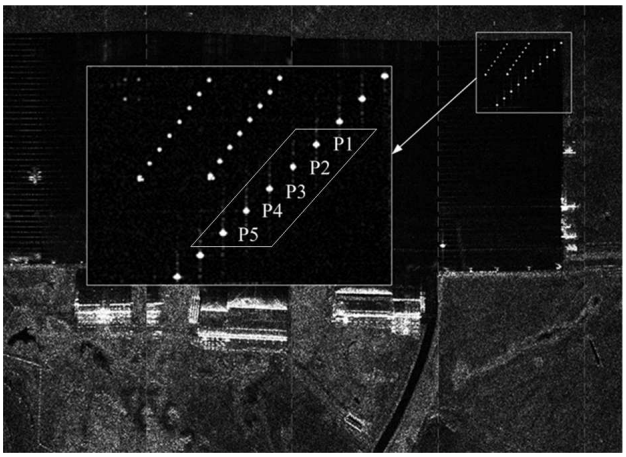



**Fig. 11.** Real-time processing result with corner reflectors.

As shown in Fig. 11, the imaging scene is 350 m × 420 m (range × azimuth). Corner reflectors from #1 to #5 in Fig. 11 are five point targets. To demonstrate the imaging performance, the two dimensional Impulse Response Width (IRW), Peak Side Lobe Ratio (PSLR) and Integrated Sidelobe Level Ratio (ISLR) of P2 in the object scene are listed in Tab. 3.

| Parameters | P2 |
|---|---|
| Range IRW [m] | 0.338 |
| Range PSLR [dB] | -33.08 |
| Range ISLR [dB] | -16.32 |
| Azimuth IRW [m] | 0.505 |
| Azimuth PSLR [dB] | -31.52 |
| Azimuth ISLR [dB] | -15.21 |

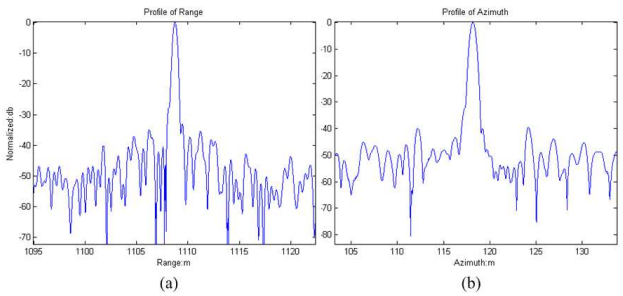
**Tab. 3.** Summarizes of point target analysis.

Due to the variations of the algorithms implemented, it is difficult to have fair comparisons among architectures for SAR applications [7], nevertheless, Table 4 demonstrates a performance comparison between our system and MIRANDA35 from FHR [5]–[6].

| Parameters | Our Sysytem | MIRANDA35 |
|---|---|---|
| Resolution [m] | 0.34 × 0.51 | 2 × 2 |
| Signal Bandwidth [MHz] | 600 | 600 |
| Swath Width [m] | 800 | 1000 |
| Size [cm3] | 14 × 14 × 10 | 52 × 42 × 27 |

**Tab. 4.** The performance comparison with MIRANDA35.

The azimuth and range profiles of corner reflector 2 in Fig. 11 are shown in Fig. 12(a) and Fig. 12(b), respectively.




(a) (b)

**Fig. 12.** Profiles of P2 in (a) range and (b) azimuth.

With the Hamming weighting, the obtained values of the range resolution and azimuth resolution are 34 cm and 51 cm, respectively, which are very close to the theoretical result. The PSLR and ISLR results are pretty good in both directions. As shown in Tab. 3 and Tab. 4, the analysis results demonstrate a high focusing quality, and the efficiency of proposed parallel processing architecture is also validated.

# 5. Conclusion

In this paper, an efficient parallel processing strategy for SAR real-time imaging is proposed. With the application of proposed method, only an eight-core DSP is fully competent for the high-resolution real-time processing of FMCW SAR. Based on the proposed parallel processing strategy, the imaging algorithm is easily realized in modular design. More importantly, the time consumption of SAR imaging is considerably reduced. The performance of proposed parallel processing strategy has been tested on a compact processing board. Moreover, the efficiency of real-time processing has been verified through airborne tests, and beneficial results have been achieved.

# Acknowledgments

Our group has paid hard work for this compact Ku-band high-resolution and real-time FMCW SAR. In this team, each talented member made numerous contributions, including Dr. Jia, Dr. Tian, and Kai Li.

# References

[1] META, A., HOOGEBOOM, P., LIGTHART, L. P., et al. Signal processing for FMCW SAR. *IEEE Transactions on Geoscience Remote Sensing*, 2007, vol. 45, no. 11, p. 3519–3532. ISSN: 0196-2892. DOI: 10.1109/TGRS.2007.906140

[2] JIA, G. W., CHANG, W. G. Study on the improvements for the high resolution FMCW SAR imaging. *Radar, Sonar and Navigation*, 2014, vol. 8, no. 9, p. 1203–1214. ISSN: 1751-8784. DOI: 10.1049/iet-rsn.2013.0383

[3] AN, D. X., HUANG, X. T., JIN, T., et al. Extended two-step focusing approach for squinted spotlight SAR imaging. *IEEE Transactions on Geoscience Remote Sensing*, 2012, vol. 50, no. 7, p. 2889–2900. ISSN: 0196-2892. DOI: 10.1109/TGRS.2011.2174460

[4] MITTERMAYER, J., MOREIRA, A., LOFFELD, O. Spotlight SAR data processing using the frequency scaling algorithm. *IEEE Transactions on Geoscience Remote Sensing*, 1999, vol. 37, no. 5, p. 2198–2214. ISSN: 0196-2892. DOI: 10.1109/36.789617

[5] PALM, S., WAHLEN, A., STANKO, S., et al. Real-time onboard processing and ground based monitoring of FMCW-SAR videos. In *Proceedings of the 10th European Conference on Synthetic Aperture Radar (EuSAR)*. Berlin (Germany), 2014, p. 1–4. ISBN: 9783800736072.

[6] JOHANNES, W., STANKO, S., WAHLEN, A., et al. Implementation of a 35 GHz SAR sensor and a high resolution camera to enable real-time observation. In *Proceedings of the 10th European Conference on Synthetic Aperture Radar (EuSAR)*. Berlin (Germany), 2014, p. 315–318. ISBN: 9783800736072.

[7] WANG, D., ALI, M. Synthetic aperture radar on low power multicore digital signal processor. In *Proceedings of the High Performance Extreme Computing (HPEC)*. Waltham (MA, USA), 2012, p. 1–6. ISBN: 9781467315777. DOI: 10.1109/HPEC.2012.6408665

[8] Texas Instruments Incorporated. *TMS320C6678 Multicore Fixed and Floating-Point Digital Signal Processor (data manual)*. 217 pages. [Online] Cited 2011-08-23. Available at: http://www.ti.com.cn/cn/lit/ds/symlink/tms320c6678.pdf

[9] Texas Instruments Incorporated. *Enhanced Direct Memory Access (EDMA3) Controller (user guide)*. 175 pages. [Online] Cited 2011-03-23. Available at: http://www.ti.com.cn/cn/ug/sprugs5a/sprugs5a.pdf

[10] GU, C. F., LI, X. Y., CHANG, W. G., et al. Matrix transposition based on TMS320C6678. In *Proceedings of the 5th Global Symposium on Millimeter Waves (GSMM)*. Harbin (China), 2012, p. 29–32. ISBN: 9781467313025. DOI: 10.1109/GSMM.2012.6314000

[11] FORNARO, G. Trajectory deviations in airborne SAR: Analysis and compensation. *IEEE Transactions on Aerospace and Electronic Systems*, 1999, vol. 35, no. 3, p. 997–1009. ISSN: 0018-9251. DOI: 10.1109/7.784069

[12] CHO, B. L., KONG, Y. K., PARK, H. G., et al. Automobile-based SAR/InSAR system for ground experiments. *IEEE Geoscience Remote Sensing Letters*, 2006, vol. 3, no. 3, p. 401–405. ISSN: 1545-598X. DOI: 10.1109/LGRS.2006.873358

# About the Authors ...

**Chengfei GU** was born in Nantong, Jiangsu Province, China, in 1988. He received the BS degree in Communication Engineering from Harbin Institute of Technology, Heilongjiang, China, in 2010, and the MSc degree in Information and Communication Engineering from National University of Defense Technology, Changsha, China, in 2012. He is currently working toward the PhD degree at the National University of Defense Technology of China. His research interests include radar imaging and real-time processing.

**Wenge CHANG** received the BS, MSc, and PhD degrees in Information and Communication Engineering from the National University of Defense Technology, Changsha, China, in 1987, 1993, and 2001, respectively. He is currently a professor with the National University of Defense Technology. His fields of interest include synthetic aperture radar system, and real-time signal processing and SAR image processing.

**Xiangyang LI** received the BS, MSc, and PhD degrees in Information and Communication Engineering from the National University of Defense Technology, Changsha, China, in 1993, 1996, and 2000, respectively. He is currently an associate professor with the National University of Defense Technology. His fields of interest include synthetic aperture radar systems, real-time signal processing.

**Zhaohe LIU** received the BS degree in Information and Communication Engineering from the National University of Defense Technology, Changsha, China, in 1987, and the PhD degree in Department of Information Technology from PLA University of Science and Technology, Nanjin, China, in 2005. He is currently a senior engineer with the Science and Technology on Near-Surface Detection Laboratory. His fields of interest include mine detection technology.