A Verilog-A Based Fractional Frequency Synthesizer Model for Fast and Accurate Noise Assessment

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Abstract. *This paper presents a new strategy to simulate fractional frequency synthesizer behavioral models with better performance and reduced simulation time. The models are described in Verilog-A with accurate phase noise predictions and they are based on a time jitter to power spectral density transformation of the principal noise sources in a synthesizer. The results of a fractional frequency synthesizer simulation is compared with state of the art Verilog-A descriptions showing a reduction of nearly 20 times. In addition, experimental results of a fractional frequency synthesizer are compared to the simulation results to validate the proposed model.*

Keywords

Frequency synthesizers, fractional, modeling, sigma-delta, phase noise, Verilog-A

1. Introduction

The design of fractional frequency synthesizers (FFS) on an integrated circuit is an extensively explored research topic [1–3]. These circuits are very important in wireless communications and clock recovery circuits [4], thus the design and simulation strategies for these circuits are still of interest. A FFS is composed of a Phase Locked Loop (PLL) based frequency synthesizer with a programmable divider. The modulus in the divider is pseudorandomly changed by a $\Sigma\Delta$ modulator (usually digital). In this way, the signal's output frequency is an integer (N) plus a fractional value ($K/2^m$) of a reference frequency ($F_{\text{out}} = (N + K/2^m)F_{\text{ref}}$) where m is the modulator's number of output bits, see the upper Fig. 1.

In fact, the FFS building blocks are hierarchical circuits and thus the simulations for the circuit design are very time consuming. It comes unpractical when many simulations must run to optimize the components performance and the design time becomes extensive. Besides, if the blocks are simulated at the device level, the simulation time increases further. A good support at this point are behavioral models considering noise and non ideal performance of some subsystems. Simulation tools such as Simulink and CCPSim [5] are a good election but it is not straightforward to substitute the models by device level blocks. On the other hand, Verilog-A is a helpful hardware description language compatible with device level design.

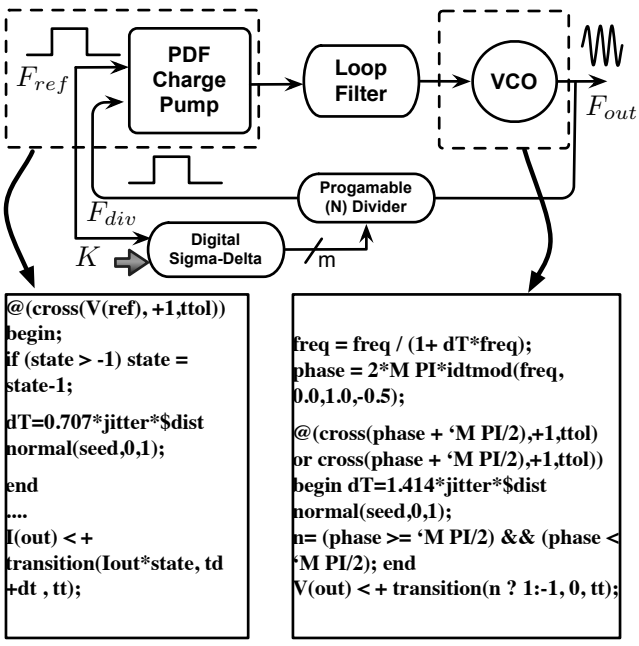


Fig. 1. Scheme of a fractional frequency synthesizer.

Figure 1 shows the schematic representation of a FFS and state of the art Verilog-A descriptions of the Phase to Freqency Detector (PFD), Charge-Pump (CP) and the Voltage Controlled Oscillator (VCO). Particularly, these circuits are important because the noise and error sources are critical for the FFS design [6], [7]. In addition, the FFS's error and noise sources can be concentrated in these subsystems [2]. Note also in Fig. 1 the command *transition*, which incorporates

the non ideal performances as time jitter for the FFS [8], [9]. In spite of the simplicity and acceptable correspondence with experimental results, the models describe phase noise in FFS for a limit of frequencies offset from the carrier because the command *transition* imposes some constraints at the simulation time.

This paper describes the aforementioned limitations and proposes to incorporate the FFS non ideal performance with Verilog-A models with an analog noise fundament, which from our point of view is more related to the circuit design parameters [6]. Section 2 resumes the principal noise sources for a FFS and presents the theoretical base to transform time jitter to the phase noise representation. Section 3 details the proposed models for the PFD-CP and VCO in the FFS which are based on an analog additive noise description. Section 4 presents behavioral simulation results of the models applied to a fractional frequency synthesizer comparing the PFD-CP and VCO models with the widely accepted models in literature, also this section presents the models validation through phase noise experimental results from a fractional frequency synthesizer on a single Bulk CMOS chip. Finally, Sec. 5 draws conclusions.

2. Transformation from Phase Noise to Time Jitter

Phase noise and jitter are two ways to describe the signal's integrity in Frequency Synthesizers; the former in frequency domain and the latter in time domain. There are analytical expressions which allow to express the quantity of displacement from the expected values in each domain. These mapping functions are widely accepted in the literature and have shown a good matching to the physical FFS perdormance [7], [8]. Typically, behavioral models for VCOs and Frequency synthesizers are described with long term and short term jitter of the output signal. In this work, the proposed behavioral models are on a frequency domain base and therefore we resume important relationships to go from one domain to another to quantify the noise perturbations properly.

The principal noise sources for fractional frequency synthesizers can be grouped in three: noise from the PFD-Charge-Pump, from Loop-Filter-VCO and from the digital $\Sigma\Delta$ modulated division factor. With this frequency domain model, the total output phase noise is estimated considering the individual noise sources in the loop shown in Fig. 2. For every case:

$$S_{\text{out}_n}(f_m) = |H_n(j2\pi f_m)|^2 \, S_{\text{input}_n}(f_m), \tag{1}$$

$$S_{\text{synt}}(f_m) = \sum_n S_{\text{out}_n}(f_m) \tag{2}$$

where $S_{\text{out}_n}(f_m)$ represents the n-th contribution to the total synthesizer's noise $S_{\text{synt}}(f_m)$. The S_{input_n} terms are noise sources which are shaped by its own input-to-output phase noise transfer function $H_n(j2\pi f_m)$. Comparing to the jitter

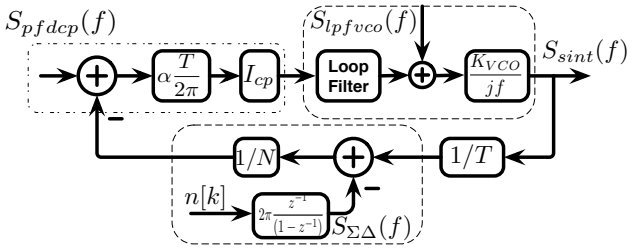


Fig. 2. Synthesizer's equivalent frequency-domain model.

based representation, this spectral based model describes directly the circuit design parameters in behavioral models.

Complementary, jitter is the timing error of a transition event in a signal. The error can be represented as a time function ($j(t)$) having a normal distribution. Starting from a jitter free signal; the error can be added as in [8], [9]:

$$V_{\text{Jitt}}(t) = v\,(t + j(t))\,. \tag{3}$$

To calculate the variance of the error timing signal $\sigma\,(j(t))$, the specified phase noise mask can be related to jitter. For this, it is necessary to distinguish between jitter in autonomous circuits (*short term jitter*) and jitter in driven circuits (*long term jitter*).

For autonomous circuits, short term jitter $\sigma\left(j_{fm}(t)\right)$ is estimated by considering phase noise as [8]:

$$S_\phi(f_m) = a\frac{f_o^2}{f_m^2} \tag{4}$$

where a is the Power Spectral Density (PSD) of the noise generating jitter. For analytical purposes it is more useful to relate phase noise to the noise figure $L\{f_m\}$ by the equation:

$$L\{f_m\} = \frac{S_\phi(f_m)}{2} = \frac{a}{2}\frac{f_o^2}{f_m^2}. \tag{5}$$

In this way, the jitter time variance can be estimated from the $L\{f_m\}$ noise figure as:

$$J_k = \sqrt{kaT} \tag{6}$$

where k is the period index and T is the oscillation period. Note the parameter a is the same in equation (4) giving an important link between these mapping functions.

For driven circuits which present long term jitter; the time displacing variance $\sigma\left(j_{\text{pm}}(t)\right)$ of every transition event is directly related to the power spectral density of the noise source. Defining the long term jitter with:

$$J = \sqrt{2\sigma\left(j_{\text{pm}}(t_c)\right)} \tag{7}$$

where t_c is the time of a transition output event. The function $\sigma\left(j_{\text{pm}}(t_c)\right)$ is defined as the relation between the time average of the noise power generating jitter and the signal's slew rate

$$\sigma\left(j_{\mathrm{pm}}(t_c)\right) \equiv \frac{\sigma(\eta_n)}{\frac{\partial(v_{t_c})}{\partial(t)}}. \tag{8}$$

Using the Parserval's theorem and the simplest slew rate definition it is possible to show that [8]:

$$J = \frac{\sqrt{T\langle\eta_n^2\rangle t_t}}{V_H - V_L} \tag{9}$$

where

$$\langle\eta_n^2\rangle = \int_{-\infty}^{\infty} S_n(f)\mathrm{d}f \tag{10}$$

is the total average noise power spectral density which generates jitter. The t_t parameter is the signal's transition time and $V_H - V_L$ is the total signal change. In resume, equations (6) and (9) should be used to model jitter variance in behavioral models by transforming its phase noise figure mask (usually given in dBc). An example of the application of this equations will be exhibited in Sec. 4.

3. Proposed Frequency Synthesizer Behavioral Model

The proposed behavioral model for the FFS includes noise as shown Fig. 3, it considers the main noise sources in a fractional frequency synthesizer being: noise from the Loop Filter and VCO, noise from the PFD-CP and the digital $\Sigma\Delta$ modulation quantization noise. These noise sources are incorporated in a behavioral analog description of noise in the PFD-CP and VCO scripts.

Let us describe the VCO using the relationship for the output phase deviations and control voltage (V_{ctrl}):

$$\Phi_{\mathrm{out}}(t) = \int 2\pi K_v V_{\mathrm{ctrl}}(t)\mathrm{d}t. \tag{11}$$

This expression can be modeled by the following script:

```
analog begin
        freq = (V(input)-Vmin)*(Fmax-Fmin)/ (Vmax-Vmin) + Fmin;
        if (freq > Fmax) freq = Fmax;
        if (freq < Fmin) freq = Fmin;
        phase = 2*M-PI*idtmod(freq,0.0,1.0,-0.5);
        sipha = sin(phase)
        v(out) < + sipha;
end
```

The ideal behavior will be deviated with noise sources into the VCO and Loop Filter, the noisy signals blur the VCO's phase randomly from cycle to cycle. For the proposed model a normal-distributed random number generator describes this white noise source as shown in Fig. 4. Note that the Loop Filter's noise is included as the output referred noise and is added to the input referred noise to the VCO. The advantage of grouping the noise descriptions, is a reduced simulation time.

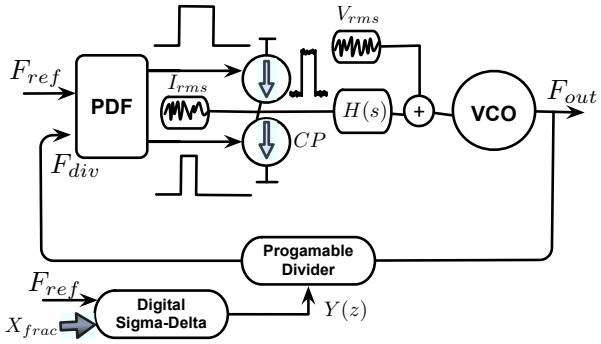


Fig. 3. Schematic representation for the Verilog-A model with the proposed scripts.

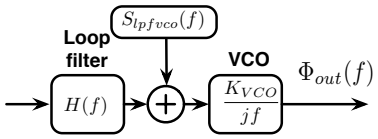


Fig. 4. VCO and Loop Filter additive noise description.

The total power delivered by the input referred noise source is equal to the variance of a random signal representing this noise:

$$\sigma^2(\eta) = \int_0^{\infty} S(f)\,\mathrm{d}f. \tag{12}$$

For a white noise source, $S(f) = \kappa$ and the total noise delivered by a noise power spectral density is evaluated from (12). This integral has no a closed form solution but there is a solution for filtered white noise source (similar to the effect of kT/C noise in analog filter circuits). A limit frequency is estimated as the one with the most dynamic for the simulation, i.e. the signal with sampling frequency for post processing (F_{sample}) to obtain a spectral amplitude.

During this work, if a relatively low frequency white-noise signal is sampled at a frequency F_{sample}, total root mean squared (*rms*) value for the noise source is therefore:

$$\eta_{\mathrm{rms}} = \sqrt{S(f)\,F_{\mathrm{sample}}} \tag{13}$$

and the estimated PSD needs only to be scaled according to the processing gain, i.e. F_{sample}/N. The noise source in Fig. 4, including contributions from loop filter and VCO are described by the script:

```
analog begin
        @ (initial-step) begin seed = 23;
        end
        vrms= sqrt(power*Fsample);
        randnum= $dist-normal(seed,0,1);
        V(out) < + randnum*vrms;
end
```

For the PDF-CP model it is important to consider that FFS are a special case of phase locked loop systems. In fact, these systems never lock as the instantaneous division modulus is constantly varying with time. Therefore, the nonlinearity in the charge pump is critical in the phase noise figure.

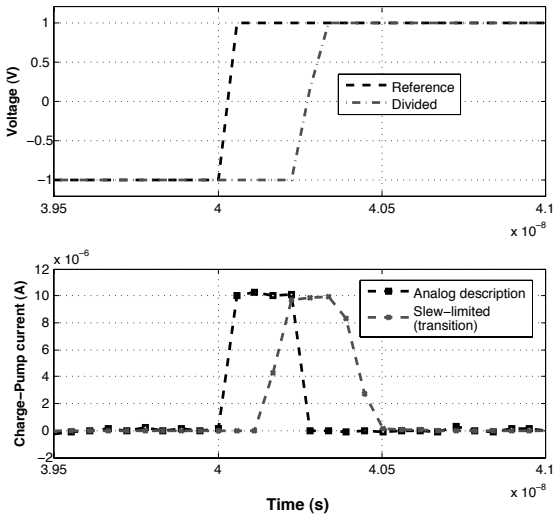


Fig. 5. Charge Pump current pulses showing the limit for jittered description.

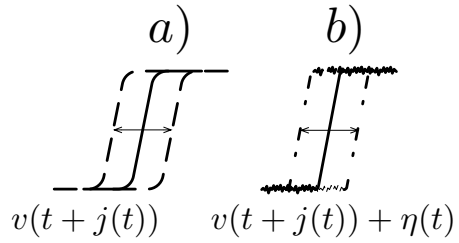


Fig. 6. Waveforms with jitter and jitter plus charge pump noise.

The same occurs for the simulation of fractional synthesizers at behavioral level. For an integer frequency synthesizer description, it is sufficient to use the models widely accepted in literature [8], [12] (the models are resumed in Fig. 1) with a timing limitation for the delay and tolerance parameters in the command *"transition"*. The "*td*" and "*tt*" are parameters that the *transition* command uses for delay and tolerance values. For the case of an ideal integer PLL, the phase to frequency detector ideally locks and when F_{ref} and F_{div} signals are in phase, with no pulse currents to the loop filter. In resume, the mentioned models are adequate for integer frequency synthesizers because, once they are in lock, the PDF-CP non linear performance is not of big impact [13].

However, this is not the case of a FFS. For shake of brevity it is only important to highlight the limitation in the command *"transition"* in FSS. Even for the ideal (noiseless) fractional synthesizer, the reference and divided phases at the PFD's input never lock and there are always current injection to the loop filter. In addition, this pulses are very small because the closed loop is *"near to lock"*. If the command *transition* is used to describe the noise in the charge pump currents (described in magnitude by *"irms"*), the parameters td, tt impose a limit in the charge transfer when phase differences are very small. The result is an incomplete description on charge pump's behavior as shown in Fig. 5 for the *slewed limit on transition* curves. Also, the nonlinearity described into the timing command is prone to increase the simulation time.

To solve this important issue with the behavioral simulation the proposed behavioral description for the PDF-CP incorporates the additive noise as is shown in the following script:

```
@(cross(V(ref), +1))
   if (state > -1) state = state-1;
@(cross(V(div), +1))
   if (state < 1) state = state+1;
randnum=$dist_normal(seed,0,1);
irms = sqrt(inpow*Fs);
I(out) < + iout*state + irms*randnum;
```

This is a description that allows to model fractional frequency synthesizers with accurate descriptions for the charge pump pulses when the difference between phases is very small. The waveforms from a simulation of the proposed behavioral charge pump model are also shown in Fig. 5 (the analog description case), now the output charge pump pulses describe more precisely the injected current. The *rms* contribution of the CP as a result of jitter in the digital circuits can be mapped with the help of eqns. (6) and (9). Additionally, the proposed behavioral model includes the noise from the current source circuits in the CP that otherwise is difficult in the time domain description. For instance, Fig. 6 shows graphically the importance of this noise source, which even in recent models are not considered [13].

4. A Comparison of the Model and Validation with Measurements

4.1 A Comparison with State of the Art Models

The proposed behavioral Verilog-A scripts are used to model a FFS with Spectre® in a Virtuoso® Analog Environment and is confronted to a time jittered based model [8], [9]. Figure 7 exhibits a comparison of the simulated schemes highlighting the principal Verilog-A scripts. The time jitter based model uses as disturbance parameter the variable *jitter* for both the PFD-CP and VCO.

On the other hand, the model in this work (rightmost in Fig. 7) considers disturbances at the *rms* noise in the charge pump I_{rms} and VCO Loop Filter V_{rms} noise. For illustration purposes, an independent block for the $I_{\text{rms}}, V_{\text{rms}}$ disturbances is shown in the scheme but of course these can be incorporated into the PDF-CP and VCO blocks.

The conditions for both simulation models are the same in terms of post signal processing and other ideal blocks. For the digital $\Sigma\Delta$ modulator and programmable frequency divider, a good alternative is to substitute logic gate circuits by ideal behavioral models. The phase noise characteristic for these blocks can also be included (similarly to the

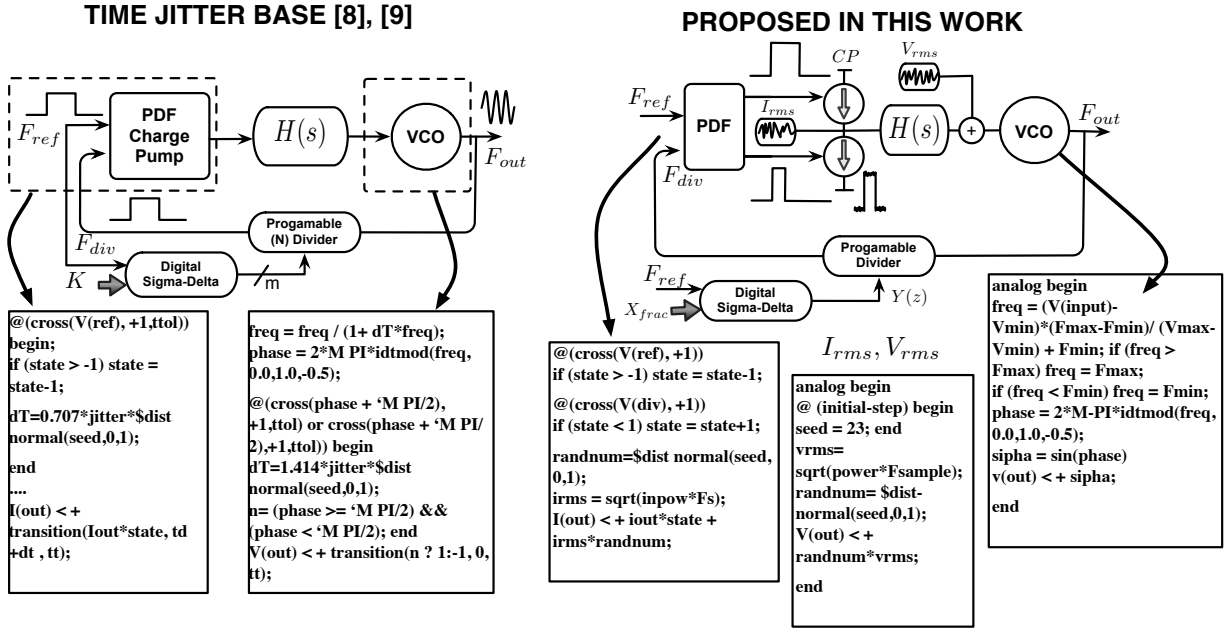


Fig. 7. Schematic representation for the Verilog-A model with the proposed scripts.

Parameter	Value	Parameter	Value
Synthesizer order	4th	ΣΔ order	3th
ΣΔ architecture	Third order MASH dithered	Fractional Resolution	1/256
Closed-Loop cut-off frequency	25 kHz	F_{ref}	25 MHz
Charge-pump current	10 µA	Programmable division moduli	$N = (64, \ldots, 79)$
Charge-Pump input referred noise ($S_{\text{pfdcp}}(f)$)	$\approx 3 \times 10^{-24}$ A^{2}Hz^{-1}	Mean CP current noise $I_{\text{rms}}(f)$)	0.56 µA
VCO Loop-Filter output referred noise ($S_{\text{lpfVCO}}(f)$)	$\approx 2 \times 10^{-18}$ V^{2}Hz^{-1}	Mean LPF VCO voltage noise $V_{\text{rms}}(f)$	125 µV
Charge-Pump jitter (J_{cp})@F_{ref}	3.8×10^{-16} s	VCO Loop-Filter jitter (J_{VCO})@1.65 GHz	5.5×10^{-14} s

Tab. 1. List of parameters for the behavioral Verilog-A simulations.

PFD-CP cases) but it is important to notice if their contribution affect the overall phase noise figure. The objective is to obtain a good trade-off between simulation time and accuracy on phase noise prediction. The behavioral model schemes in Fig. 7 were implemented in the Virtuoso Analog environment, every block has its own script and can be latter substituted by transistor level or spice netlists.

The modeling parameters for both implementations where extracted from a previously designed and fully integrated FFS on a 0.35 µm CMOS process, and are detailed in Tab. 1. The most relevant parameters for the fractional synthesizer's dynamics are: the voltage controlled oscillator (*VCO*) gain K_{VCO}, charge pump current I_{CP} and loop filter cut-off frequency f_c (for $H(s)$ in Fig. 7). The principal noise sources in the proposed model are modeled by mean squared valued input referred noise sources as explained in Section 3. The charge pump input noise spectral density $S_{\text{pfdcp}}(f)$ is modeled with the parameter I_{rms} and is obtained from the charge pump current sources as following. Let the power spectral density for the charge pump transistors to be:

$$S_{\text{pfdcp}}(f) = 4kT(2/3)g_m \tag{14}$$

where

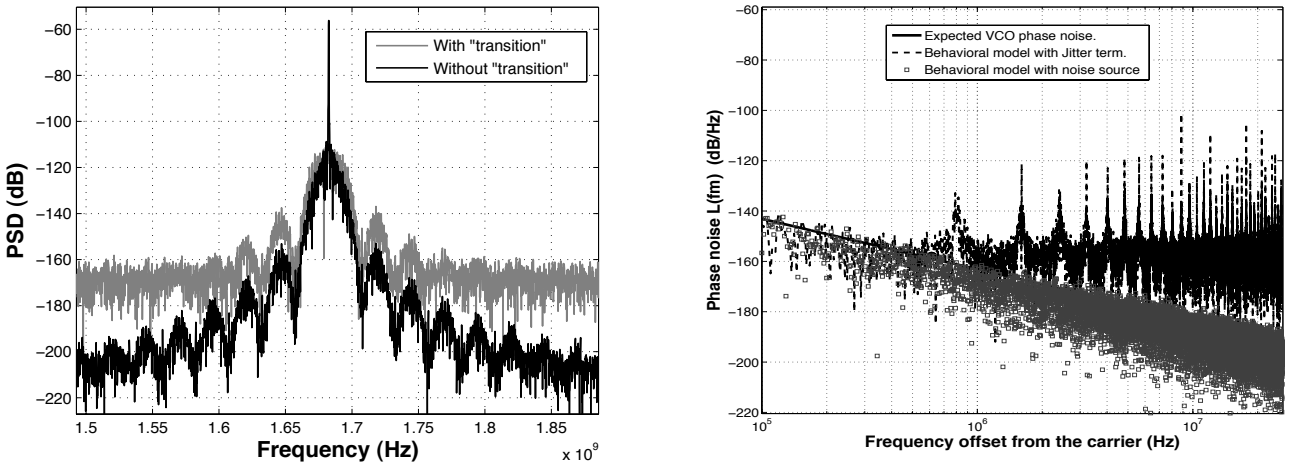
$$g_m \approx \frac{2I_D}{(V_{\text{gs}} - V_{\text{th}})} \tag{15}$$

for $I_{\text{cp}} = 10\,\mu\text{A}$ and a 0.2 V overdrive, the approximated noise density is $S_{\text{cp}}(f) = 3 \times 10^{-24}$ A^{2}Hz^{-1}. For a sample frequency of $F_{\text{sample}} = 7.9$ GHz, the input refereed noise has a random mean square value (see eqn. (13)):

$$I_{\text{rms}} = \sqrt{S_{\text{pfdcp}} F_{\text{sample}}} = 0.56\,\mu\text{A}. \tag{16}$$

The Loop Filter (*LPF*) and *VCO* phase noise contribution $S_{\text{lfVCO}}(f)$ is modeled with the parameter V_{rms} and is calculated similarly to the charge pump approximation.

The same disturbances are modeled in the time jittered approach with help of the equations resumed in Sec. 2 which map the $L\{f_m\}$ and $a = S(f)$ parameters to the jitter variance for each block. In other words, with the $S_{\text{pfdcp}}(f)$, $S_{\text{lpfVCO}}(f)$ values in Tab. 1 and equation (6) is possible to calculate the jitter mean value which is also presented in the mentioned table as parameters J_{cp} and J_{VCO} respectively.



(a) Estimated power spectral density.

(b) Phase noise contribution of the VCO.

Fig. 8. A comparison of the behavioral simulation results for the FFS and the VCO contrabution.

	Jittered (transition) ref. [8], [9] leftmost in Fig. 7	Additive noise (analog) **this work** rightmost in Fig. 7
SO	Linux SLES 11	Linux SLES 11
Simulator	Spectre®	Spectre®
# Processors	24	24
Processor model	E55645@2.4 GHz	E55645@2.4 GHz
RAM	39.2 G	39.2 G
# samples	2^{23}	2^{23}
Simulation time	31400 s	1540 s

Tab. 2. Behavioral simulation setup comparison.

With these parameters, behavioral simulations were launched for $f_{\text{out}} = \left(67 + \frac{77}{256}\right) f_{\text{ref}}$ with the time jitter and the proposed behavioral models. The power spectral densities where calculated with a *pwelch* algorithm from a 2^{22} size sequence of the synthesizer output at $F_{\text{sample}} = 7.9\,\text{GHz}$. To estimate the FFS output spectral amplitude, the processing gain must be considered and is related to the number of samples and the sampling frequency i. e. F_s/N.

Figure 8 shows the simulation results for the FFS's spectrum and phase noise VCO's contribution. The charge pump input referred noise is modeled in a time domain jitter representation (when the command *transition* is utilized) and is compared to the obtained when using an analog input referred noise description (as proposed in this paper). With the command *"transition"* and *slew* and *delay* of 50 ps, the output spectrum in Fig. 8(a) is well predicted only for low frequencies offset from the carrier (note also Fig. 8(b)), because this command introduces the non linear characteristics that are not present in the charge pump (previously mentioned in Sec. 3).

In addition, the command transition combined with the noise additive noise model increases the simulation time. For the proposed model, under the same conditions, the simulation time is reduced nearly 20 times. For the present case the time jitter approach takes about eight hours to complete a simulation while the proposed model uses 25 minutes. Table 2 presents the simulation details, comparing the proposed Verilog-A scripts with the state of the art time jitter models. The proposed models reduce the simulation time with no loss of accuracy.

4.2 Model Validation with Experimental Results

To validate the proposed behavioral models, the Verilog-A simulation results are compared to experimental phase noise measurements. The fractional frequency synthesizer was designed and fabricated on an AMS 0.35 µm bulk CMOS process. Figure 9 shows the principal IC building blocks and the test setup configuration.

The fractional synthesizer contains a LC-tank based VCO with NMOS structures as varactors for voltage tuning. An active loop filter configuration cascaded to a passive RC filter yields a third order transfer function [14], thus giving rise to a fourth order Type II fractional synthesizer. The charge pump circuits were designed with low sensitive current sources and dummy current sources prevent large glitches on the current transitions [2]. A traditional PFD circuit with D-Flip flops performs the phase control loop. The programable frequency divider works with a phase selection technique including a synchronization network to avoid erroneous division moduli which come as a result of process, temperature and bias variations.

For the fractional division, a third order 8-bit digital $\Sigma\Delta$ modulator pseudorandomly changes the programable divider's division modulus with a dithered sequence

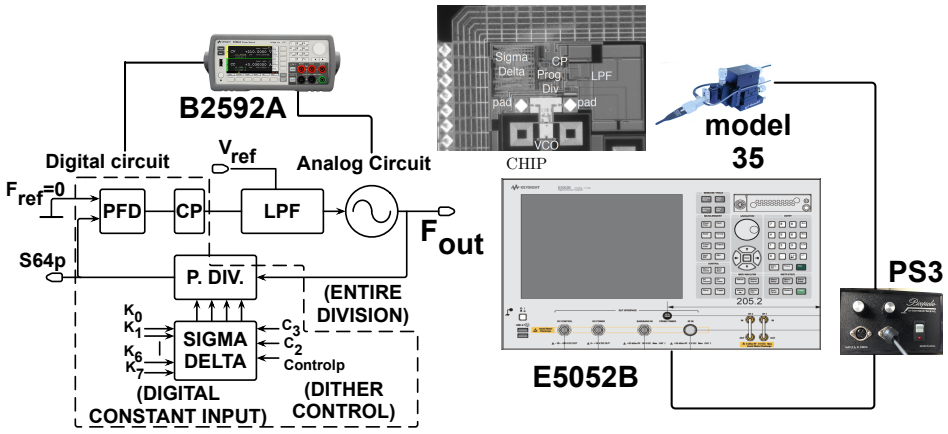
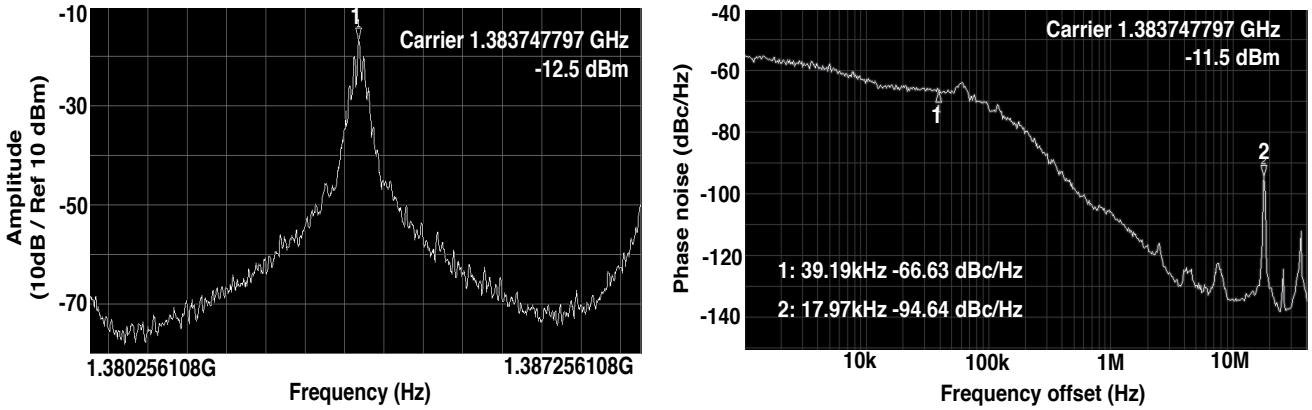


Fig. 9. Test setup for the fully integrated fractional frequency synthesizer to validate the proposed model.



(a) Measured spectrum of the FFS.

(b) Phase noise measurement result.

Fig. 10. Experimentar results of a FFS to compare the proposed behavioral models.

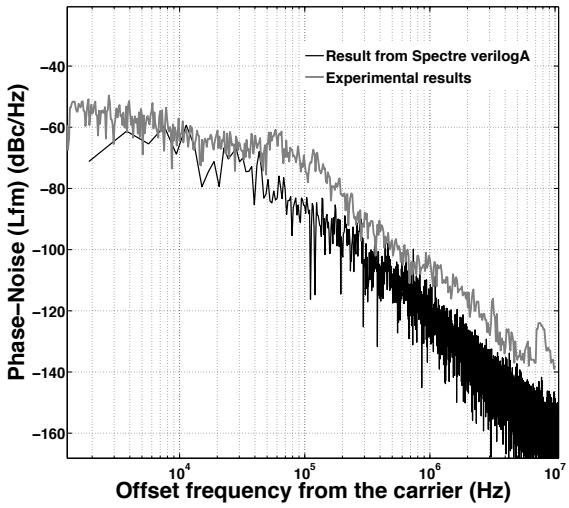


Fig. 11. Response for the phase noise simulation compared to the experimental results.

on the chain of accumulators to improve randomness of the controlling sequence [11]. The fractional factor is programmed with the ΣΔ digital constant value (pins $K_0, \ldots, K_7$ in Fig. 9) and the control pins $C_0, \ldots, C_3$ set the entire division factor. The entire division moduli have this restriction from the output dynamic range on the digital ΣΔ modulator, as it roams between 4 different division moduli.

Table 1 also encloses the fractional frequency synthesizer's parameters also used for the behavioral simulation. The test printed circuit board was fixed to a Cascade BTS100 system to reduce vibrations and noise from external sources. The phase noise experimental results were obtained measuring the synthesizer's output with an E5250B Signal Source Analyzer, shown in Fig. 9. To test on chip the RF signal, one analog buffer stage on every VCO's output node is set to On-Chip *pads*. The signal source analyzer obtained the RF signal with the active probe Picoprobe Model 35 and the PS-3 power supply. A very low noise source B2952A was used to set the 3.3 V for the analog and digital sections of the chip. For this measurement the reference input for the fractional synthesizer was disable to strictly measure the phase noise from the integrated synthesizer.

Figure 10 shows the experimental results captured from the E5052B signal source analyzer where the carrier is locked to 1.383747 GHz in the fractional synthesizer. The phase noise figure shows the charge pump idle tones from the sigma delta modulation close to 17.9765 MHz offset from the carrier which is the fractional divider's output frequency and was verified through the output signal $s64p$ in the test board (Fig. 9). It is important to mention that the phase noise result with the proposed noise additive model is compared to the experimental results. Figure 11 presents the phase noise measurements compared to the simulation results under the same conditions, there is a clear congruence between the proposed behavioral simulation results and the experimental phase noise figures. For close to the frequency carrier range $(10-100)$ kHz phase noise is around -70 dB. With the fractional synthesizer's dynamics given by the loop filter's cut off frequency the phase noise falls to -90 dB@1 MHz offset from the carrier frequency. Mixing tones at about 1.5 MHz offset from the carrier frequency appeared on experimental phase noise figure but it is not correlated to reference frequency. A possible source of this high level noise figure is the process variants on the loop filter passive elements. For all frequency ranges the experimental phase noise figure validates the effectiveness of the proposed Verilog-A behavioral models.

5. Conclusions

Behavioral modeling is a powerful tool to predict the dynamic features of mixed signal circuits such as fractional frequency synthesizers. However the behavioral models can be described from several point of views. This paper presented the advantages and drawbacks of modeling phase noise in frequency synthesizers as time jitter in driven and autonomous circuits and proposed a new Verilog-A analog additive noise description.

In the proposed approach the phase noise has been modeled as RMS values for noise sources into the circuits, considering a limit in the spectral density. The experimental results allowed to validate the accuracy of these models comparing the phase noise figures obtained from Verilog-A. With the proposed additive noise approach the simulation time is reduced nearly 20 times compared to noisy jittered models. With the guidelines presented, the models can be extended to circuits fabricated in nano scaled CMOS processes.

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