

Design of 12-phase, 2-stage Harmonic Rejection Mixer for TV Tuners

Dongju LEE, Hocheol JEONG, Minjae LEE

School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju, Korea

minjae@gist.ac.kr

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Abstract. A two-stage 12-phase harmonic rejection mixer (HRM) for TV tuners is proposed in order to reject the local oscillator (LO) harmonics up to the ninth order. The proposed 12-phase weighing scheme can eliminate the third and ninth harmonic rejection (HR) sensitivity to the amplitude error caused by irrational numbers such as $\sqrt{3}$. To verify this HR, the 2-stage HR circuit is designed with baseband g_m scaling in order to save power and improve the HR ratios without calibration. The proposed HRM achieves the third to ninth worst HR ratios, more than 55 dB, according to Monte Carlo simulations. It consumes 6.5 mA under a 2.5 V supply voltage.

Keywords

Harmonic rejection mixer, multiphase, TV tuner, direct conversion, active mixer

1. Introduction

For wideband analog/digital TV tuners covering VHF and UHF bands, harmonic rejection (HR) is a challenging issue because the radio frequency (RF) signals and unwanted signals around the local oscillator (LO) harmonics are translated into the same baseband.

The required HR ratios for TV are 60–70 dB for LO harmonics [1]. In order to suppress the unwanted harmonic mixing, various HR techniques have been introduced [1–4]; however, HR ratios are degraded due to the amplitude and phase errors that result from device mismatch [2]. In order to reduce the sensitivity of the HR to mismatch, 2-stage HR techniques [5], [6] have been presented. The 2-stage harmonic mixing has two merits: amplitude error reduction and small integer numbers for root number generation.

- 1) In 2-stage harmonic mixing [5], the total amplitude error from the HR stages is a multiplication of the errors in the first and second HR stages: $(\varepsilon_{1st} \cdot \varepsilon_{2nd}) / 4$, where ε_{1st} and ε_{2nd} are the relative errors in the first/second HR stages, respectively. Therefore, this 2-

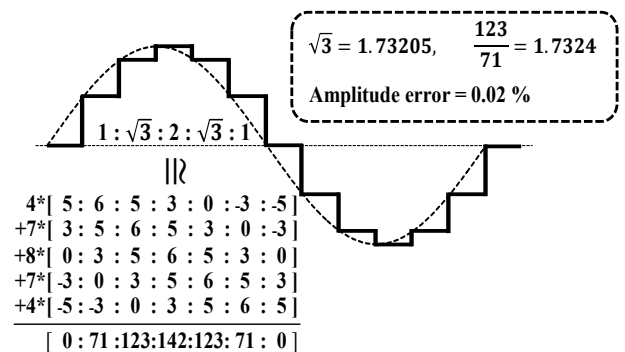


Fig. 1. The effective LO waveform of the proposed HRM.

stage harmonic mixing can reduce the HR sensitivity to stage amplitude errors.

- 2) In order to have a weighting ratio of {0:29:41:29} for an 8-phase LO with 2-stage, weighting numbers in each stage range only between 2 to 7; {2:3:2}/{5:7:5}. Thus, the unit finger width of the transistors can be easily increased to reduce device mismatch.

However, these 2-stage HR techniques use 8-phase LOs in which, particularly for VHF (54–216 MHz) band reception, the odd harmonics higher than the fifth order also down-convert unwanted signals to baseband because input RF frequencies span up to 16X range (from 54 to 860 MHz). To ease the requirements of the RF filter and to extend HR to the ninth harmonic, the number of LO phases must be increased to 12. Conventional 12-phase LO, however, has been reported with 1-stage implementation [7], of which HR ratios are vulnerable to amplitude mismatch or device mismatch.

In this paper, a 12-phase harmonic rejection mixer (HRM) with a 2-stage is proposed to desensitize HR ratios to device mismatch so that the third, fifth, seventh, and ninth HR is realized for TV tuner bands (54–860 MHz). To the extent of our knowledge, a 2-stage HRM with 12-phase LOs has not been reported before. This paper is organized as follows. Section 2 describes the 12-phase HR principle, numerical calculations of HR ratios, and circuit implementations of the HRM. The Monte Carlo simulation results are presented and discussed in Sec. 3. Finally, the paper is concluded in Sec. 4.

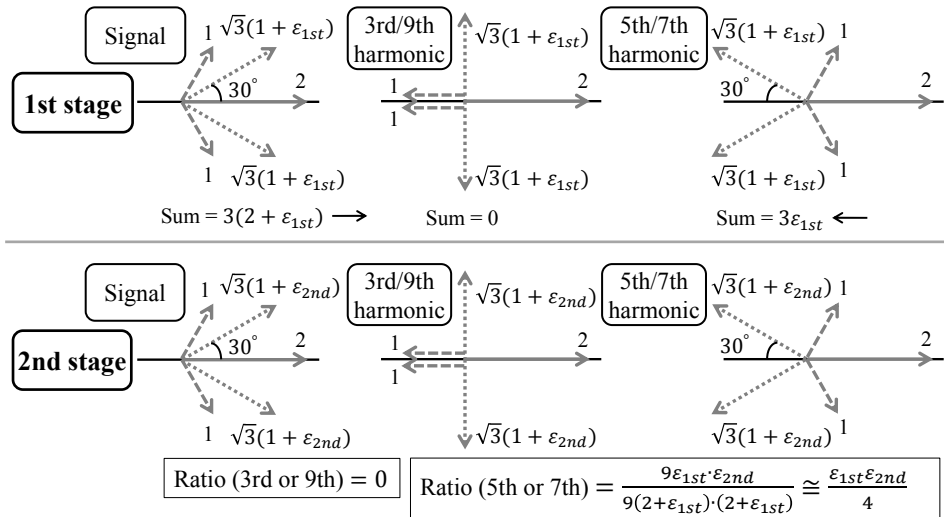


Fig. 2. The vector diagrams of 12-phase 2-stage harmonic mixing.

2. Harmonic Mixing

2.1 Design Consideration

When the number of non-overlapping LO phases is N , the LO harmonics greater than or equal to the $(N-1)^{\text{th}}$ order are not suppressed, which results in poor HR ratios, e.g. only $20\log(n)$ dB for the n^{th} harmonic. Thus, a 12-phase LO is required in order to enable the sine wave to reject the third to ninth LO harmonics, whereas the 8-phase LO [5], [6] can only reject third/fifth LO harmonics. A 12-phase HRM [7] based on LO-gating techniques [8], [9] was realized through 1-stage harmonic mixing with a weighting ratio of $\{6.2:10.8\}$ to approximate $\sqrt{3}$. This $\{31:54\}$ ratio is close to $\sqrt{3}$ with a 0.57% amplitude error. However, it is not easy to implement these high integer numbers with good matching and low power consumption in 1-stage harmonic mixing particularly when transconductance (g_m) scaling [2] is used. The similar issue exists in 8-phase HRMs as well and has been overcome by 2-stage harmonic mixing [5].

To design the 12-phase 2-stage HR circuit, the static amplitude error due to the irrational number ($\sqrt{3}$) limits the achievable HR ratio and should be considered. When the total weighting ratio in order to generate $\{1:\sqrt{3}:2:\sqrt{3}:1\}$ is selected, it is not easy to find corresponding integer weighting ratios for each stage in the 2-stage HR circuit. First, possible small integer weighting ratios to approximate $\{1:\sqrt{3}:2:\sqrt{3}:1\}$ are investigated. Then, weighting ratios for each stage can be extended as follows: $\{2:3:4:3:2\}$, $\{3:5:6:5:3\}$, $\{4:7:8:7:4\}$, \dots , and so on. Two selections among those can make the desired total weighting ratio for the 2-stage HR. In this paper, the $\{3:5:6:5:3\}/\{4:7:8:7:4\}$ ratios were selected to generate $\{0:71:123:142:123:71\}$, as depicted in Fig. 1. The zero factor in this ratio is realized from the cancellation of differential circuits. As the weighting factors increase, the ratio

between the first and second factors approaches $\sqrt{3}$, but higher factors require more areas and power for the g_m scaling technique.

Figure 2 depicts the effects of the relative errors, ϵ_{1st} and ϵ_{2nd} on the approximations for $\sqrt{3}$. The relative errors of third/ninth harmonics are perfectly cancelled despite the non-zero ϵ_{1st} and ϵ_{2nd} because the total vector summation for the third/ninth harmonics becomes zero, which results from the error vectors having equal amplitude and opposite sign. The cancellation of these relative errors helps to improve the third HR ratio (HR3) and HR9. In the case of the fifth and seventh harmonics, the total relative error can be reduced to $\epsilon_{1st} \cdot \epsilon_{2nd} / 4$. The achievable HR5 or HR7 is the sum of the HR ratios in the each HR stage. The ϵ_{1st} in a $\{3:5\}$ ratio for the approximation of $\sqrt{3}$ is 3.775% and the ϵ_{2nd} in a $\{4:7\}$ ratio is 1.03%. Then, the HR ratios in the first and second HR stages are 34.5 dB and 45.76 dB, respectively. The total HR ratio is 80.26 dB, when no phase error is assumed.

2.2 HR Sensitivity Analysis to Amplitude and Phase Errors

When both amplitude and phase errors are considered, the HR ratios are estimated through equations based on [5]. The HR3 of a single-balanced 12-phase HRM is derived as

$$\frac{\sin^2(3\pi/12)}{162\sin^2(\pi/12)} [\sigma_A^2 + 27(1+\epsilon)^2 \sigma_\theta^2] \quad (1)$$

where σ_A is the standard deviation (SD) of amplitude error in percentage, σ_θ is the SD of phase error in radian, and ϵ is the relative error due to the approximation of $\sqrt{3}$ in percentage. From (1), it is noted that σ_A is not multiplied by ϵ since the two $\sqrt{3}$ vectors in the third/ninth harmonics are in the opposite direction as described in Fig. 2. Thus, HR3 is less sensitive to σ_A and dominated by σ_θ in our scheme.

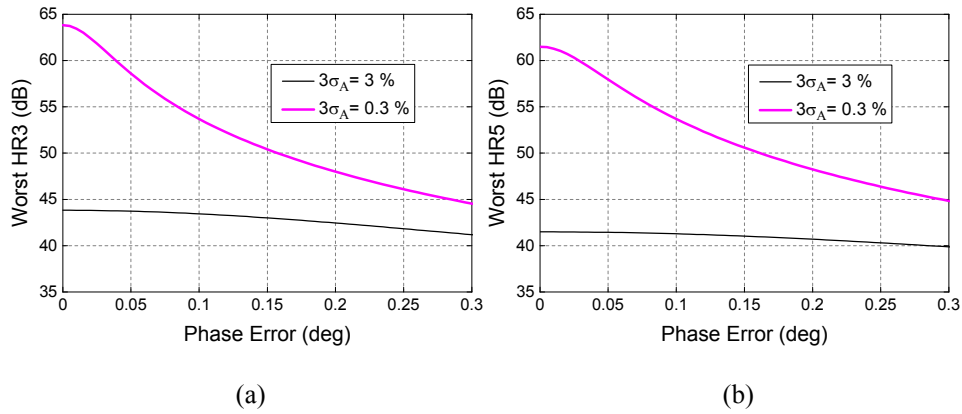


Fig. 3. Estimated (a) HR3 and (b) HR5 versus phase error with $3\sigma_A = 3\%$ and 0.3% for a 12-phase HRM.

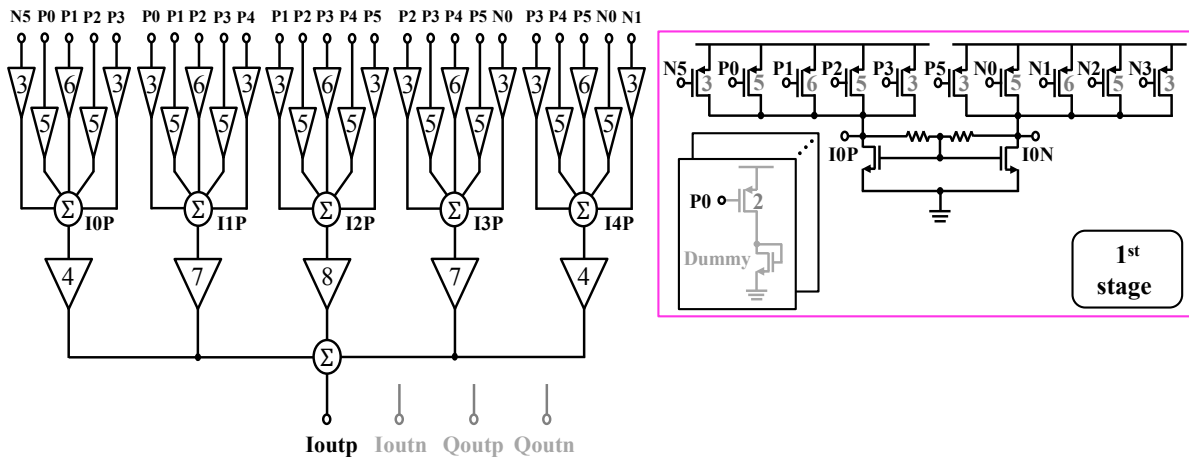


Fig. 4. The 12-phase HR circuit.

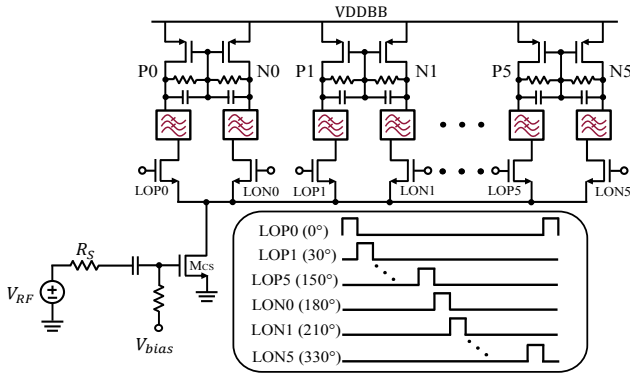


Fig. 5. The RF section of the HRM.

Similarly, the HR5 of a 12-phase HRM is written as

$$\frac{\sin^2(5\pi/12)}{1800 \sin^2(\pi/12)} [(1 + 9(1 + \epsilon)^2)\sigma_A^2 + 75(1 + (1 + \epsilon)^2)\sigma_\theta^2] \quad (2)$$

Assuming $\epsilon = 1\%$, $3\sigma_A$ worst-case HR ratios versus phase error are plotted in Fig. 3. When phase error is zero, the $3\sigma_A$ (0.3%) worst HR3 and HR5 are 63.8 and 61.5 dB. To accomplish HR ratios over than 50 dB, $3\sigma_A$ amplitude error is selected to 0.3% and σ_θ should be less than 0.15° .

2.3 Implementation of HRM

Two methods are conventionally used in baseband HR circuits: the resistor weighting with OTAs and g_m scaling. Although resistor matching is more accurate than g_m matching, the number of OTAs and power consumption increases significantly. Unlike OTAs, which require a constant bias current, the common-source (CS) amplifier with g_m scaling only passes the signal current when the LO switch is on and the branch is active, which results in less current consumption. Thus, the g_m -based HR circuit was implemented in this work. The block diagram of the 2-stage HR circuit for the I and Q channels is presented in Fig. 4. In the first HR stage, PMOS amplifiers have a g_m ratio of $\{3:5:6:5:3\}$ in order to approximate $\{1:\sqrt{3}:2:\sqrt{3}:1\}$.

This g_m ratio is implemented by scaling the total width of MOSFETs. As an instance, the device size for the factor 3 is $W/L = 37.5 \mu\text{m}/1.2 \mu\text{m}$. But the problem is that each PMOS amplifier in the first stage has different C_{gs} due to their different total width, which increases path mismatch and degrades HR performances. To eliminate this mismatch, dummy cells with diode-connected NMOS

	P0	P1	P2	P3	P4	P5	N0	N1	N2	N3	N4	N5	
I0P-I0N	5	6	5	3	0	-3	-5	-6	-5	-3	0	3	·4
I1P-I1N	3	5	6	5	3	0	-3	-5	-6	-5	-3	0	·7
I2P-I2N	0	3	5	6	5	3	0	-3	-5	-6	-5	-3	·8
I3P-I3N	-3	0	3	5	6	5	3	0	-3	-5	-6	-5	·7
I4P-I4N	-5	-3	0	3	5	6	5	3	0	-3	-5	-6	·4
Total	0	71	123	142	123	71	0	-71	-123	-142	-123	-71	

Tab. 1. Weighting factors for 12-phase harmonic mixing.

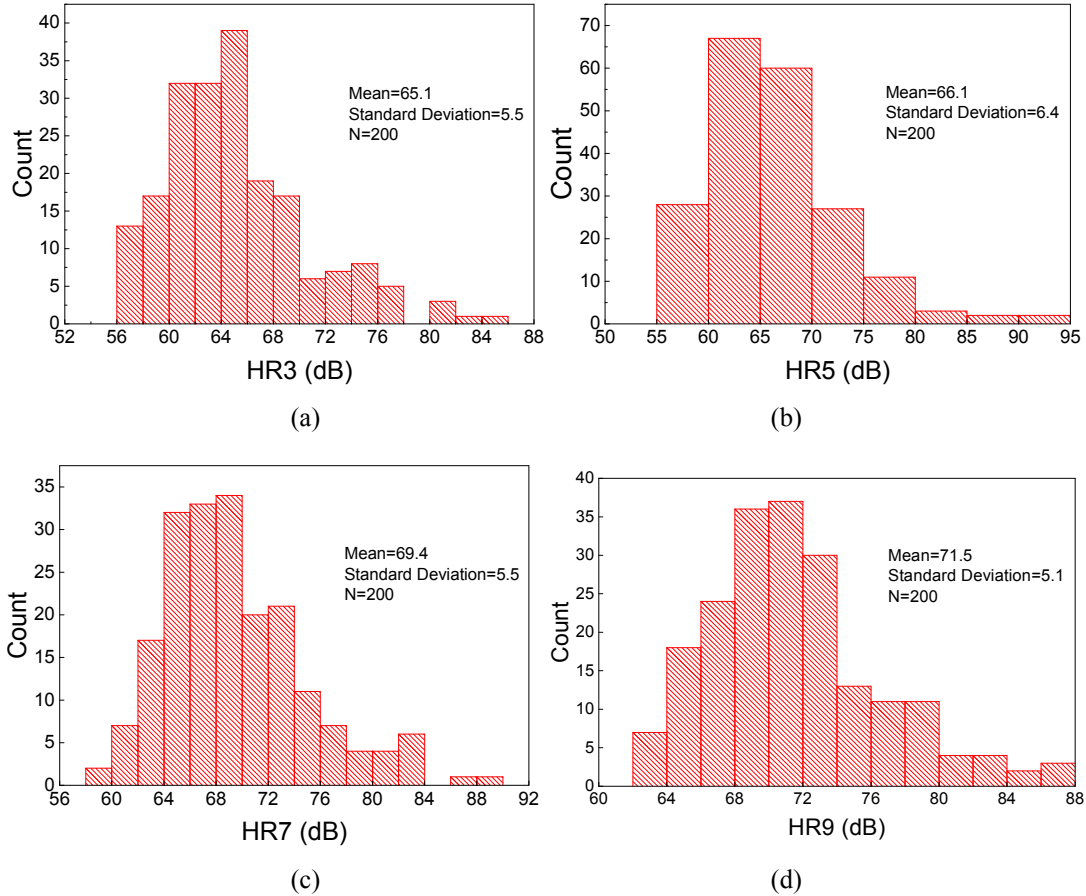


Fig. 6. Monte Carlo simulation results of (a) HR3, (b) HR5, (c) HR7, and (d) HR9 for the proposed 12-phase 2-stage HRM with the weighting ratio of {3:5:6:5:3}/{4:7:8:7:4} at the 111 MHz effective LO.

loads in Fig. 4 are added to match loading capacitances in the paths. The combined drain currents at the first stage outputs are converted to differential voltages via load resistors, which drive the NMOS CS amplifiers in the second HR stage that has a g_m ratio of {4:7:8:7:4} for five 30° phase-shifted signals. These weighting factors are summarized in Tab. 1.

The RF section of the HRM is described in Fig. 5. The CS amplifier (M_{CS}) generates a bias current of 1 mA in order to drive the 12-phase active mixer. The 12-phase LO switches are driven using non-overlapping 8.33% duty-cycle LO signals. The lowpass filters (LPF) are connected to the mixer in order to suppress the LO feedthrough and out-of-band interferers. The mixer, LPFs, and thick PMOS loads operate under a 2.5 V supply for better linearity.

3. Simulation Results

HR performances depend on both amplitude and phase errors of the effective LO waveform. In the g_m -based HR circuit, the LO amplitude is realized by g_m scaling that is sensitive to device mismatch. Thus, the Monte Carlo HR simulations are used to estimate their sensitivity to device mismatch and different process corners as well. In order to find the HR ratios, an RF signal ($111 \cdot N + 4$ MHz, $N = 1, 3, 5, 7, \text{ and } 9$) was applied and down-converted to 4 MHz via the N^{th} order LO harmonics with the 111 MHz effective LO. Then, the power differences between the fundamental and harmonic tones were compared. Figure 6 illustrates that the worst-case third, fifth, seventh, and ninth HR ratios obtained by Monte Carlo simulation are 56, 55, 58, and 62 dB, respectively.

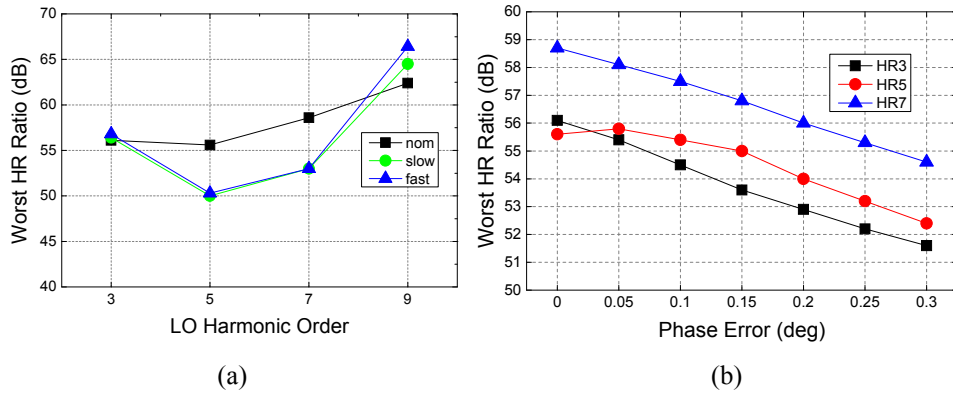


Fig. 7. Worst-case HR ratios from Monte Carlo simulation results (200 runs) with (a) process corners and (b) phase error at the 111 MHz effective LO.

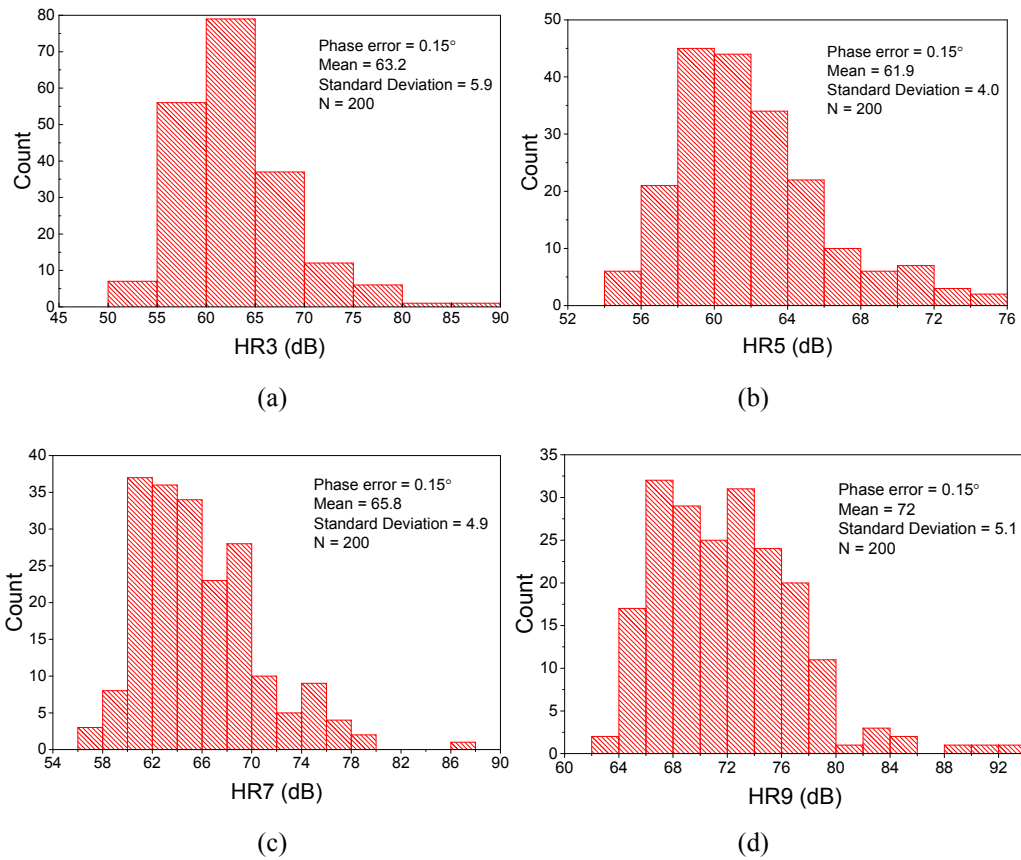


Fig. 8. Monte Carlo simulation results of (a) HR3, (b) HR5, (c) HR7, and (d) HR9 including 0.15° phase error at the 111 MHz effective LO.

This g_m -based 2-stage HR circuit has $\sim 0.1\%$ drain current mismatch due to g_m scaling according to Monte Carlo simulation. Derived from (1) and (2), the estimated 3σ worst-case HR3 and HR5 are supposed to be 63.8 and 61.5 dB, which are ~ 7 dB higher than the Monte Carlo simulation results shown in Fig. 6. These discrepancies result from unaccounted mismatch sources other than g_m scaling mismatch, such as mixer switches and loads.

Figure 7 shows the effects of process corners and phase error in HR ratios. Figure 7(a) demonstrates that the worst-case HR ratios maintain > 50 dB in nom (27 °C), slow (120 °C), and fast (-40 °C) corners. In Fig. 7(b), the

worst-case HR ratios are still better than 50 dB even with 0.3° phase error. The phase error is generated by phase shifts of the LO signal. The Monte Carlo simulation results assuming phase error of 0.15° are plotted in Fig. 8, where the worst-case HR3 of 53.6 and HR5 of 55 dB are achieved.

The wideband HR ratios of the proposed HRM are shown in Fig. 9. The RF signal at 115 MHz is down-converted to 4 MHz by the 111 MHz effective LO and the third RF interference at 335 MHz is down-converted to 2 MHz by the third LO harmonic. The third to ninth RF interferences at low frequency bands (54–95 MHz) are also down-converted to in-band by LO harmonics, thus HR3 to

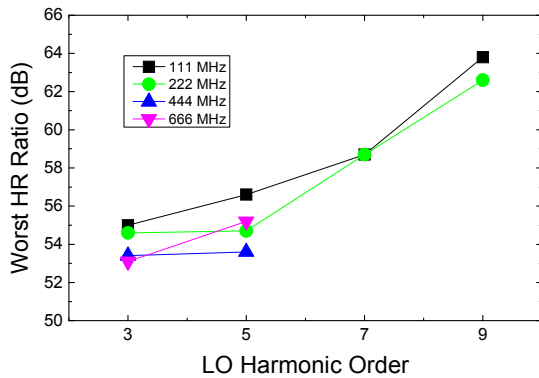


Fig. 9. Worst-case HR3–9 with third to ninth RF interferences.

	12-phase HRM	8-phase HRM	This Work
Architecture	12-phase 1-stage	8-phase 2-stage	12-phase 2-stage
Weighting ratios	{0:15:26:30 :26:15}	{2:3:2}/ {5:7:5}	{3:5:6:5:3}/ {4:7:8:7:4}
DSB NF (dB)	10.3	10.5	11
Voltage gain (dB)	22.7	41.5	40.3
IIP3 (dBm)	−1.5	+0.6	−0.5
HR3, 5, 7, 9 (dB)	52/52/56/61	56/59/17/21	56/55/58/62
Power (mW)	4.7	11.75	16.25

Tab. 2. Performance summary and comparison.

HR9 are reported. The effective LO frequency is varied from 111 to 666 MHz. The worst-case HR3 is maintained greater than 53 dB.

The HRM performances are summarized and compared in Tab. 2. Worst-case HR ratios from Monte Carlo simulations (200 runs) are reported in Tab. 2. The device size for the biggest factor 30 in the 1-stage HRM is $W/L = 75 \mu\text{m}/1.2 \mu\text{m}$, which is the same size as the factor 6 in the proposed HRM. The 2-stage harmonic mixing improves HR3 by 4 dB compared to 1-stage harmonic mixing. Compared to the 8-phase HRM, the proposed 12-phase HRM achieves almost 40 dB improvement on HR7 and HR9, while maintaining comparable voltage gain and IIP3. Under a 2.5 V supply, the 8-phase and proposed 12-phase HRMs consumed 11.75 and 16.25 mW, respectively. Although the 12-phase HRM requires more power consumption compared to the 8-phase HRM, it can reject odd harmonics up to the ninth order.

4. Conclusion

A 12-phase HRM using the 2-stage g_m -based HR circuit is presented for the TV tuner bands in order to suppress unwanted odd LO harmonics. Unlike conventional 8-phase HR schemes, the proposed 12-phase 2-stage HR scheme extends the maximum order of HR from the fifth order to the ninth order harmonic with small weighting factors, and rejects the third to the ninth LO harmonics between 55 to 62 dB without calibration. Although our

scheme was demonstrated on the g_m scaling scheme, it can be also applied to other resistor weighting schemes with transimpedance amplifiers (TIAs).

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References

- [1] CHEN, C., WU, J., HUANG, C., et al. A CMOS switched load harmonic rejection mixer for DTV tuner application. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2013, vol. 60, no. 2, p. 428–436. DOI: 10.1109/TCSI.2012.2215695
- [2] WELDON, J., NARAYANASWAMI, R., RUDELL, J., et al. A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers. *IEEE Journal of Solid-State Circuits*, 2001, vol. 36, no. 12, p. 2003–2015. DOI: 10.1109/4.972151
- [3] LERSTAVEESIN, S., GUPTA, M., KANG, D., et al. A 48–860 MHz CMOS low-IF direct-conversion DTV tuner. *IEEE Journal of Solid-State Circuits*, 2008, vol. 43, no. 9, p. 2013–2024. DOI: 10.1109/JSSC.2008.2001900
- [4] ANDREWS, C., DIAMANTE, L., YANG, D., et al. A wideband receiver with resonant multi-phase LO and current reuse harmonic rejection baseband. *IEEE Journal of Solid-State Circuits*, 2013, vol. 48, no. 5, p. 1188–1198. DOI: 10.1109/JSSC.2013.2254535
- [5] RU, Z., MOSELEY, N., KLUMPERINK, E., et al. Digitally enhanced software-defined radio receiver robust to out-of-band interference. *IEEE Journal of Solid-State Circuits*, 2009, vol. 44, no. 12, p. 3359–3375. DOI: 10.1109/JSSC.2009.2032272
- [6] LIN, F., MAK, P.-I., MARTINS, R. An RF-to-BB-current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF. *IEEE Journal of Solid-State Circuits*, 2014, vol. 49, no. 11, p. 2547–2559. DOI: 10.1109/JSSC.2014.2354647
- [7] RAFI, A. A., VISWANATHAN, T.R. Harmonic rejection mixing techniques using clock-gating. *IEEE Journal of Solid-State Circuits*, 2013, vol. 48, no. 8, p. 1862–1874. DOI: 10.1109/JSSC.2013.2259032
- [8] PULLELA, R., SOWLATI, T., ROZENBLIT, D. Low flicker-noise quadrature mixer topology. In *IEEE International Solid-State Circuits Conference, ISSCC Digest of Technical Papers*. San Francisco (USA), 2006, p.1870–1879. DOI: 10.1109/ISSCC.2006.1696244
- [9] LEE, D., LEE, M. Low flicker noise, odd-phase master LO active mixer using a low switching frequency scheme. *IEEE Journal of Solid-State Circuits*, 2015, vol. 50, no. 10, p. 2281–2293. DOI: 10.1109/JSSC.2015.2449556

About the Authors ...

Dongju LEE was born in 1983. He received his M.S. degree from Gwangju Institute of Science and Technology

(GIST), Gwangju, in 2008. He is currently working towards the Ph.D. degree at GIST. His research interests include analog and RF IC designs for multiband and multi-mode wireless receivers.

Hocheol JEONG was born in 1988. He received the B.S. degree in Electronic and Radio Wave Engineering from Kyunghee University (KHU), Suwon, Korea in 2014, the M.S. degree from GIST, Gwangju, Korea in 2016. He is currently working toward the Ph.D. degree at GIST. His research areas are analog and RF IC design for wireless applications.

Minjae LEE was born in 1976. He received his B.Sc. and M.S. degrees both in Electrical Engineering from Seoul National University, Seoul, Korea in 1998 and 2000 respectively. He received the Ph.D. degree in Electrical Engi-

neering from the University of California, Los Angeles, in 2008. In 2000, he was a consultant with GCT semiconductor, Inc., and Silicon Image Inc., designing analog circuits for wireless communication and digital signal processing blocks for Gigabit Ethernet. He joined Silicon Image Inc., Sunnyvale, CA in 2001, developing Serial ATA products. In August 2008, he joined Agilent Technologies in Santa Clara, CA, where he was involved with the development of next generation high-speed ADCs and DACs. Since 2012, he has been with the School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju, Korea, where he is now an Assistant Professor. He was the recipient of the 2007 Best Student Paper Award at the VLSI Circuits Symposium in Kyoto, Japan. He received the 2015 Distinguished Lecture Award in Gwangju Institute of Science and Technology.