Triangle/Square Waveform Generator Using Area Efficient Hysteresis Comparator

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Abstract. *A function generator generating both square and triangle waveforms is proposed. The generator employs only one low area comparator with accurate hysteresis set by a bias current and a resistor. Oscillation frequency and its non-idealities are analyzed. The function of the proposed circuit is demonstrated on a design of 1 MHz oscillator in STMicroelectronics 180 nm BCD technology. The designed circuit is thoroughly simulated including trimming evaluation. It consumes 4.1 µA at 1.8 V and takes 0.0126 mm^2 of silicon area. The temperature variation from −40 °C to 125 °C is ±1.5 % and the temperature coefficient is 127 ppm/°C.*

Keywords

Function generator, triangle and square wave generator, hysteresis comparator

1. Introduction

Relaxation oscillator circuits are present in almost every electronic application such as microcontrollers, DC-DC converters or RFID chips. With increasing demand for small form surface mount packages silicon area of every block can have an impact on whether the final design fits into the package or not. Recently several architectures with low silicon area have been proposed. In [1] a capacitor is linearly charged and the threshold is compared with a current-mode comparator. In [2] a voltage on an exponentially charged capacitor is compared with a hysteresis comparator. However, for some applications, such as DC-DC converters [3], a triangular waveform may be required.

The conventional approach to generation of such a waveform is depicted in Fig. 1. A capacitor is charged with a constant current of alternating orientation generated by a current source (CS) between two voltage levels V_{lo} and V_{hi}. This solution requires two comparators. Instead of two comparators another solutions may employ single comparator with a hysteresis. In [4] a CMOS Schmitt trigger is used.

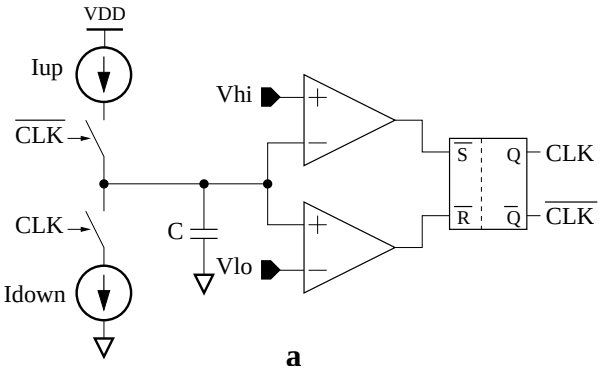

Fig. 1. Conventional triangle oscillator.

The main drawback of such a circuit is that the hysteresis and the frequency are sensitive to PVT variations.

To address this issue, the solution in [5] uses a comparator with a hysteresis set by an external resistor network. In [6] the hysteresis is set with a resistor and a saturation current of an OTA. In [7] two OTAs are used to form a Schmitt trigger and another OTA is used as an integrator. These solutions require either comparator or OTA with a differential input stage.

Another class of generators is based on the so-called modern functional blocks. In [8] two second-generation current conveyors (CCII) are used for square/triangular generation. A current mode generator is presented in [9] using two multiple-output current controlled current differencing transconductance amplifiers (MO-CCCDTA). Another voltage mode solution uses two differential voltage current conveyors (DVCC) in [10]. A differential output generation was presented in [11] using dual output and fully balanced voltage differencing buffered amplifiers (DO-VDBA and FB-VDBA, respectively). Solutions in [12] and [13] employ single Z-copy controlled gain voltage differencing current conveyors (ZC-CG-VDCC) for voltage/current output functional generator. All these designs require complex functional blocks that take a lot of silicon area. The overview of the mentioned architectures can be seen in Tab. 1.

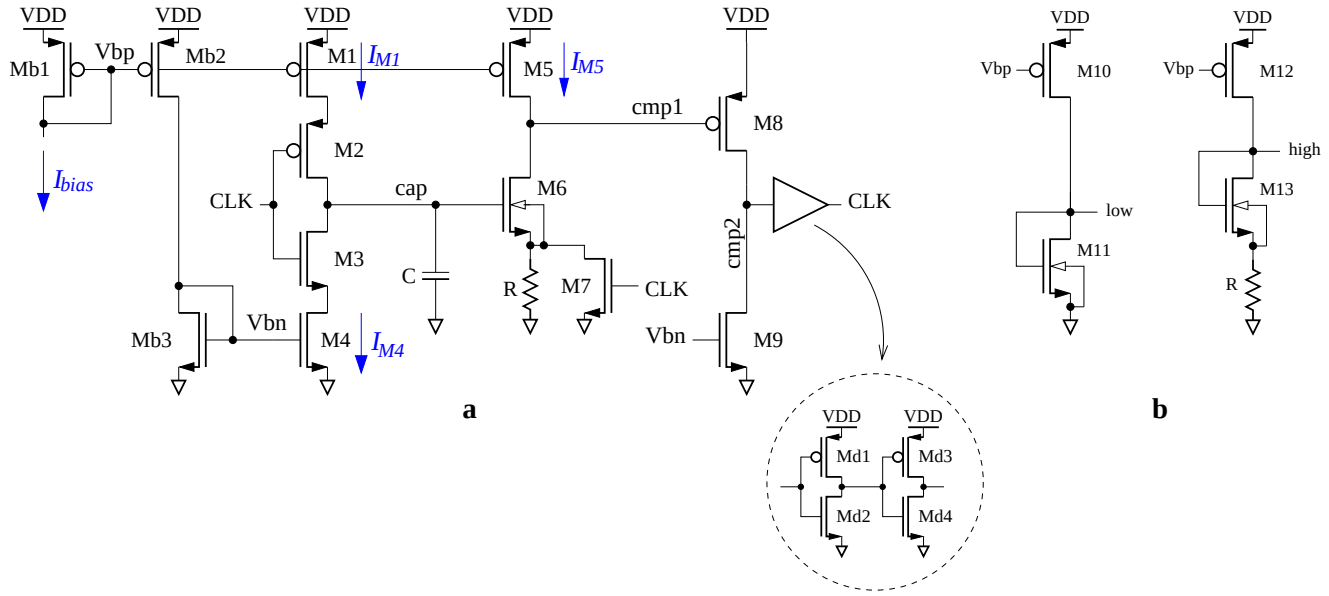

Fig. 2. Proposed circuit: (a) Waveform generator, (b) reference generators (when not explicitly shown the bulks are tied to V_{DD} or ground for PMOS and NMOS, respectively).

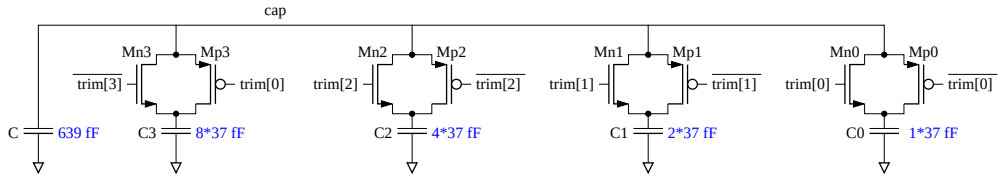

Fig. 3. Trimming circuit.

Reference	Number of passive elements	Number of transistors	Architecture	Type of out. sig. (Voltage/Current)
[4]	1	19	CS + CMOS Schmitt trig.	Volt.
[5]	4	N/A	CS + Opamp	Volt.
[6]	2	15	CS + OTA	Volt.
[7]	3	N/A	3× OTA	Volt.
[8]	4	N/A	2× CCII	Volt.
[9]	1	58	2× MO-CCCDTA	Cur.
[10]	4	N/A	2× DVCC	Volt.
[11]	3	24	DO-VDBA + FB-VDBA	Volt.
[12]	3	52	ZC-CG-VDCC	Both
[13]	1	N/A	ZC-CG-VDCC	Both
Fig. 2a	2	20	CS + single input comp.	Volt.

Tab. 1. Comparison of selected architectures.

In this article a new triangular relaxation oscillator is proposed. This circuit requires only one single ended comparator and therefore saves both silicon area and power consumption. Section 2 described operation of the proposed circuit and analyses its oscillation frequency, design of a 1 MHz relaxation oscillator can be found in Sec. 3 and its simulation results are presented in Sec. 4, conclusion follows in Sec. 4.

2. Circuit Analysis

The schematic of the proposed waveform generator is in Fig. 2a. Transistors M_1 and M_4 work as current sources with M_{2-3} as switches controlling charging and discharging of the capacitor C. For symmetrical waveform both current must be equal. Hysteresis comparator is composed of transistors M_{5-9}. M_6 together with R work as $V \rightarrow I$ converter whose output current is compared to I_{M5} produced by M_5. M_8 and M_9 then form a second stage of the comparator whose output is further amplified by a digital CMOS buffer. Hysteresis is created by shorting the resistor by M_7. If the bulk of M_6 is shorted to the source the body effect is avoided and the two threshold voltages are (assuming high gain in the first stage of the comparator):

$$V_{\text{low}} = V_{gs6}|_{I_{M5}}, \tag{1}$$

$$V_{\text{high}} = V_{gs6}|_{I_{M5}} + R\, I_{M5}. \tag{2}$$

Absolute value of the two voltages is dependent on the gate-source voltage of M_6 but the difference depends only on the current in the first stage of the comparator and the resistor value.

Some applications (e.g. DC-DC converters) may require reference voltages corresponding to the comparator thresholds. These can be extracted with the circuits depicted in Fig. 2b. M_{11} is sized to have the same current density as

M_6 so that $V_{gs11} = V_{gs6} = V_{\text{low}}$. Similarly, if $I_{M12} = I_{M5}$ and M_{13} is the same size as M_6 then the voltage on the drain of M_{13} corresponds to V_{high}. By the same principle, if needed, setting the resistor value between 0 and R (resistor value in the oscillator) can generate any voltage within the oscillator output voltage range.

Due to the delay of the comparator the capacitor voltage v_{cap} overshoots the threshold V_{high} by $\text{SR}^+ t_d^+$, where SR^+ is the positive slew rate on the capacitor given by $\frac{I_{M1}}{C}$ and t_d^+ if the rising propagation delay of the comparator. Similarly for the opposite phase v_{cap} undershoots V_{low} by $\text{SR}^- t_d^-$, SR^- being negative slew rate given by $\frac{I_{M4}}{C}$ and t_d^- being falling propagation delay. The rising and falling half-periods are

$$T^{+/-} = \frac{(V_{\text{high}} + \text{SR}^+ t_d^+) - (V_{\text{low}} - \text{SR}^- t_d^-)}{\text{SR}^{+/-}}. \tag{3}$$

Substituting (1) and (2) into (3) and summing both half-periods we get for a symmetrical waveform ($\text{SR}^+ = \text{SR}^-$) the following oscillation period

$$T = 2\left(RC\frac{I_{M5}}{I_{M1}} + t_d^+ + t_d^-\right). \tag{4}$$

The frequency of oscillation is therefore dependent on the product of R and C as is the temperature dependence. The effect of the comparator delay can be compensated by increasing the value of C.

The comparator delay portion of the oscillation period is dominated by t_d^- caused mostly by slewing of the *cmp1* node from saturation voltage of M_6 V_{ds6}^{sat} to the threshold of the second stage give by $V_{\text{DD}} - |V_{\text{THP}}|$, where V_{THP} is the threshold voltage of PMOS transistor M_8. This delay t_{slew} can be estimated as follows. Slewing starts when the input voltage of the comparator crosses threshold V_{low}. Around this operating point M_6 can be approximated by a corresponding transconductance g_{m6} that is charging a parasitic capacitance C_p of node *cmp1*. As the voltage on the capacitor v_{cap} continues to linearly decrease so does the current charging C_p given by $g_{m6} v_{\text{cap}}$. The slewing time can be computed by the following integral

$$\begin{aligned} V_{\text{DD}} - |V_{\text{THP}}| - V_{ds6}^{\text{sat}} &= \int_0^{t_{\text{slew}}} \frac{g_{m6} v_{\text{cap}}}{C_p} \mathrm{d}t \\ &= \int_0^{t_{\text{slew}}} \frac{g_{m6} \text{SR}^- t}{C_p} \mathrm{d}t. \end{aligned} \tag{5}$$

Solving for t_{slew} leads to

$$t_d^- \approx t_{\text{slew}} = \sqrt{\frac{2(V_{DD} - |V_{\text{THP}}| - V_{ds6}^{\text{sat}}) C_p}{g_{m6} \text{SR}^-}}. \tag{6}$$

Equation (6) shows that to decrease the slewing delay of the comparator the parasitic capacitance C_p must be minimized and the transconductance g_{m6} must be maximized. The former can be done by minimizing M_8 for lower gate capacitance, the latter by increasing drain current of M_6 which is given by I_{M5}.

3. Design

The proposed waveform generator with 1 MHz frequency was designed in STMicroelectronics 180 nm BCD technology with supply voltage of 1.8 V. Values of the passive components were selected to be easily integrated on-chip: $R = 500\,\text{k}\Omega$, $C = 1\,\text{pF}$. For good linearity a MOM (Metal-Oxide-Metal) capacitor was selected together with N+ polysilicon resistor for good temperature behavior.

Since the on-chip resistors and capacitors have large process variations trimming is usually employed to put the resultant frequency within a given specification. This can be accomplished by trimming either the resistor or the capacitor. The drawback of the resistor trimming is a change of triangle amplitude with trimming code. This may not be an issue when only a digital output is used but may pose a problem for subsequent processing when the triangular output is used as well, e.g. in DC-DC converters. For this reason the capacitor trimming was selected and the trimming circuit can be found in Fig. 3. The main capacitor C is accompanied with four binary scaled capacitor $C_0 - C_4$ which can be switched parallel to the main capacitor using transfer gates controlled by trimming bits. The unit capacitance of the trimming capacitors and therefore the trimming range was selected according to the technology spread of the oscillation period and is about ±30 %. The remaining value of the main capacitor C was then reduced by the parasitic capacitances of the transistors connected to the *cap* node, e.g. drain/source capacitances of M_{n0-3}, M_{p0-3}, M_2, M_3 or gate capacitance of M_6. This correction makes 65 fF.

Component	Width / Length
M_{b1}, M_{b2}, M_1, M_5, M_{10}, M_{12}	2 µm / 2 µm
M_{b3}, M_4, M_9	1 µm / 4 µm
M_2	2 µm / 0.18 µm
M_3	1 µm / 0.18 µm
M_6, M_{11}, M_{13}	2 µm / 0.56 µm
M_7	1 µm / 0.18 µm
M_8, M_{d1}, M_{d3}	1 µm / 0.24 µm
M_{d2}, M_{d4}	0.7 µm / 0.24 µm
M_{n0-3}	0.7 µm / 0.18 µm
M_{p0-3}	1 µm / 0.18 µm

Tab. 2. Transistor dimensions.

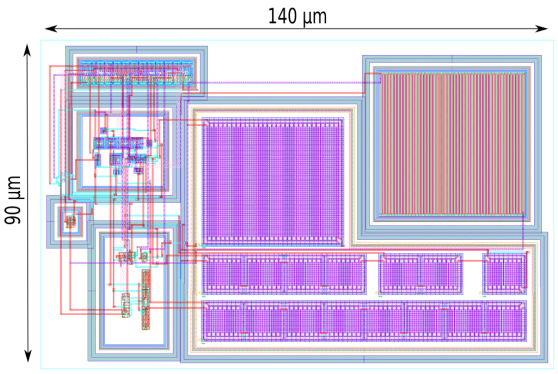

Fig. 4. Layout.

The typical bias current as well as all the branch current through M_{b1}, M_{b2}, M_1 or M_5 is 1 µA. In order to stabilize the amplitude of the triangle waveform the bias current should have inverse temperature and process dependency as the resistor R. This is not a problem as the bias current I_{bias} distributed across the chip is usually derived from a trimmed bandgap voltage V_{bg} and a reference resistor R_{bias} as $I_{\text{bias}} = V_{\text{bg}}/R_{\text{bias}}$. If R_{bias} is the same resistor type as R then the triangle waveform amplitude is a scaled copy of the bandgap voltage.

The transistor dimensions are summarized in Tab. 2. The gate lengths of the transistors operating as switches were kept at minimum of the given technology at 180 nm. However, the transistors operating as current sources have gate lengths in the order of micro meters for high output resistance and good matching. The former has impact on the triangular waveform linearity and the latter on statistical duty cycle variations.

Figure 4 shows a layout of the proposed circuit (excluding reference generators of Fig. 2b). The circuit takes 0.0126 mm^2 out of which the largest part is taken by the capacitors and the resistor.

4. Simulation Results

The designed circuit has been simulated in Eldo simulator from Mentor Graphics. The bias current was derived from a constant voltage source and an N+ polysilicon resistor to simulate chip bias current behavior and to stabilize amplitude of the triangle waveform across corners and temperature. The simulated transient waveforms of the main circuit including the reference generators are depicted in Fig. 5. It can be seen that the triangular waveform generated on the *cap* node exceeds the ideal boundaries given by the reference voltages V_{low} and V_{high} (waveforms *low* and *high*). This is caused by the propagation delays of the comparator t_d^+ and t_d^- as discussed in Sec. 2. The origin of the propagation delays can be seen on the depicted waveforms of internal nodes of the comparator *cmp1* and *cmp2* which show slew rate limitation caused by the designed constant current of M_5 and M_9. The square waveform output *clk* is then produced by reshaping the signal on node *cmp2* by the digital CMOS buffer. The oscillating frequency for a typical corner is 0.94 MHz, read from the waveforms t_d^+ is 3 ns and t_d^- is 34 ns out of which t_{slew} is about 28 ns. We can compare this result with a theoretical value given by (6). Using (values from operating point analysis) V_{DD} = 1.8 V, $|V_{\text{THP}}|$ = 0.55 V, V_{ds6}^{sat} = 0.19 V, C_p = 4.9 fF, g_{m6} = 18 µS and SR$^-$ = 1 V/µs we get theoretical value of t_{slew} equal to 24 ns which is in good agreement with the simulated value.

The average current consumption of the generator core (w/o ref. gens. on Fig. 2b) is 4.1 µA. This is equivalent to 7.38 µW at the respective supply voltage.

In order to evaluate process spread of the circuit a Monte Carlo (MC) analysis was run on top of the transient simulation. Further to assess the effectiveness of the trimming method a transient sweep across all the trimming steps was simulated in each MC run and the value closest to the target value (i.e. 1 MHz in this case) was selected. This in fact simulates a real factory trimming.

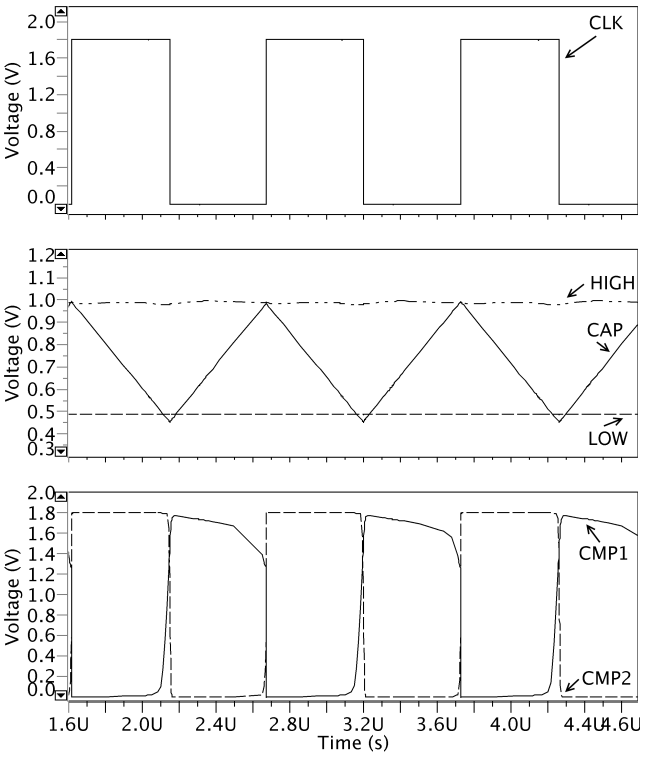

Fig. 5. Simulation results.

Figures 6 and 7 shows histograms and statistical parameters of 500 runs of MC analysis. Results of oscillation frequency before trimming can be seen in Fig. 6a. The maximum deviation from the nominal frequency is 26 % and is caused by the process variability of sheet capacitance and sheet resistance in the given technology process. Figure 6b shows histogram of frequency after trimming. The maximum deviation is now 4.27 % from the nominal frequency. Duty-cycle variation histogram is in Fig. 6c and its standard deviation is 0.82 %. This statistical variation of the duty-cycle is caused by the mismatches of current mirrors $M_{b3} - M_4$ and $M_{b2} - M_1$ and can be improved by enlarging the area of the transistors [14].

Figure 7 shows histogram of the peak-to-peak amplitude of the triangle waveform. As described above, the bias current was assumed to be derived from an ideal bandgap voltage reference and the same resistor type as resistor R. The amplitude of the triangle waveform is thus not affected by the process spread of the resistor (which is around ±20 %) and is given mostly by the mismatches of M_{b1}, M_5 and R.

Variation of the oscillation frequency with temperature can be see in Fig. 8. For the extended temperature range spanning from −40 °C to 125 °C the total frequency variation is ±1.05 % and the temperature coefficient is therefore 127 ppm/°C.

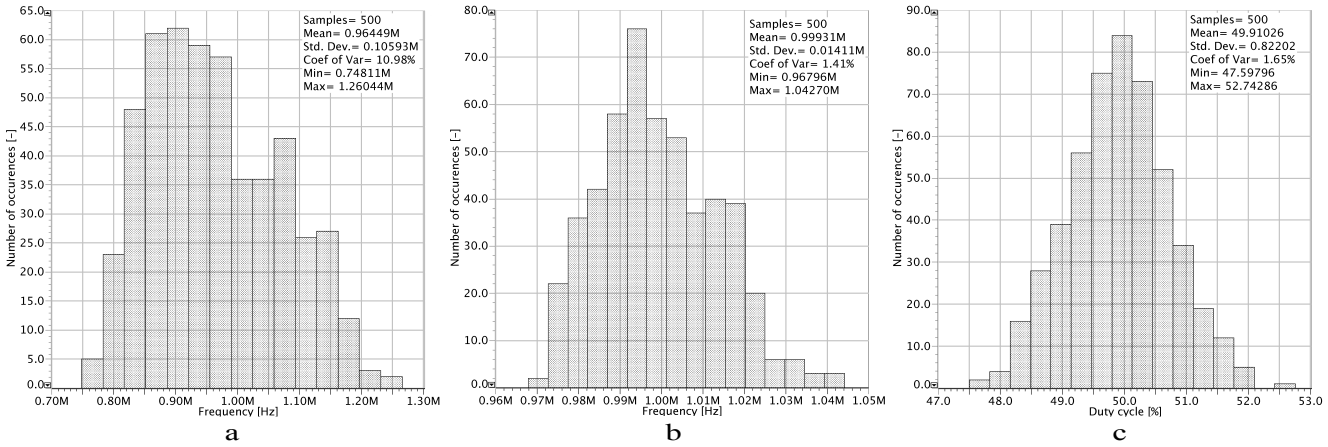

Fig. 6. Monte Carlo analysis histograms: (a) Frequency before trimming, (b) frequency after trimming, (c) duty cycle.

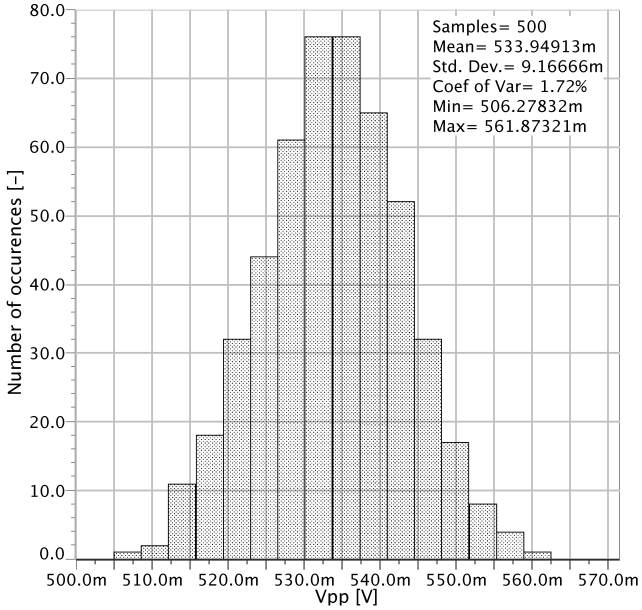

Fig. 7. Triangle waveform peak-to-peak histogram.

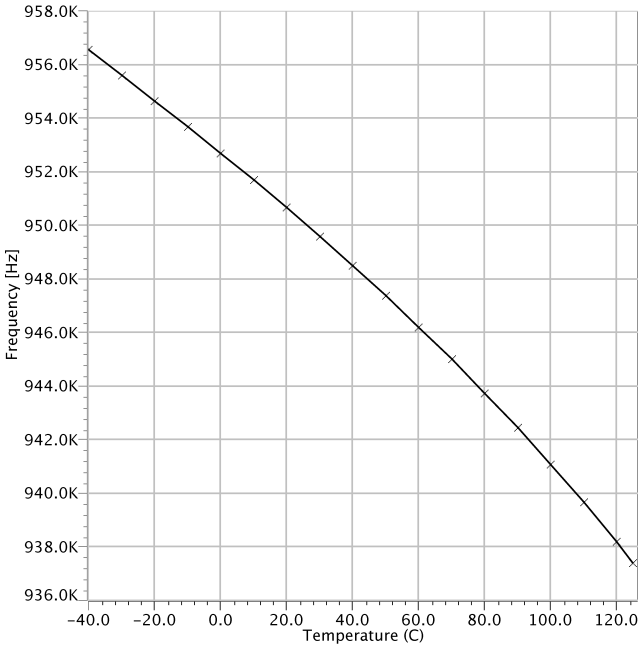

Fig. 8. Frequency temperature variation.

5. Conclusion

A new area efficient circuit generating triangular waveform was proposed. Oscillating period together with the major source of error caused by the propagation delay of the comparator was derived. A 1-MHz waveform generator based on the proposed topology was designed in STMicroelectronics 180-nm BCD technology consuming 7.38 µW and occupying only 0.0126 mm^2. The temperature and process stability of the oscillation frequency depends on the resistors and capacitors available in the given technology. The type of these elements can be selected to at least partially compensate for the temperature behavior of each other. In the presented design a temperature coefficient of 127 ppm/°C was achieved. To cope with the process spread a trimming is usually employed as was demonstrated. The proposed topology can be used as a general purpose square wave generator or as a triangular generator in DC-DC converters.

Acknowledgments

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