VLSI Implementation of Fixed-Point Lattice Wave Digital Filters for Increased Sampling Rate

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Abstract. *Low complexity and high speed are the key requirements of the digital filters. These filters can be realized using allpass filters. In this paper, design and minimum multiplier implementation of a fixed point lattice wave digital filter (WDF) based on three port parallel adaptor allpass structure is proposed. Here, the second-order allpass sections are implemented with three port parallel adaptor allpass structures. A design-level area optimization is done by converting constant multipliers into shifts and adds using canonical signed digit (CSD) techniques. The proposed implementation reduces the latency of the critical loop by reducing the number of components (adders and multipliers). Three design examples are included to analyze the effectiveness of the proposed approach. These are implemented in verilog HDL language and mapped to a standard cell library in a 0.18 μm CMOS process. The functionality of the implementations have been verified by applying number of different input vectors. Results and simulations demonstrate that the proposed design method leads to an efficient lattice WDF in terms of maximum sampling frequency. The cost to pay is small area overhead. The postlayout simulations have been done by HSPICE with CMOS transistors*

Keywords

VLSI implementation, lattice wave digital filters, three port adaptor, canonical signed digit coefficient, fixed-point arithmetic

1. Introduction

Wave digital filters constitute a wide class of infinite impulse response (IIR) digital filters that transform an analog network into a topological equivalent digital filter [1]. These filters find applications in a wide variety of areas such as communication, control, biomedical engineering, audio processing and others. A major advantage of WDFs over most of other recursive filters is that they can inherit the fundamental properties such as low coefficient sensitivity and stability under finite-arithmetic conditions [2]. Therefore, these are very attractive for Very Large Scale Integration

(VLSI) implementation. In these filters, silicon area, computational complexity, power consumption, and maximum achievable sampling rate are highly dependent on coefficient word length [3]. Therefore, the word length should be as short as possible, but must be sufficient to satisfy the given filter specifications [2]. Many researchers have investigated WDFs that demand low power consumption and high speed, etc., however the toughest challenge is the implementation. The VLSI implementation of WDFs using symmetric two port adaptor structure is represented in [3], [4]. In [5], the bit level systolic array method is used to increase the sampling rate to design unit element WDF and a lattice WDF using the same specifications. The systolic hardware architecture of the two filters is compared to the expected values of the integrated circuit parameters. Another method which is used to achieve significant increase in sampling rate of WDFs is most significant bit first arithmetic [6]. However, all the filters mentioned above are based on conventional two port adaptor structures also known as Richards' allpass structure. Although M.S. Anderson et al. have compared two port and three port series adaptor realizations of second-order allpass section but VLSI implementation is not done [7]. In [8], we have proposed the VLSI implementation of lattice WDF using three port series adaptor allpass structure which provides improved maximum sampling frequency compared to Richards' allpass structure based WDFs.

In this paper, we have replaced conventional Richards' allpass structures with three port parallel adaptor allpass structures using bit parallel arithmetic to improve the maximum sampling rate. To increase maximum sampling frequency, the latency can be reduced by using low-sensitivity filters, resulting in short coefficients (low-latency multiplications) and by removing unnecessary operations in the critical loop via numerical equivalent transformations [9]. However, in this work, we have mainly concerned with minimizing the critical loop latency. It is minimized by reducing the number of logic components in the critical loop. Three port parallel adaptor allpass structures can be realized with adders, delays and multipliers [9], [10]. The adaptor coefficients are quantized in fixed-point arithmetic. A general multiplier element is very costly in full-custom VLSI implementation. To solve this problem, the multiplication of a data sample

by a filter coefficient value is carried out by using a sequence of shifts and adds and/or subtracts. For low power dissipation, the challenge is to implement the multiplier with minimum number of adders. For this purpose, it is attractive to use the canonical signed digit (CSD) representation. Therefore, using CSD coefficients, the hardware cost is reduced as well as speed is increased. The minimum number of nonzero bits are observed in CSD coefficients compared to other radix-2 representations. This reduces the number of adders/subtractors [11]. Multiple constant multiplication method is applied to implement CSD coefficients, which in turn again reduces the number of adders [9], [12].

To verify the results, VLSI implementation of lattice WDF of different orders is illustrated in Sec. 6. These filters are coded in verilog HDL language and mapped to a standard cell library in a 0.18 μm CMOS process. For the same specifications, these filters are implemented using conventional Richards' allpass as well as three port parallel adaptor allpass structures. This is enabled us to make a proper comparison between their corresponding hardware realizations. The implemented filters are simulated and tested by applying different input vectors. The comparison results show that the latter design is more efficient than the conventional design in terms of the maximum sampling rate at the cost of small area overhead.

The rest of the paper is organized as follows. Section 2 describes the lattice wave digital filters. Realization of allpass structures is presented in Sec. 3. In Sec. 4 the fixed point coefficient realization is explained. Section 5 explores the VLSI implementation. Three design examples of fixed point lattice wave digital filters using conventional Richards' allpass and three port parallel adaptors allpass structures are presented in Sec. 6. Comparative analysis of the different approaches is also given in Sec. 6. Section 7 concludes the paper.

2. Lattice Wave Digital Filters

An explicit class of wave digital filters are called lattice wave digital filter. It is well known that the lattice WDF structures have many attractive properties such as low coefficient sensitivity and consequently the low accuracy requirements for the register word length, higher dynamic range, higher overflow level, lower round-off noise, stability and good nonlinear properties under finite-arithmetic conditions where effects of rounding, truncation and overflow are present [2], [10], [13]. Lattice WDF structures find applications in lowpass-highpass filter, bandpass-bandstop filter, Hilbert transformers and quadrature mirror filters (QMF) realization [14], [15]. The resulting structures are found to have minimum hardware, highly modular and less sensitive, making them suitable for signal processors and VLSI implementation. The lattice WDF is represented by two parallel branches, which realize allpass filters. These allpass filters can be realized by using first- and/or second-order wave digital allpass sections. These
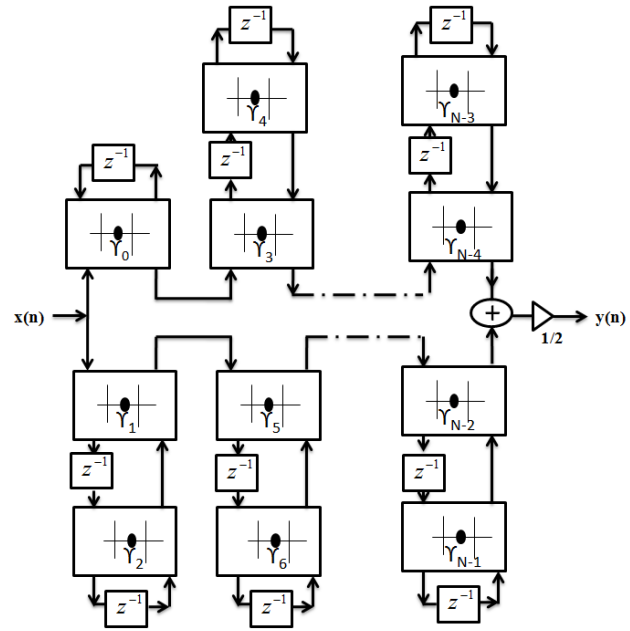

Fig. 1. Lattice wave digital filter realization of N order.

sections can be implemented using symmetric two port or three port networks known as adaptors in lattice WDF terminology and delay elements [16]. The signal flow graph of adaptor consists of multipliers and adders. The multipliers are the γ coefficients that characterize the lattice WDF. The signal flow graph of an Nth order lattice WDF is depicted in Fig. 1, where block z^{-1} represents the unit delay. For any order N there are $\frac{N+1}{2}$ stages and a maximum of N adaptors. The transfer function of a lattice WDF can be written as the sum of transfer function of two allpass branches

$$H(z) = \frac{H_0(z) + H_1(z)}{2} \tag{1}$$

where $H_0(z)$ and $H_1(z)$ are the transfer functions of stable allpass filters of orders M and N, respectively. In case of low pass filters, $M = N - 1$ or $M = N + 1$ so that $M + N$ order of overall $H(z)$ is odd. These filters can be realized in many different ways [17].

In this work, we only consider the cascade realization of the first- and second-order allpass sections. A first-order allpass section can be realized using Richards' structure, where a symmetric two port adaptor and a delay element are used [9]. The second-order allpass section can be realized using a cascade of two first-order Richards' allpass structures. A second-order allpass section is also realized using a three port parallel adaptor and two delay elements [1]. The detailed discussion of the first- and second-order allpass sections is given in Sec. 3. These allpass sections are recursive structures. Generally, recursive structures require a smaller number of arithmetic operations per sample than their nonrecursive counterparts. One limitation of the recursive structure is the maximum sampling frequency $f_{\max}$ at which a filter can operate [1]. The maximum sampling frequency for a recursive algorithm, described by a fully specified signal flow graph is [18]

$$f_{max} = \frac{1}{T_{min}} = \min\left\{\frac{N_i}{T_{tot}}\right\} \qquad (2)$$

where T_{min} is the minimum sampling time, T_{tot} is the total latency of the arithmetic operations and N_i is the number of delay elements in the directed loop i [18]. The loop(s) that determines the maximum sampling frequency is called the critical loop(s). The digital filters with high maximum sampling frequency are suitable candidates of low power and high speed applications. The reason is that if required sampling rate is less than the maximum sampling rate, the excess speed can be utilized to reduce the power consumption via power supply voltage scaling techniques [17], [18]. The area can be minimized by clever hardware design [19]. From (2), we observe two factors that are affecting the maximum sampling rate. The first factor is the number of delay elements in the critical loop and second is the total latency in the critical loop. The maximum sampling frequency can be increased by increasing the number of delay elements in the critical loop or by minimizing the critical loop latency. In this work, we have mainly concerned with minimizing the critical loop latency. It is minimized by reducing the number of logic components in the critical loop. It is further minimized by reducing the critical delay at logic level.

3. Realization of Allpass Structures

A lattice WDF, is realized by the two parallel allpass branches whose output are summed to produce the filter output. These allpass filters are replaced by the cascaded first- and second-order allpass sections implemented using either symmetric two port or three port parallel adaptor structures and delay elements. A first-order two port adaptor has a co-efficient value (γ) which controls the response of the allpass section. This adaptor requires a single multiplication and three additions each. Lattice WDFs use four types of symmetric two port adaptors as its building blocks depending on the value of γ coefficient. The signal flow graphs of four single multiplier symmetric two port configurations are shown in Fig. 2. These adaptor coefficients γ may be guaranteed to fall into the interval $-1 < \gamma < 1$ [13]. Methods to calculate these coefficients from the design specifications have been discussed in [13]. The different adaptor structure can be chosen depending on the value of γ coefficient as given in Tab. 1.

In these adaptor structures, the coefficient value of the actual multiplier (α) to be implemented is always positive and less than or equal to half, that is, $0 \leq \alpha \leq \frac{1}{2}$. To design allpass section from these adaptor structures, one port is terminated with the delay element. Generally, the transfer function of a first-order allpass section is given by

$$H(z) = \frac{t_0 + z^{-1}}{1 + t_0 z^{-1}} \qquad (3)$$

and for a second-order allpass section

$$H(z) = \frac{t_2 + t_1 z^{-1} + z^{-2}}{1 + t_1 z^{-1} + t_2 z^{-2}} \qquad (4)$$

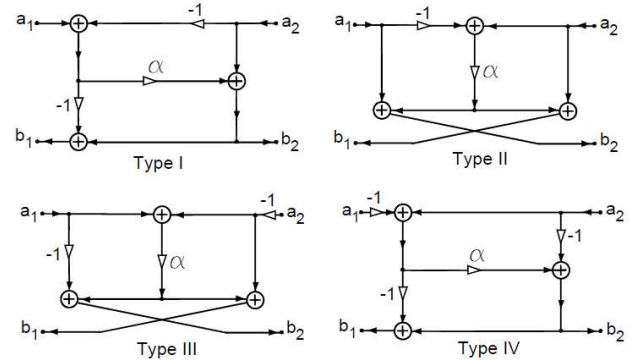| Adaptor type	γ range	α/γ conversion
Type I	$\frac{1}{2} < \gamma < 1$	$\alpha = 1 - \gamma$
Type II	$0 < \gamma \leq \frac{1}{2}$	$\alpha = \gamma$
Type III	$-\frac{1}{2} \leq \gamma < 0$	$\alpha = -\gamma$
Type IV	$-1 < \gamma < -\frac{1}{2}$	$\alpha = 1 + \gamma$

Tab. 1. Adaptor types.

Fig. 2. Signal flow graph of four symmetric two-port adaptor.

where $t_0 = -\gamma_0$, $t_1 = (\gamma_1 - 1)\gamma_2$ and $t_2 = -\gamma_1$ [13]. The first- and the second-order allpass sections realized using symmetric two port adaptors are called as Richards' allpass structure. Different symmetric two port adaptor structures can be chosen depending on the value of γ coefficient as given in Tab. 1. The second-order allpass sections are also realized using three port parallel adaptor and delays, called as three port parallel adaptor allpass structure.

3.1 Richards' Structures

First-order Richards' allpass structure is composed of the symmetric two-port adaptor and a delay element, as shown in Fig. 3. The signal flow graph of the conventional symmetric two-port adaptor forming the first-order Richards' allpass structure is described by the following equations

$$b_1 = \alpha(a_2 - a_1) + a_2, \qquad (5)$$
$$b_2 = \alpha(a_2 - a_1) + a_1 \qquad (6)$$

where a_1 and a_2 are the inputs and b_1 and b_2 are the outputs. The critical loop is shown by thick lines in Fig. 3. Since this critical loop has one multiplier, two adders and one delay element, the total latency T_{tot} is equal to $T_{m,\alpha} + 2T_a$, where $T_{m,\alpha}$ is the time delay for the multiplier and T_a is the adder delay [9], [19] and $N_i = 1$. Using (2), the maximum sampling frequency f_{max} of this structure is given by

$$f_{max} = \frac{1}{T_{m,\alpha} + 2T_a}. \qquad (7)$$

Similarly, the second-order Richards' allpass structure is cascade of the two first-order allpass structures and is shown in Fig. 4. Since this critical loop has two multipliers, four adders and one delay element, T_{tot} is equal to $T_{m,\alpha_1} + T_{m,\alpha_2} + 4T_a$, where, T_{m,α_1} and T_{m,α_2} are the time delays for the two multipliers and T_a is the adder delay [9] and $N_i = 1$. The f_{max} of this structure is given by

$$f_{max} = \frac{1}{T_{m,\alpha_1} + T_{m,\alpha_2} + 4T_a}. \qquad (8)$$

3.2 Three Port Parallel Adaptor Allpass Structure

A second-order three port parallel adaptor allpass structure is shown in Fig. 5. The transfer function of this section is given by [18]

$$H(z) = \frac{(1-\beta_1-\beta_2) + (\beta_1-\beta_2)z^{-1} - z^{-2}}{-1 + (\beta_1-\beta_2)z^{-1} + (1-\beta_1-\beta_2)z^{-2}} \qquad (9)$$

where β_1 and β_2 are the adaptor coefficients. Comparing with (4) we get the relationship between the adaptor coefficients to [18]

$$\beta_1 = \frac{(1-\gamma_1)(1+\gamma_2)}{2}, \quad \beta_2 = \frac{(\gamma_1-1)(\gamma_2-1)}{2}. \qquad (10)$$

It is observed from Fig. 5 that one of the two loops can be the critical loop. Assuming same number of fractional bits of β_1 and β_2, loop 1 has one multiplier, three adders and one delay element. While, loop 2 has one multiplier, four adders and one delay element. Since loop 2 contains more components, therefore, it is considered as the critical loop. The maximum sampling frequency of this structure is given by

$$f_{max} = \frac{1}{T_m + 4T_a}. \qquad (11)$$

We observe that the critical loop of the Richard's second-order allpass structure contains two multipliers and four adders as shown in Fig. 4. However, a three port parallel adaptor allpass structure contains only one multiplier and four adders. For the latter realization, the price to pay is somewhat longer coefficient wordlength to meet the filter specifications. However, it is found that the three port adaptor coefficients typically require one extra bit to match the performance of the two port realization for a given coefficient wordlength [7].
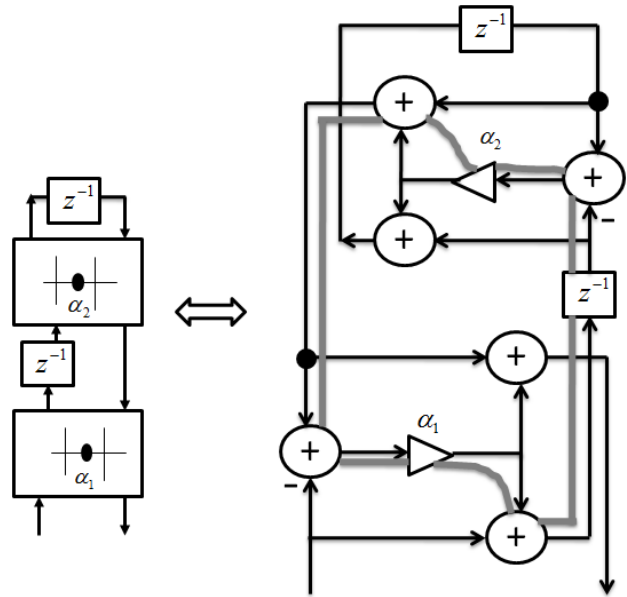

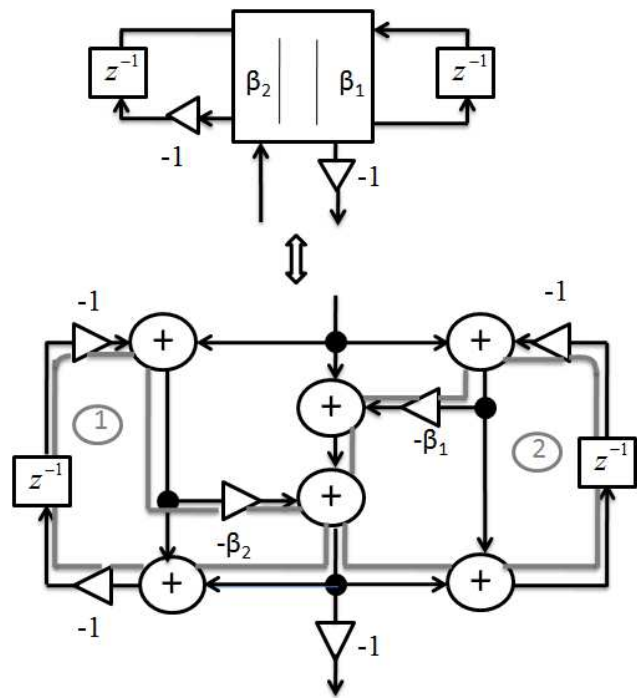**Fig. 3.** First-order Richards' allpass structure with critical loop.

Fig. 4. Second-order Richards' allpass structure with critical loop.

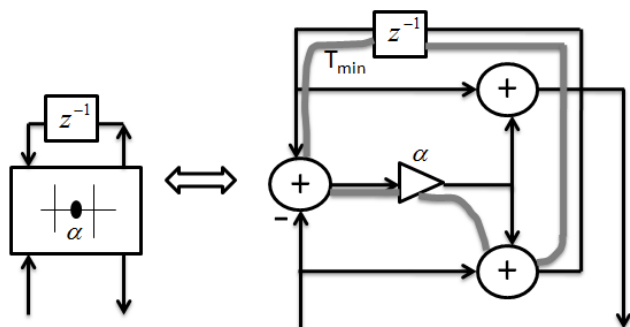**Fig. 5.** A three port parallel adaptor allpass structure.

4. Fixed-Point Coefficients

In this work, we concentrate on coefficient quantization in fixed point arithmetic. The goal of a fixed-point arithmetic is to maximize the filter performance and minimize finite-word-length effects [20–24]. It is desired that the coefficient values γ_k for $k = 0, 1, 2, \ldots, (M+N-1)$ are expressed as the following fixed-point binary numbers [10]

$$-x_0 + \sum_{r=1}^{T} x_r 2^{-r} \qquad (12)$$

where x_r for $r = 0, 1, \ldots, B$ is either 0 or 1. Here x_0 is the sign bit. For negative numbers sign bit is equal to one, whereas for non-negative numbers it is equal to zero. The goal is to express all the filter coefficient values in the above form with the minimum number of fractional bits B. For efficient multiplier implementation in full-custom VLSI implementation, the multiplication of a data sample by a filter coefficient value is carried out by using a sequence of shifts and adds and/or subtracts. In this case, it is desired to express the coefficient values in the following form

$$\sum_{r=1}^{R} x_r 2^{-P_r} \tag{13}$$

where each x_r is either 1 or -1 and the P_R's are nonnegative integers in the increasing order. The goal is to find all the coefficient values with minimum number of R, the number of power-of-two terms and the maximum number of shifts P_R is made as small as possible [10]. For this purpose, it is attractive to use the canonic-signed-digit (CSD) representation. This representation has three digits, -1, 0 and $+1$ as opposed to the two's-complement representation which has only two digits, 0 and $+1$ [10]. The number of adders and/ or subtractors required to realize a CSD coefficient is one less than the number of nonzero digits in this coefficient representation form [25].

5. VLSI Implementation

In this section, VLSI implementation of lattice WDF is presented. These filter structures are realized using adders, multipliers and delay elements. The multiplication of a data sample with each filter coefficient value is performed using a sequence of shift and add and/or subtract operations which is called as multiplierless implementation. Hence, the filters are implemented only with the adders and/or subtractors and delay elements. For minimum adder implementation the coefficients are realized in CSD representation. Steps followed for the implementation are given in Fig. 6 [26]. Mentor Graphics ASIC Design Kit (ADK) tools are used for IC flow, synthesis to standard cells and IC physical design and simulation.

6. Design Examples

To show the design process three examples of the lattice wave digital structure and their multiplierless implementation are presented. In these implementations Richards' and three port parallel adaptor allpass structures are used. The input samples wordlength is chosen as 8-bits. The coefficients wordlength is 9-bits and 10-bits for Richards' and three port parallel adaptor allpass sections, respectively. The performance of the two implementations are compared in terms of maximum sampling frequency and area.
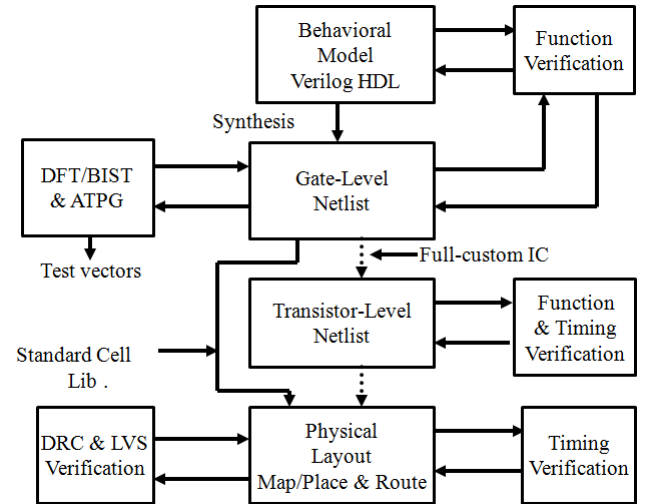

Fig. 6. Flow Diagram of VLSI Implementation.

Example 1:

Specifications of the Chebyshev low-pass lattice WDF are as follows [16, p. 12]: Sampling frequency $F = 16$ kHz, Passband edge frequency $f_p = 3.4$ kHz, Stopband edge frequency $f_s = 4.5$ kHz, Passband ripple $A_p = 0.5$ dB, Stopband attenuation $A_s = 50$ dB and Filter order $N = 9$. We see from Fig. 1 that 9th order lattice WDF is composed of one first- and four second-order allpass sections [9]. Its transfer function is given by

$$H(z) = \frac{1}{2} \left[\left(\frac{-0.66771 + z^{-1}}{1 - 0.66771 z^{-1}} \right) \left(\frac{0.61883 - 0.87844 z^{-1} + z^{-2}}{1 - 0.87844 z^{-1} + 0.61883 z^{-2}} \right) \right.$$
$$\left(\frac{0.91914 - 0.41780739 z^{-1} + z^{-2}}{1 - 0.41780739 z^{-1} + 0.91914 z^{-2}} \right) + \left(\frac{0.49630 - 1.19393 z^{-1} + z^{-2}}{1 - 1.19393 z^{-1} + 0.49630 z^{-2}} \right)$$
$$\left. \left(\frac{0.76628 - 0.57968 z^{-1} + z^{-2}}{1 - 0.57968 z^{-1} + 0.76628 z^{-2}} \right) \right]. \tag{14}$$

For multiplierless implementation of the lattice WDF, γ coefficients, adaptor type, α coefficients (for Richards' implementation), β coefficients (for three port parallel adaptor implementation) and their CSD representations are given in Tab. 2. For Richards' implementation, blocks of first- and second-order allpass sections are replaced with their equivalent signal flow graphs depicted in Fig. 3 and 4, respectively. The minimum sampling periods T_{min} of individual allpass sections are as follows

$$T_{min\alpha_0} = T_m + 2T_a,$$
$$T_{min\alpha_1\alpha_2} = 2T_m + 5T_a,$$
$$T_{min\alpha_3\alpha_4} = 2T_m + 5T_a, \tag{15}$$
$$T_{min\alpha_5\alpha_6} = 2T_m + 5T_a,$$
$$\text{and } T_{min\alpha_7\alpha_8} = 2T_m + 4T_a.$$

The minimum sampling period T_{min} of the overall filter, is given by

$$T_{min} = \max \left\{ T_{min\alpha_0}, T_{min\alpha_1,\alpha_2}, T_{min\alpha_3,\alpha_4}, T_{min\alpha_5,\alpha_6}, T_{min\alpha_7,\alpha_8} \right\}$$
$$= 2T_m + 5T_a. \tag{16}$$

$\gamma_i, 0 \le i \le 8$	Adaptor type	$\alpha_j, 0 \le j \le 8$	α_{CSD}	$\beta_k, 1 \le k \le 8$	β_{CSD}
0.667713527	1	0.33228647	0.01010101	–	–
−0.49630558	3	0.49630558	0.1000000$\bar{1}$	1.34511717	1.010100000
0.797917736	1	0.202082263	0.010$\bar{1}$0100	0.1511885	0.0010100$\bar{1}$0
−0.618835168	4	0.381164832	0.10$\bar{1}$00010	1.24864118	1.0100000$\bar{1}$0
0.542641521	1	0.457358479	0.100$\bar{1}$0101	0.370194	0.101000$\bar{1}$0
−0.766286584	4	0.233713416	0.01000$\bar{1}$00	1.17298493	1.010$\bar{1}$01000
0.328193215	2	0.328193215	0.01010100	0.5933016	0.1010$\bar{1}$0000
−0.919144204	4	0.080855796	0.00010101	1.1684758	1.010$\bar{1}$01$\bar{0}$10
0.217705053	2	0.217705053	0.0100$\bar{1}$000	0.7506684	1.0$\bar{1}$0000000

Tab. 2. Low-pass filter coefficients (Example 1).

The maximum sampling frequency f_{max} is given by

$$f_{max} = \frac{1}{T_{min}} = \frac{1}{2T_m + 5T_a}. \tag{17}$$

For multiplierless implementation, f_{max} is given by the following equation

$$f_{max} = \min\left\{\frac{1}{2T_a + 2T_a}, \frac{1}{3T_a + 5T_a}, \frac{1}{4T_a + 5T_a}, \frac{1}{3T_a + 5T_a},\right.$$
$$\left.\frac{1}{3T_a + 4T_a}\right\} = \frac{1}{9T_a}. \tag{18}$$

To implement a low-pass lattice WDF using three port parallel adaptors, blocks of second-order allpass sections are replaced with three port parallel adaptor allpass structures, shown in Fig. 5. Although, (α_0) is implemented with the Richards' first-order allpass structure. The f_{max} of the overall filter is determined by one of the critical loops of this allpass section. The f_{max} in terms of T_m and T_a for each of these allpass sections is same as given in (11). The multipliers are implemented with a network of shift and add and/or subtract operations using CSD coefficients. β coefficients and their CSD equivalents are given in Tab. 2. For the multiplierless implementation, f_{max} is given by

$$f_{max} = \min\left\{f_{max\alpha_0}, f_{max\beta_1\beta_2}, f_{max\beta_3\beta_4}, f_{max\beta_5\beta_6}, f_{max\beta_7\beta_8}\right\}$$
$$= \min\left\{\frac{1}{6T_a}, \frac{1}{6T_a}, \frac{1}{5T_a}, \frac{1}{6T_a}\right\} = \frac{1}{6T_a}. \tag{19}$$

Comparing equations (18) and (19), we observe that f_{max} is improved by approximately 49 % by reducing critical delay. The filters are implemented in CMOS VLSI design and results are summarized in Tab. 3. Here, f_{max} for three port adaptors allpass based lattice WDF is improved by 15 % compared to Richards' allpass based filter. However, the area is increased by 24 %.

	f_{max}	Area (mm^2)	Number of gates
Richards' allpass	58.5 MHz	2.952	2304
Three port adaptor allpass	67.6 MHZ	3.669	2887

Tab. 4. Comparison of f_{max} and area of low-pass lattice WDF based on Richards' and three port parallel adaptor structures (Example1).

Example 2:

Consider an elliptic low-pass lattice WDF with the following specifications [13]. $F = 16\,kHz$, $f_p = 3\,kHz$, $f_s = 5\,kHz$, $A_p = 1.0\,dB$, $A_s = 40\,dB$, Filter type = Chebyshev, and $N=5$. From Fig. 1, we observe that 5th order lattice WDF consists of one first- and two second-order allpass sections. For the above specifications, transfer function is given by

$$H(z) = \frac{1}{2}\left[\left(\frac{-0.6338 + z^{-1}}{1 - 0.6338z^{-1}}\right)\left(\frac{0.8260 - 0.68566z^{-1} + z^{-2}}{1 - 0.68566z^{-1} + 0.8260z^{-2}}\right)\right.$$
$$\left. + \left(\frac{0.5372 - 1.01532z^{-1} + z^{-2}}{1 - 1.0153z^{-1} + 0.5372z^{-2}}\right)\right]. \tag{20}$$

For multiplierless implementation of the lattice WDF, γ coefficients, adaptor type, α coefficients (for Richards' implementation), β coefficients (for three port parallel adaptor implementation) and their CSD representations are given in Tab. 4. For Richards' structure implementation, f_{max} is given by

$$f_{max} = \min\left\{\frac{1}{2T_a + 2T_a}, \frac{1}{4T_a + 5T_a}, \frac{1}{3T_a + 4T_a}\right\}$$
$$= \min\left\{\frac{1}{4T_a}, \frac{1}{9T_a}, \frac{1}{7T_a}\right\} = \frac{1}{9T_a}. \tag{21}$$

To implement the low-pass lattice WDF using three port parallel adaptors, the f_{max} in terms of T_m and T_a for each of these allpass sections, is same as given in (11). The β coefficients and their CSD equivalents are given in Tab. 4. For the multiplierless implementation, f_{max} is given as follows

$$f_{max} = \min\left\{f_{max\alpha_0}, f_{max\beta_1\beta_2}, f_{max\beta_3\beta_4}\right\}$$
$$= \min\left\{\frac{1}{4T_a}, \frac{1}{7T_a}, \frac{1}{6T_a}\right\} = \frac{1}{7T_a}. \tag{22}$$

Comparing equations (21) and (22) shows that f_{max} is improved by approximately 28.5 % by reducing critical loop delay. The filters are implemented in CMOS VLSI design to verify the results and are summarized in Tab. 5. Here, f_{max} for three port adaptors allpass based lattice WDF is improved by approximately 16.5 % compared to Richards' allpass based filter. However, the area is increased by 18 %.

$\gamma_i, 0 \leq i \leq 4$	Adaptor type	$\alpha_j, 0 \leq j \leq 4$	α_{CSD}	$\beta_k, 1 \leq k \leq 4$	β_{CSD}
0.6338	1	0.3662	0.10$\bar{1}$00010	–	–
−0.5372	4	0.4628	0.1000$\bar{1}$0$\bar{1}$	1.2762603	1.010010$\bar{1}$01
0.6605	1	0.3395	0.10$\bar{1}$0$\bar{1}$00$\bar{1}$	0.26093	0.010000$\bar{1}$0
−0.8360	4	0.1740	0.010$\bar{1}$0$\bar{1}$01	1.262709	1.010000100$\bar{1}$
0.3755	1	0.3755	0.10$\bar{1}$00000	0.573291	0.1001010$\bar{1}$

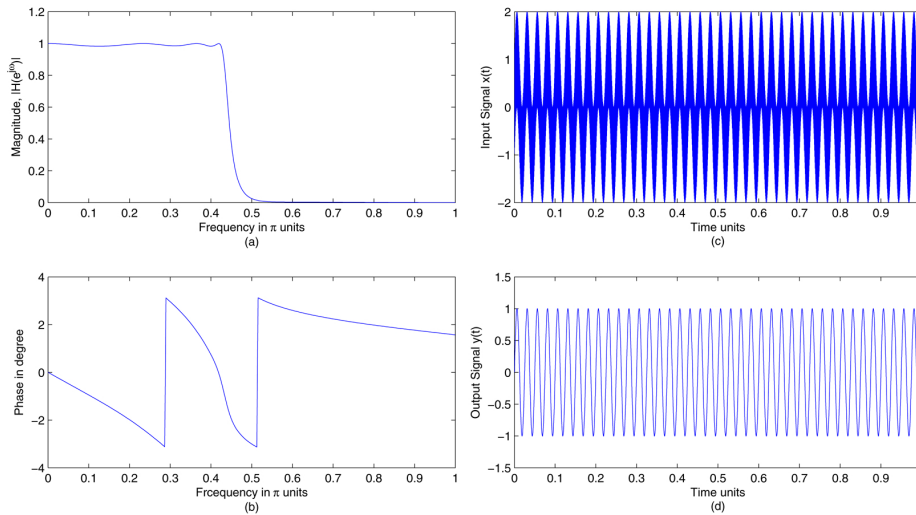**Tab. 3.** Coefficients of low-pass WDF filter (Example 2).

Fig. 7. Magnitude response (a), phase response (b), input signal (c), filtered output (d).

	f_{max}	Area (mm²)	Number of gates
Richards' allpass	70.0 MHz	1.934	1476
Three port adaptor allpass	81.6 MHZ	2.285	1698

Tab. 6. Comparison of f_{max} and area of low-pass lattice WDF (Example 2).

	f_{max}	Area (mm²)	Number of gates
Richards' allpass	63.1 MHz	2.472	1865
Three port adaptor allpass	71.3 MHz	2.966	2595

Tab. 7. Comparison of f_{max} and area of low-pass lattice WDF (Example 3).

Example 3:

Consider an elliptic low-pass lattice WDF with the following specifications [13]. $F = 16\,\text{kHz}$, $f_p = 3.4\,\text{kHz}$, $f_s = 4.6\,\text{kHz}$, $A_p = 0.2\,\text{dB}$, $A_s = 65\,\text{dB}$, Filter type= Cauer, and Filter order $N = 7$. From Fig. 1, we observed that the 7th order lattice WDF requires one first- and three second-order allpass sections. For given filter specifications, the transfer function is obtained as

$$H(z) = \frac{1}{2} \left[\left(\frac{-0.5190 + z^{-1}}{1 - 0.5190z^{-1}} \right) \left(\frac{0.66872 - 0.557752z^{-1} + z^{-2}}{1 - 0.55772z^{-1} + 0.66872z^{-2}} \right) \right.$$
$$\left. + \left(\frac{0.40441 - 0.853474z^{-1} + z^{-2}}{1 - 0.853474z^{-1} + 0.40441z^{-2}} \right) \left(\frac{0.89613 - 0.39193z^{-1} + z^{-2}}{1 - 0.39193z^{-1} + 0.89613z^{-2}} \right) \right].$$
$$(23)$$

The magnitude and phase response of the designed filter are depicted in Fig. 7(a) and 7(b). When an input signal $x(t) = \sin(80\pi t) + \sin(12000\pi t)$ is applied to the filter, its

$\gamma_i, 0 \leq i \leq 6$	Adaptor type	$\alpha_j, 0 \leq j \leq 6$	α_{CSD}	$\beta_k, 1 \leq k \leq 6$	β_{CSD}
0.51290	1	0.4871	0.10000$\bar{1}$01	–	–
−0.40441	3	0.40441	0.10$\bar{1}$01000	0.8337626	1.00$\bar{1}$0$\bar{1}$0$\bar{1}$0$\bar{1}$
0.60271	1	0.3922	0.10$\bar{1}$00100	0.2618522	0.010000$\bar{1}$0
−0.66872	4	0.3313	0.1010101	1.113236	1.00100$\bar{1}$010
0.33424	2	0.33424	0.10$\bar{1}$0$\bar{1}$0$\bar{1}$0	0.5554835	0.100100$\bar{1}$00
−0.89613	4	0.1038	0.00100$\bar{1}$0$\bar{1}$	1.14402056	1.001001010
0.20669	2	0.2067	0.010$\bar{1}$0101	0.69502645	1.0$\bar{1}$0$\bar{1}$001

Tab. 5. Low-pass filter coefficients Example 3.

output is $y(t) = \sin(80\pi t)$. Both $x(t)$ and $y(t)$ are shown in Fig. 7(c) and 7(d). The responses shown in Fig. 7 are illustrated using MATLAB tool.

For multiplierless implementation of the lattice WDF, γ coefficients, adaptor type, α coefficients (for Richards' implementation), β coefficients (for three port parallel adaptor based implementation) and their CSD representations are given in Tab. 6. For Richards' implementation, $f_{\max}$ is given by

$$f_{\max} = \min\left\{\frac{1}{2T_a + 2T_a}, \frac{1}{4T_a + 5T_a}, \frac{1}{4T_a + 4T_a}, \frac{1}{4T_a + 4T_a}\right\}$$
$$= \min\left\{\frac{1}{4T_a}, \frac{1}{9T_a}, \frac{1}{8T_a}, \frac{1}{8T_a}\right\} = \frac{1}{9T_a}. \tag{24}$$

To implement a low-pass lattice WDF using three port parallel adaptors, the $f_{\max}$ in terms of T_m and T_a for each of these allpass sections, is same as given in (11). β coefficients and their CSD equivalents are given in Tab. 6. For multiplierless implementation, minimum $f_{\max}$ of the overall filter is given by

$$f_{\max} = \min\left\{f_{\max\alpha_0}, f_{\max\beta_1\beta_2}, f_{\max\beta_3\beta_4}, f_{\max\beta_5\beta_6}\right\}$$
$$= \min\left\{\frac{1}{4T_a}, \frac{1}{7T_a}, \frac{1}{6T_a}, \frac{1}{6T_a}\right\} = \frac{1}{7T_a}. \tag{25}$$

Comparing of equations (24) and (25), $f_{\max}$ is improved by approximately 28.5 % by reducing critical loop delay. The filters are implemented in CMOS VLSI design and results are summarized in Tab. 7. CMOS layout diagram of the WDF using three port adaptor allpass structure is depicted in Fig. 8. The $f_{\max}$ for three port adaptors based lattice WDF is improved by 13 % compared to Richards' structure based filter. However, the area is increased by 20 %.

7. Conclusion

In this paper, novel approach to design a fixed-point lattice WDF for increased maximum sampling frequency is presented. It is increased by reducing the number of logic components in the critical loop resulting reduced critical delay of the logic components. Second-order three port parallel adaptor allpass section has smaller number of logic components in their critical loop than Richards' allpass section. For the given examples the maximum sampling frequency is improved by using three port parallel adaptor allpass than the conventional Richards' allpass structures. Three design examples are included here of different order lattice WDF. Three port parallel adaptor and Richards' allpass structures based lattice WDF meeting the same filter specifications were designed and implemented using logic synthesis from Verilog HDL description. Lattice WDF structures were evaluated with respect to throughput and arithmetic complexity. The efficient implementation of lattice WDF is presented using 0.18 μm CMOS process in a standard cell library.
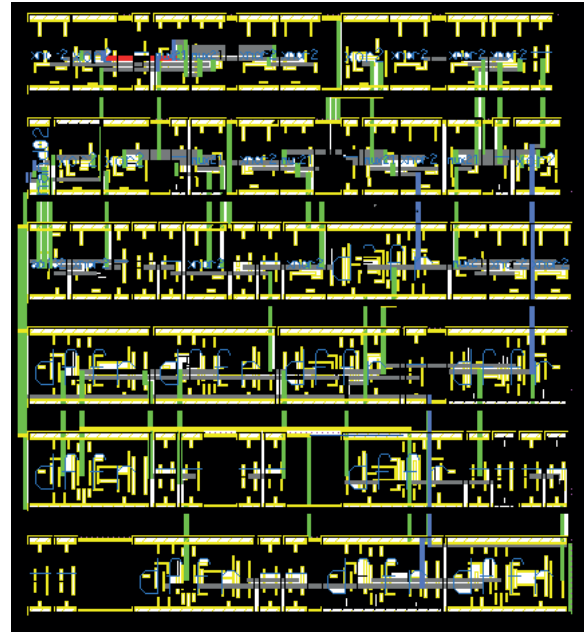

Fig. 8. Layout Diagram of lattice WDF implemented with three port adaptor allpass structure.

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