A CMOS Morlet Wavelet Generator

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Abstract. *The design and characterization of a CMOS circuit for Morlet wavelet generation is introduced. With the proposed Morlet wavelet circuit, it is possible to reach a low power consumption, improve standard deviation (σ) control and also have a small form factor. A prototype in a double poly, three metal layers, 0.5μm CMOS process from MOSIS foundry was carried out in order to verify the functionality of the proposal. However, the design methodology can be extended to different CMOS processes. According to the performance exhibited by the circuit, may be useful in many different signal processing tasks such as nonlinear time-variant systems.*

Keywords

CMOS, wavelet, Morlet, analog multiplier, weak-inversion

1. Introduction

Analog signal processing owes its importance to its strong presence in electronic systems, communications systems, measuring instruments and control equipment among others in which analog signal processing plays an important role. Some examples of analog signal processing include filtering, equalization, impedance matching and magnitude and phase modulation, to name a few. However, Fourier analysis does not provide information about the moment in which the frequency components occur. For that purpose, we use the wavelet transform, which supplies information about the instant when the frequency events appear.

Wavelets are a powerful tool which can be used for a wide range of applications, such as: signal processing [1], data compression [2], smoothing and image denoising [3], fingerprint verification [4], among others [5–12]. There are different types of wavelets, each one with different characteristics and specific applications. One of the simplest is the Haar wavelet, which is widely used for signal analysis using continuous or discrete transforms, and has only one vanishing moment [13]. Another widely used wavelet in the signal analysis is the Mexican hat, whose name comes from the symmetrical shape of its graph. This wavelet is the second derivative of the Gaussian probability density function and has a linear phase response [14]. Daubechies is another wavelet that is characterized by an order N depending on the desired number of vanishing moments, where N is a positive integer. The essential property of wavelets is the so-called compact support, which indicates if the wavelet is of finite duration.

There are several software tools for the analysis and implementation of wavelets (Fortran, IDL, Matlab and Python), however, they have a high consumption of resources in hardware. Instead, dedicated hardware can be used, which has the benefits of a lower consumption of resources and higher processing speed. This paper presents the design of a Morlet wavelet generator circuit which takes advantage of the MOS transistor operating in weak inversion where it has the necessary exponential behavior to generate the Gaussian shape. The resulting circuit is compact and exhibits ultra low power consumption. The paper is organized as follows: Section 2 presents a brief mathematical Morlet wavelet review; Sec. 3 introduces the proposed architecture for Morlet wave generation; Sec. 4 shows the realization of Morlet wavelet; Sec. 5 shows the reported experimental results; finally, conclusions are drawn in Sec. 6.

2. Morlet Wavelet

The wavelet transform is generated using dilatations and translations of the function $\psi(t)$. These translation and dilation processes are defined as:

$$\psi_{\tau,a} = \frac{1}{\sqrt{a}}\psi\left(\frac{t-\tau}{a}\right) \tag{1}$$

where τ conducts the translation and a provides the dilation. The mother wavelet $\psi^*_{\tau,a}(t)$, can be a modulated function composed of two parts:

$$\psi^*_{\tau,a}(t) = \left[\cos\left(\omega_o\frac{t-\tau}{a}\right) + \mathrm{j}\sin\left(\omega_o\frac{t-\tau}{a}\right)\right]\psi_{\tau,a}(t). \tag{2}$$

The Morlet wavelet is constructed by modulating a sinusoidal signal by a Gaussian shape. Hence, it is not a finite-time function. However, the energy in this wavelet is confined

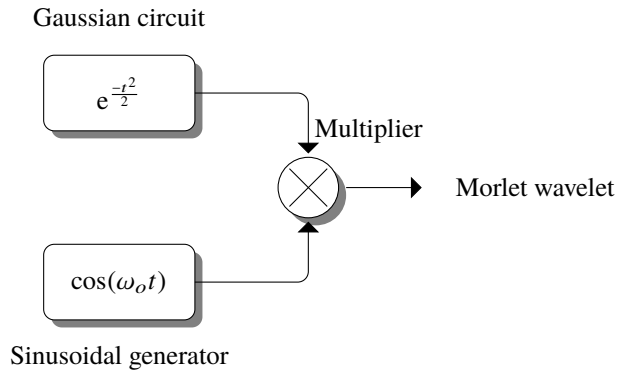

Fig. 1. Block diagram for the realization of a Morlet wavelet.

to a finite interval. Only the real part of the function $\psi^*_{\tau,a}(t)$ is considered for non-stationary signal analysis. The real part of the Morlet wavelet is given by:

$$\psi_R(t) = e^{\frac{-t^2}{2}} \cos(\omega_o t). \tag{3}$$

From (3), three different blocks are required to build the Morlet wavelet: a Gaussian bell shape generator, a sinusoidal source, and a multiplier. In order to perform the multiplication and the sinusoidal signal generation, several topologies have proved to be functional and have enhanced performance [15–18]. The block diagram realization for (3) is given in Fig. 1. Although the Gaussian generator is a very common function, there are scarce reports on this topic. Some relevant articles are considered: In [19] a Gaussian generator is proposed using switched current circuits with the disadvantage of using various control signals. In [20], the MOS-translinear principle is exploited. However, it results in a circuit too complex for implementation. Finally, [21] and [22] use a simple circuit which exploits the transistor weak inversion region, obtaining an acceptable performance.

3. MOS Transistor in Weak Inversion

The minimum voltage to operate an MOS transistor is determined by two parameters; the threshold voltage (V_{TH}) and the voltage applied between the gate and the source terminals (V_{GS}) of the transistors. To achieve low-voltage circuits, designers need to minimize these two parameters. The threshold voltage can be reduced by modifying the process (low threshold technologies are available at the expense of higher production cost), however, V_{TH} is not a controllable parameter for integrated circuit designers [23]. The other parameter that can be modified is the V_{GS} voltage, reducing V_{GS} below V_{TH} the transistor operates in weak inversion region. The transistor weak inversion conditions are [24], [25]:

$$V_{GS} < V_{TH}, \quad I_D \geq 2n\mu C_{ox} V_t^2 \frac{W}{L}, \quad V_{DS} > 4V_t. \tag{4}$$

In this region the transistor operates at low voltage and low power consumption and the drain current is given by:

$$I_D = \frac{W}{L} I_{DO} e^{\frac{(n-1)V_{BS}}{nV_t}} e^{\frac{V_{GS}-V_{TH}}{nV_t}} \left(1 - e^{\frac{-V_{DS}}{V_t}} + \frac{V_{DS}}{V_o}\right) \tag{5}$$

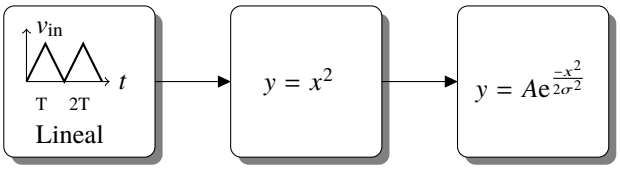

Fig. 2. Block diagram for the realization of a Gaussian function.

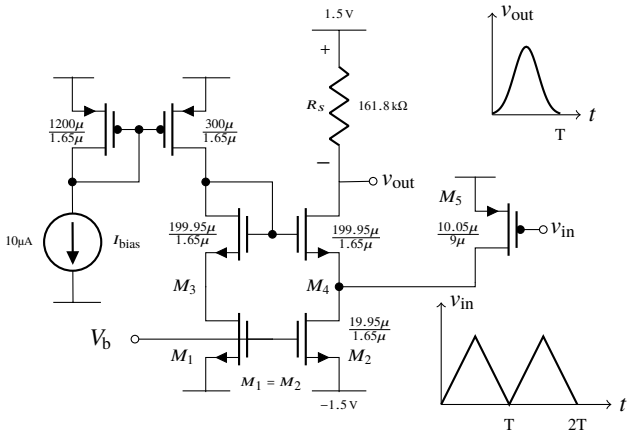

Fig. 3. Proposed Circuit to generate the Gaussian function.

where V_{DS} is the drain-source voltage, V_{BS} is the source-bulk voltage, V_t is the thermal voltage kT/q and V_o is the Early voltage. n is the slope factor, where normally $n < 2$ but becomes $n \approx 1$ for high values of V_{GS}. I_{DO} is the current related to transconductance parameter K, and is defined by

$$I_{DO} \approx \frac{2K(nV_t)}{e^2}. \tag{6}$$

Neglecting the Early and body ($V_{BS} = 0$) effects (5) becomes:

$$I_D = \frac{W}{L} I_{DO} e^{\frac{V_{GS}-V_{TH}}{nV_t}} \approx I_s e^{\frac{V_{GS}}{nV_t}}. \tag{7}$$

In CMOS AMI 0.5 µm, typical values are: $V_{THN} = 0.7$ V; $V_{THP} = 0.9$ V; $\mu_n C_{ox} = 58.4\,\mu A/V^2$, $n \approx 1$. With these technology values and the proposed transistor size $W/L = 120$ the expected current is:

$$I_D \leq 9.4\,\mu A. \tag{8}$$

4. Morlet Wavelet Realization

The operating principle of Gaussian circuit is described in [21], and the block design to realize the Gaussian function is shown in Fig. 2, where the input to the first block should be a triangular wave follow by a squaring block and an exponential circuit. The proposed circuit to generate a Gaussian function is show in Fig. 3.

In this circuit, the input signal is a triangular waveform, which is applied to a P-type transistor (M_5) operating in the saturation region. As a result, the drain current of M_5 is proportional to the square of the input voltage. Neglecting the channel modulation effect, the conditions in this operating region are [25]:

$$I_{\mathrm{Dsat5}} = \frac{1}{2}\mu_p C_{\mathrm{ox}} \left(\frac{W}{L}\right)_5 (V_{\mathrm{SG}} - V_{\mathrm{THP}})^2, \tag{9}$$

$$V_{\mathrm{SD}} > (V_{\mathrm{SG}} - V_{\mathrm{THP}}). \tag{10}$$

The output current in M_5 is converted to voltage through transistor M_2 operating in the linear region, thereby the V_{D2} is proportional to squared v_{in}. The conditions at the linear region are [25]:

$$I_{\mathrm{D2}} \approx \mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_2 (V_{\mathrm{GS2}} - V_{\mathrm{THN}}) V_{\mathrm{DS}}. \tag{11}$$

According to the previous equations, the equivalent resistance is:

$$r_{\mathrm{DS2}} = \frac{1}{\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_2 (V_{\mathrm{b}} - V_{\mathrm{THN}})}. \tag{12}$$

Note that voltage $V_{\mathrm{b}} = V_{\mathrm{GS1,2}}$ is used to bias the transistors M_1 and M_2. I_{bias} is set small enough to make transistors M_3 and M_4 work in weak inversion. Under this condition, we can express the currents in M_3 and M_4 as

$$I_{\mathrm{D3}} = I_{\mathrm{s}} \mathrm{e}^{\frac{V_{\mathrm{G3}}}{nV_{\mathrm{t}}}} \mathrm{e}^{\frac{-V_{\mathrm{S3}}}{nV_{\mathrm{t}}}} \quad \text{and} \quad I_{\mathrm{D4}} = I_{\mathrm{s}} \mathrm{e}^{\frac{V_{\mathrm{G4}}}{nV_{\mathrm{t}}}} \mathrm{e}^{\frac{-V_{\mathrm{S4}}}{nV_{\mathrm{t}}}} \tag{13}$$

where V_{G3}=V_{G4}, $V_{\mathrm{S3}} = I_{\mathrm{D3}} \cdot R_{\mathrm{DS1}}$. If we combine I_{D3} and I_{D4} and assuming that I_{D5} is greater than I_{D4}, which we can safely assume because M_5 operates in saturation and M_4 in weak inversion, I_{D4} is:

$$I_{\mathrm{D4}} \approx I_{\mathrm{D3}} \mathrm{e}^{\frac{-I_{\mathrm{D5}} * R_{\mathrm{DS2}}}{nV_{\mathrm{t}}}} \approx I_{\mathrm{D3}} \mathrm{e}^{-\frac{(\frac{1}{2}\mu_p C_{\mathrm{ox}} \left(\frac{W}{L}\right)_5 (V_{\mathrm{SG5}} - V_{\mathrm{THP}})^2)}{nV_{\mathrm{t}}(\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_2 (V_{\mathrm{b}} - V_{\mathrm{THN}}))}}. \tag{14}$$

The exponential current is inversely proportional to I_{D5} and R_{DS2} and the variance is controlled by V_{b}. The design considerations for those transistors are low bias current (I_{bias}) and large dimensions. As shown in Sec. 2, the current has an exponential behavior in this region. The drain current of M_4 should be a Gaussian waveform, which is converted to voltage using resistor R_{G} in order to have it available in the next stage.

In accordance to Fig. 1, the Gaussian function needs to be multiplied by a cosine function to generate a Morlet wavelet. For this reason, the next block is a four-quadrant multiplier based on Gilbert cell [26]. The Gilbert cell is composed of six MOS transistors, which form three differential pairs operating in saturation, generating a differential output current [26]. The schematic is shown in Fig. 4 [15].

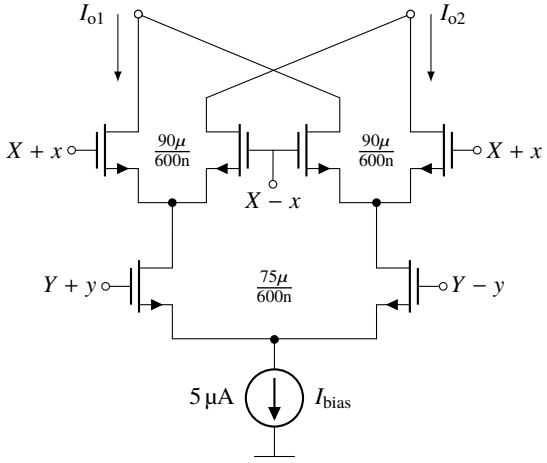

Fig. 4. Multiplier used in the generation of the Morlet wavelet.

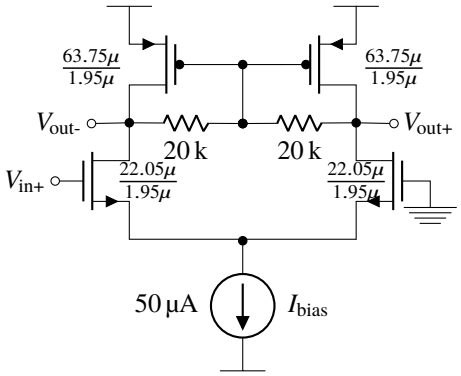

Fig. 5. Single-to-differential converter.

The four-quadrant multiplier output current is given by [26]:

$$I_{\mathrm{o}} = I_{\mathrm{o1}} - I_{\mathrm{o2}} = 2\sqrt{k}x \left(\sqrt{I_{y1}} - \sqrt{I_{y2}}\right). \tag{15}$$

The term $\left(\sqrt{I_{y1}} - \sqrt{I_{y2}}\right)$ is generated by the bottom differential pair [26]:

$$\left(\sqrt{I_{y1}} - \sqrt{I_{y2}}\right) = \sqrt{2K_3 y} \tag{16}$$

where y is the bottom differential pair input and K_3 is its transconductance, therefore, the output current of the Gilbert multiplier is given by [26]:

$$I_{\mathrm{o}} = I_{\mathrm{o1}} - I_{\mathrm{o2}} = 2\sqrt{2KK_3}xy \tag{17}$$

where $K = \mu C_{\mathrm{ox}} W/L$ and x, y are the voltage inputs. Notice that the multiplier cell requires differential inputs. Figure 5 shows the circuit that modifies the Gaussian and sine waves into a differential signal in order to interconnect the gaussian circuit with the multiplier.

5. Experimental Results

A prototype of the CMOS circuit for a Morlet Wavelet generator was implemented in a double poly, three metal

		This work	[27]	[28]	[29]	[30]
Technology		0.5 µm	1.2 µm	2 µm	-	0.35 µm
Transistors						
	Squaring	1	CMOS	2	6	7
	Exponential	5	Log-domain integrators	10	one comparator	-
	Multiplier	6	38	0	0	-
Area		99 µm × 27 µm	-	-	-	-
Power Consumption		430 µW	1.4 nA	3 V	-	-
Sigma control		V_b	-	I_x	V_{dis}	I_t

Tab. 1. Performance and comparison among other approaches.

Fig. 6. Prototype die photo.

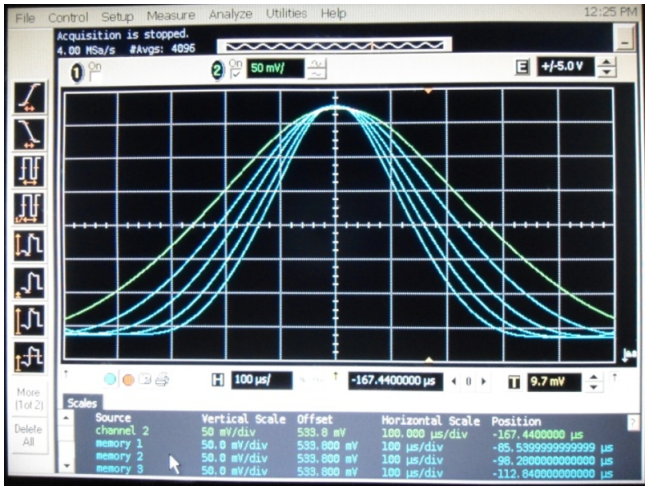

Fig. 7. Gaussian output waveform of the prototype.

layers, 0.5 µm ON Semiconductors CMOS technology from MOSIS foundry. The die photo is shown in Fig. 6. Since the Gaussian circuit uses transistors operating in weak-inversion, this block is suitable for low voltage and low power applications. In addition, the layout of the gaussian circuit is compact as it only uses five transistors requiring an area of 99 µm × 27 µm. This layout includes a current mirror with a ratio of 1 : (1/10) in order to facilitate the measurement of the circuit, and two single-to-differential converters blocks. Figure 7 shows the output voltage of the Gaussian circuit. In this figure, V_b is swept from 0.5 V to 1.5 V, where the applied

Fig. 8. Morlet output waveform of the prototype.

triangular waveform has an amplitude of 500 mV at 10 kHz. Note that this characterization has been made by a voltage-voltage relation in order to obtain the Gaussian function and has no relation to the AC response of the circuit itself.

Finally, the four-quadrant multiplier allows us to multiply the Gaussian function and the sine wave, providing the Morlet wave shown in Fig. 8. In this particular case, the triangular function goes from 1.6 kHz to 10 kHz and the sinusoidal function runs at 60 kHz.

6. Conclusion

This paper presents the design of a Morlet wave generator based on a simple Gaussian circuit which is suitable for low-voltage, low-power applications. The design takes advantage of the various operating regions of the MOS transistor. A prototype of the proposal was implemented in a double poly, three metal layers, 0.5 µm in CMOS technology from MOSIS foundry. The prototype is compact with an active area of 205.95 µm × 192.45 µm. The results obtained in the characterization show that using the weak-inversion region of the MOS transistor is an appropriate option for attaining Gaussian functions with 10 µA. The total power consumption of the Morlet wavelets was 287 µA with ±1.5 V of the total power supply and can generate a Gaussian function at a maximum frequency of 673 kHz. The variation of σ is obtained with V_b, which varies from −0.5 V to 1.5 V. Table 1 shows a comparison of circuits that generate Gaus-

sian functions and Morlet wavelet. It can be seen that our proposal has fewer transistors with respect to other topologies, whereby a good form factor, smaller number of nodes whereby a wider bandwidth is achieved is obtained with lower power consumption. It can be concluded that the proposed Morlet wavelet generator has an acceptable performance in terms of power consumption, the frequency of operation and control of the standard deviation sigma.

References

[1] BAYRAM, I., SELESNICK, I. W. A dual-tree rational-dilation complex wavelet transform. *IEEE Transactions on Signal Processing*, 2011, vol. 59, no. 12, p. 6251–6256. DOI: 10.1109/TSP.2011.2166389

[2] YE, L., HOU, Z. Memory efficient multilevel discrete wavelet transform schemes for jpeg2000. *IEEE Transactions on Circuits and Systems for Video Technology*, 2015, vol. 25, no. 11, p. 1773–1785. DOI: 10.1109/TCSVT.2015.2400776

[3] MALEKI, A., RAJAEI, B., POURREZA, H. R. Rate-distortion analysis of directional wavelets. *IEEE Transactions on Image Processing*, 2012, vol. 21, no. 2, p. 588–600. DOI: 10.1109/TIP.2011.2165551

[4] BHATNAGAR, G., WU, Q. M. J., RAMAN, B. A new fractional random wavelet transform for fingerprint security. *IEEE Transactions on Systems, Man, and Cybernetics - Part A: Systems and Humans*, 2012, vol. 42, no. 1, p. 262–275. DOI: 10.1109/TSMCA.2011.2147307

[5] TAN, M., QIU, A. Spectral Laplace-Beltrami wavelets with applications in medical images. *IEEE Transactions on Medical Imaging*, 2015, vol. 34, no. 5, p. 1005–1017. DOI: 10.1109/TMI.2014.2363884

[6] HOWLADER, T., CHAUBEY, Y. P. Noise reduction of CDNA microarray images using complex wavelets. *IEEE Transactions on Image Processing*, 2010, vol. 19, no. 8, p. 1953–1967. DOI: 10.1109/TIP.2010.2045691

[7] YANG, L., TANG, Y. Y. , LU, Y., et al. A fractal dimension and wavelet transform based method for protein sequence similarity analysis. *IEEE/ACM Transactions on Computational Biology and Bioinformatics*, 2015, vol. 12, no. 2, p. 348–359. DOI: 10.1109/TCBB.2014.2363480

[8] AHMAD, S., BOLIC, M., DAJANI, H., et al. Measurement of heart rate variability using an oscillometric blood pressure monitor. *IEEE Transactions on Instrumentation and Measurement*, 2010, vol. 59, no. 10, p. 2575–2590. DOI: 10.1109/TIM.2010.2057571

[9] BANERJEE, S., MITRA, M. Application of cross wavelet transform for ECG pattern analysis and classification. *IEEE Transactions on Instrumentation and Measurement*, 2014, vol. 63, no. 2, p. 326–333. DOI: 10.1109/TIM.2013.2279001

[10] BREGNI, S. Compared accuracy evaluation of estimators of traffic long-range dependence. *IEEE Latin America Transactions*, 2015, vol. 13, no. 11, p. 3649–3654. DOI: 10.1109/TLA.2015.7387944

[11] LEE, T. Y., SHEN, H. W. Efficient local statistical analysis via integral histograms with discrete wavelet transform. *IEEE Transactions on Visualization and Computer Graphics*, 2013, vol. 19, no. 12, p. 2693–2702. DOI: 10.1109/TVCG.2013.152

[12] JI, H., YANG, X., LING, H., et al. Wavelet domain multifractal analysis for static and dynamic texture classification. *IEEE Transactions on Image Processing*, 2013, vol. 22, no. 1, p. 286–299. DOI: 10.1109/TIP.2012.2214040

[13] KYRIAKOPOULOS, K., PARISH, D. Applying wavelets for the controlled compression of communication network measurements. *IET Communications*, 2010, vol. 4, no. 5, p. 507–520. DOI: 10.1049/iet-com.2009.0050

[14] WANG, L., CHEN, T. Multistability of neural networks with mexican-hat-type activation functions. *IEEE Transactions on Neural Networks and Learning Systems*, 2012, vol. 23, no. 11, p. 1816–1826. DOI: 10.1109/TNNLS.2012.2210732

[15] MINCICA, M., PEPE, D., ZITO, D. CMOS UWB multiplier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2011, vol. 58, no. 9, p. 570–574. DOI: 10.1109/TCSII.2011.2161175

[16] HWANG, Y.-S., LIU, W.-H., TU, S.-H., et al. New building block: Multiplication-mode current conveyor. *IET Circuits, Devices Systems*, 2009, vol. 3, no. 1, p. 41–48. DOI: 10.1049/iet-cds:20080156

[17] KUMNGERN, M., JUNNAPIYA, S. A sinusoidal oscillator using translinear current conveyors. In *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. 2010, p. 740–743. DOI: 10.1109/APCCAS.2010.5774754

[18] PITTALA, C., SRINIVASULU, A. Two simple sinusoidal oscillators using single operational transresistance amplifier. In *Proceedings of the 3rd International Conference on Signal Processing, Communication and Networking (ICSCN)*. 2015, p. 1–5. DOI: 10.1109/ICSCN.2015.7219906

[19] QINCHUN, H. Analog implementation of Morlet wavelet using switched current circuits. In *Proceedings of the IEEE International Conference on Signal Processing, Communication and Computing (ICSPCC)*. 2013, p. 1–4. DOI: 10.1109/ICSPCC.2013.6664016

[20] SANCHEZ-LOPEZ, C., DIAZ-SANCHEZ, A., TLELO-CUAUTLE, E. MOS-translinear Morlet wavelets. In *Proceedings of the 45th Midwest Symposium on Circuits and Systems (MWSCAS)*. 2002, vol. 1, p. 1–8. DOI: 10.1109/MWSCAS.2002.1187205

[21] MADRENAS, J., VERLEYSEN, M., THISSEN, P., et al. A CMOS analog circuit for Gaussian functions. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 1996, vol. 43, no. 1, p. 70–74. DOI: 10.1109/82.481479

[22] SRIVASTAVA, R., SINGH, U., GUPTA, M. Analog circuits for Gaussian function with improved performance. In *Proceedings of the World Congress on Information and Communication Technologies (WICT)*. 2011, p. 934–938. DOI: 10.1109/WICT.2011.6141373

[23] RODRIGUEZ-VILLEGAS, E. *Low Power and Low Voltage Circuit Design with the FGMOS Transistor*. 1st ed. IET, 2006. ISBN: 978-0-86341-617-0

[24] ENZ, C. C., VITTOZ, E. A. *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. 1st ed. Wiley, 2006. ISBN: 978-0-470-85541-6

[25] WANG, A., CALHOUN, B. H., CHANDRAKASAN, A. P. *Subthreshold Design for Ultra Low-Power Systems*. 1st ed. Springer, 2006. ISBN: 978-0-387-33515-5

[26] HAN, G., SANCHEZ-SINENCIO, E. CMOS transconductance multipliers: A tutorial. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 1998, vol. 45, no. 12, p. 1550–1563. DOI: 10.1109/82.746667

[27] LI, H., GANG, H., ZHANG, G., et al. Log-domain implementation of analog wavelet filters. In *Proceedings of the International Conference on Intelligent Control and Information Processing*. 2010, p. 187–190. DOI: 10.1109/ICICIP.2010.5565318

[28] CHOI, J., SHEU, B. J., CHANG, J. C. F. A Gaussian synapse circuit for analog VLSI neural networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 1994, vol. 2, no. 1, p. 129–133. DOI: 10.1109/92.273156

[29] CHURCHER, S., MURRAY, A. F., REECKIE, H. M. Programmable analogue VLSI for radial basis function networks. *Electronics Letters*, 1993, vol. 29, no. 18, p. 1603–1605. DOI: 10.1049/el:19931068

[30] SAATLO, A. N., OZOGUZ, S. CMOS implementation of scalable Morlet wavelet for application in signal processing. In *Proceedings of the 38th International Conference on Telecommunications and Signal Processing (TSP)*. 2015, p. 1–4. DOI: 10.1109/TSP.2015.7296375

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