QPSK Modulator with Continuous Phase and Fast Response Based on Phase-Locked Loop

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Abstract. *Among M-phase shift keying (M-PSK) schemes, quadrature phase-shift keying (QPSK) is used most often because of its efficient bandwidth consumption. However, in comparison with minimum-shift keying, which has continuous phase transitions, QPSK requires a higher bandwidth to transmit a signal. This article focuses on the phase transitions in QPSK signals, and a QPSK modulator based on a phase-locked loop (PLL) is proposed. The PLL circuit in the proposed system differs from that of conventional PLL circuits because a three-input XOR gate and a summing circuit are used. With these additional components, the proposed PLL provides a continuous phase change in the QPSK signal. Consequently, the required bandwidth for transmitting the QPSK signal when using the proposed circuit is less than that for a conventional QPSK signal with a discontinuous phase. The analytical results for the proposed system in the time domain agree well with the experimental and simulation results of the circuit. Both the theoretical and experimental results thus confirm that the proposed technique can be realized in real-world applications.*

Keywords

QPSK, Phase Locked Loop (PLL), phase shift

1. Introduction

Digital modulation currently plays a vital role in communication systems such as satellite communication [1–4], television broadcasting, asymmetrical digital subscriber lines (ADSL) [5], and mobile communication [6], [7]. This is because digital modulation provides high security, is not subject to interfering noise, and requires less bandwidth than analogue modulation. Various types of digital modulation exist, including amplitude shift keying (ASK), frequency shift keying (FSK) and phase shift keying (PSK). In PSK modulation, the phase of the output signal is shifted from the reference phase according to the input data bit. There are multiple variants of PSK, such as binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK) and M-phase shift keying (M-PSK). Among the PSK variants, QPSK modulation is one of the most popular ones, and four different phases are assigned for it: i.e., 45°, 135°, −135°, and −45°.

In general, M-PSK digital phase modulation involves a signal of the form $s(t) = A\cos(\omega_c t - \phi_n)$, where ϕ_n is one of the M-PSK phases. This expression can be rewritten as $s(t) = a_n \cos(\omega_c t) + b_n \sin(\omega_c t)$, where $a_n = A\cos\phi_n$ and $b_n = A\sin\phi_n$. It can be seen that the key factors for controlling the phase of the M-PSK signal are a_n and b_n, which are the voltage levels corresponding to each set of digital data bits (n bits/set). For example, in the case of 2 bits/set, $M = 2^2 = 4$, which is equivalent to QPSK modulation; hence, four possible two-bit combinations (00, 01, 10, 11) are converted to analogue voltage levels by using a D/A converter to generate the associated a_n and b_n. Finally, a phase-modulated signal is obtained.

This basic principle for generating a QPSK signal has led to many modulation techniques, such as QPSK modulation using FPGA [8], [9], VLSI [10] or CMOS [11–14]. All these techniques are based on the application of the aforementioned basic principle by using modern technology. Some limitations exist such as applicable frequencies, power consumption, unsupported electronic components, and high cost. In 2007, a QPSK modulating circuit that controls the gain of a phase-locked loop (PLL) to shift the phase was proposed, along with external circuits [15]. However, the reference frequency used for the PLL in this approach is fairly low; as a result, it cannot be implemented using current technology. In addition, the requirement of external circuits also increases the level of complexity of this technique. Furthermore, the continuous phase change in the PSK signal owing to the operation of the PLL is not mentioned in the study. In [16], a QPSK modulating circuit constructed with basic electronic components (e.g., op-amps, D flip-flops, inverters, and BJTs) was proposed. This structure not only is complex but also lacks flexibility owing to the mandatory requirement of a 90° phase difference in the input signals.

It is well known that the phase in a QPSK signal is discontinuous, which results in signal components of high frequency; thus, QPSK signals require a high bandwidth for transmission. The bandwidth required can be reduced by using minimum-shift keying (MSK) [17], which is

known as continuous phase shift keying. There are no phase discontinuities because the frequency changes occur at the carrier's zero-crossing points. Therefore, MSK requires less bandwidth than QPSK. However, it should be noted that an MSK signal uses more than one frequency for signal transmission, whereas a QPSK signal uses only one frequency.

In this paper, a technique for generating a QPSK signal based on a PLL circuit is proposed. Given that the PLL has a natural response every time the parameters in the system are changed, the outputs of the PLL (the QPSK signal) has a continuous phase change and a constant frequency. Hence, this technique requires less bandwidth than conventional QPSK and uses only one constant frequency, unlike MSK, which uses multiple frequencies. In the demodulation process, the principle of demodulating conventional QPSK signals can be applied to the proposed approach. Although the demodulation process necessarily starts after the phase transition in the modulated signal is complete, this is not important because the phase transition time of the modulated signal is constant. In addition, the phase transition time can be adjusted by modifying the cut-off frequency of the low-pass filter.

2. Principles

A PLL is a control system that generates an output signal whose phase is related to the phase of the input signal. Although the basic concepts of PLL operation are relatively simple, the associated mathematical analysis, which involves many elements, can become complicated. A block diagram of a conventional PLL is shown in Fig. 1(a). The reference signal and the output signal from the voltage-controlled oscillator (VCO) are fed into the phase detector. The output from the phase detector is passed through the loop filter and then applied to the VCO.

2.1 Conventional Phase-Locked Loops

In this section, a brief overview of conventional PLLs, which consist of a phase detector (PD), a low-pass filter (LPF), a VCO, and an integrator, is presented. The notation used in the figures is as follows:

$\phi_i(s)$: Laplace transform of the input function $\phi_i(t)$
$\phi_o(s)$: Laplace transform of the output function $\phi_o(t)$
$\phi_d(s)$: Laplace transform of the phase error $\phi_d(t)$
$V_L(s)$: Laplace transform of the loop filter output $v_L(t)$
$\omega_o(s)$: Laplace transform of the frequency output of the VCO $\omega_o(t)$
$F(s)$: Transfer function of the loop filter
$I(s)$: Transfer function of the integrator
ω_r: Running frequency of the VCO
k_d: Gain of the phase detector
A: Gain of the loop filter
B: Sensitivity of the VCO
C: Gain of the integrator
D: A constant, where $D=A\times B\times C$

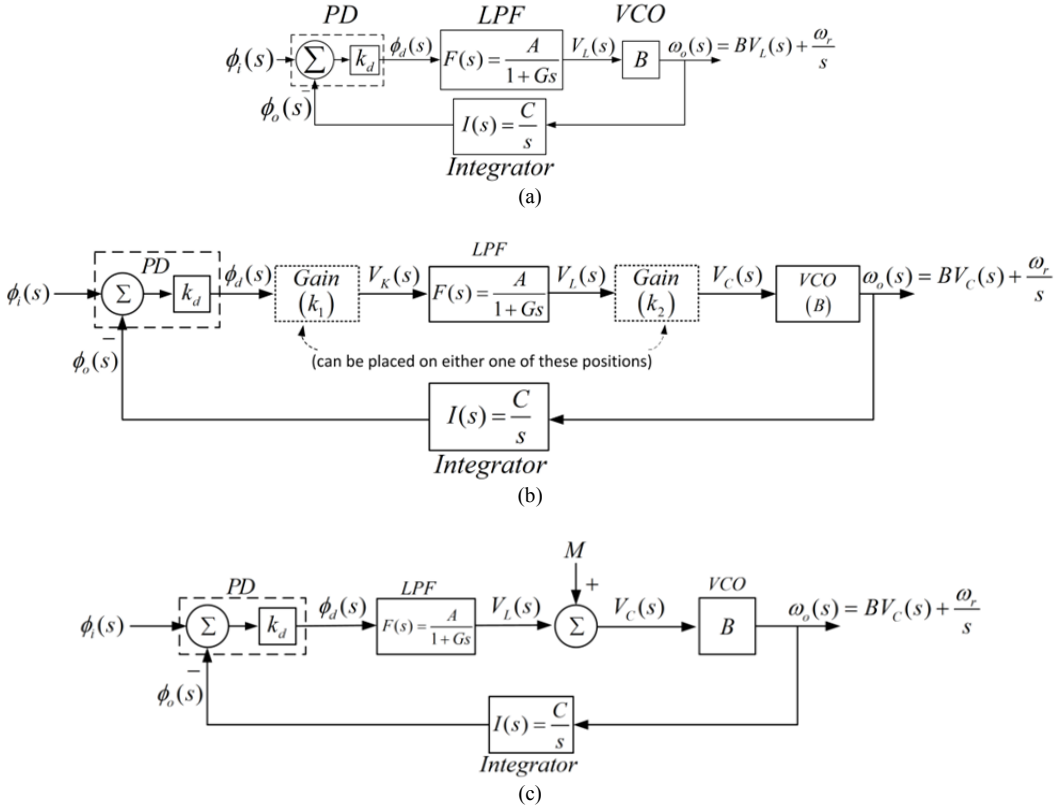


Fig. 1. Block diagrams of different PLLs: (a) Block diagram of a conventional PLL. (b) Block diagram of a PLL with gain control. (c) Block diagram of a PLL with a summing circuit.

The aim of conventional PLL analysis is to obtain the complete solution $\phi_o(t)$ of the system. From Fig. 1(a), the relationship of the parameters in the system can be written as

$$\phi_o(s) = F(s)I(s)Bk_d\phi_i(s) - F(s)I(s)Bk_d\phi_o(s) + I(s)\frac{\omega_r}{s}. \quad (1)$$

Substituting the transfer function of the loop filter, $F(s) = A/(1 + Gs)$, and the transfer function of the integrator, $I(s) = C/s$, in (1) yields

$$Gs^2\phi_o(s) + s\phi_o(s) + D\phi_o(s) = D\phi_i(s) + \frac{C\omega_r}{s} + CG\omega_r. \quad (2)$$

By taking the inverse Laplace transform of both sides of (2), it becomes a second-order differential equation.

$$G\frac{\mathrm{d}^2\phi_o(t)}{\mathrm{d}t^2} + \frac{\mathrm{d}\phi_o(t)}{\mathrm{d}t} + D\phi_o(t) = D\phi_i(t) + C\omega_r u(t) + CG\omega_r\delta(t). \quad (3a)$$

In reality, all systems have the causality property. For this system, t in (3a) is said to be greater than zero ($t > 0$), and applying this property to (3a) gives rise to (3b).

$$\frac{G\mathrm{d}^2\phi_o(t)}{\mathrm{d}t^2} + \frac{\mathrm{d}\phi_o(t)}{\mathrm{d}t} + D\phi_o(t) = D\phi_i(t) + C\omega_r. \quad (3b)$$

From (3b), the solution for $\phi_o(t)$ can be determined by solving the differential equation. In general, $\phi_o(t)$ is composed of two parts: a homogeneous solution (the natural response $\phi_{on}(t)$) and a particular solution (the forced response $\phi_{of}(t)$). The natural response can be found from the second-order differential equation when there is no input applied to the system,

$$G\frac{\mathrm{d}^2\phi_{on}(t)}{\mathrm{d}t^2} + \frac{\mathrm{d}\phi_{on}(t)}{\mathrm{d}t} + D\phi_{on}(t) = 0. \quad (4)$$

From (4), the characteristic equation is given by (5), and the solutions of (5) are expressed in (6).

$$Gm^2 + m + D = 0, \quad (5)$$

$$m_{1,2} = \frac{-1 \pm \sqrt{1 - 4GD}}{2G}. \quad (6)$$

In the transfer function of the loop filter, ω_c is specified as the cut-off frequency. Hence, the relationship equation between G and ω_r is defined as $G = 1/\omega_r$, and (6) can be rewritten as

$$m_{1,2} = -\frac{\omega_c}{2} \pm \frac{\omega_c}{2}\sqrt{1 - \frac{4D}{\omega_c}}. \quad (7)$$

By using the Taylor series $\sqrt{1+x} = 1 + \frac{x}{2} - \frac{x^2}{8} + \frac{x^3}{16} - \ldots$ for $|x| \le 1$ and $x = -4D/\omega_c$, (7) can be rewritten as

$$m_{1,2} = -\frac{\omega_c}{2} \pm \frac{\omega_c - 2D}{2}. \quad (8)$$

From (8), the solutions are $m_1 = -D$ and $m_2 = -(\omega_c + D)$, and thus the solution of the natural response is

$$\phi_{on}(t) = \frac{C_1}{\exp(Dt)} + \frac{C_2}{\exp((\omega_c - D)t)}. \quad (9)$$

Next, the forced response $\phi_{of}(t)$ will be analyzed from the second-order differential equation. Let the input signal of the system $\phi_i(t)$ be a linear function of time, given as

$$\phi_i(t) = \omega_i t + \theta_i \quad (10)$$

where ω_i is the reference frequency and θ_i is the initial phase of the input signal. Then, $\phi_{of}(t)$ can be expressed in the following form

$$\phi_{of}(t) = at + b \quad (11)$$

where a and b are constants. Replacing $\phi_i(t)$ and $\phi_{of}(t)$ in (3) with (10) and (11) yields

$$\phi_{of}(t) = \omega_i t + \theta_i + \frac{C\omega_r - \omega_i}{D}. \quad (12)$$

Thus, the complete response is

$$\phi_o(t) = \left(\frac{C_1}{\exp(Dt)} + \frac{C_2}{\exp((\omega_c - D)t)}\right) + \left(\omega_i t + \theta_i + \frac{C\omega_r - \omega_i}{D}\right). \quad (13)$$

From (13), the process of the PLL can be described as follows: when a proper input is fed to the PLL, the system will reach the "steady-state" mode if the natural response is zero. It should be noted that parameters of the PLL (e.g., all gains in the PLL and the cut-off frequency) have an effect on the time required to reach the steady state. When the PLL is in the steady state, its output is

$$\phi_o(t) = \omega_i t + \theta_i + \frac{C\omega_r - \omega_i}{D}. \quad (14)$$

By comparing the reference signal in (10) with the output in (14), it can be seen that the angular frequency of the reference signal is equal to that of the output signal, but the phase is shifted, as given by

$$\phi_d(t) = \frac{\omega_i - C\omega_r}{D}. \quad (15)$$

The shifted phase depends on the angular frequency of the reference signal and all gains in the system. It should be noted that a QPSK modulator using this technique was presented in [15].

2.2 QPSK Modulator Based on a PLL with a Gain Control

According to the analysis shown in the previous subsection, the phase of the output signal can be controlled by the system gain. However, it is fairly difficult to change the gain of a conventional PLL, and the PLL may not be able to reach its locking state as a result of any change made to the system. Therefore, the simplest way to shift the phase of the signal is by adding a gain controller between the

phase detector and the low-pass filter or between the low-pass filter and the VCO, as shown in the block diagram of the PLL with gain control in Fig. 1(b). In this figure, it should be noted that k_1 is a gain constant that is placed between the phase detector and the loop filter and that k_2 is a gain constant that is placed between the loop filter and the VCO. The PLL system is analyzed using Fig. 1(b); the complete response is calculated as in (16) and the phase difference is calculated as in (17).

$$\phi_o(t) = \left(\frac{C_1}{\exp(k_1k_2Dt)} + \frac{C_2}{\exp\left((\omega_c - k_1k_2D)t\right)}\right) + \left(\omega_i t + \theta_i + \frac{C\omega_r - \omega_i}{k_1k_2D}\right), \tag{16}$$

$$\phi_d(t) = \frac{\omega_i - C\omega_r}{k_1k_2D}. \tag{17}$$

From (16) and (17), reference [15] shows that the output phase can be correctly shifted to two positions: π/4 and 3π/4 radians, and that additional circuits are required to shift the phase to –π/4 and –3π/4 radians. The natural response that occurs for each instance of phase shifting causes continuous phase shift modulation. The benefits of such a modulation system are decreased bandwidth usage and high-order harmonic component prevention. However, the gain required for shifting from π/4 to 3π/4 is not the same for shifting from 3π/4 to π/4. For this reason, the natural response occurring for each instance of phase shifting is definitely not equal. Because of the gain variation required for the different phase changes, the non-persistent natural response of the QPSK-PLL modulation with a gain control circuit causes demodulation difficulty. To control phase changes so that the natural response is consistent and to reduce complexity of demodulation, the PLL structure has been improved, as presented in the following section.

2.3 QPSK Modulator Based on a PLL with a Summing Circuit

Another method for generating the QPSK signal is to place a summing circuit between the low pass-filter and the VCO, as depicted in Fig. 1(c). A DC level, *M*, is employed to obtain the desired phase shift. This technique also provides a continuous phase shift in the QPSK signal. The complete response of the system is given by

$$\phi_o(t) = \left(\frac{C_1}{\exp(Dt)} + \frac{C_2}{\exp\left((\omega_c - D)t\right)}\right) + \left(\omega_i t + \theta_i + \frac{C\omega_r - \omega_i + BCM}{D}\right). \tag{18}$$

Equation (18) shows that the DC level can control the output phase shift, which results in

$$\phi_d(t) = \frac{\omega_i - C\omega_r - BCM}{D}. \tag{19}$$

As shown in (18), the DC level *M*, which is used for phase shifting, has no effect on the natural response, as opposed to the case when a PLL with a gain control is used. In addition, the time between phase changes is always constant; as a result, the demodulation procedure when using this technique can be easily managed. Furthermore, the phase-shifting speed can also be controlled by adjusting the cut-off frequency of the low-pass filter. However, only two phase positions can be obtained. Therefore, to achieve the other two phase shift positions, phase reversing is required, which will be discussed in the next section.

2.4 π-Radian Phase Shifting Based on the Data Bit

In this subsection, the theory for adapting operations for π-radian phase shifting based on the data bit of the phase detector is described. In a conventional PLL, the phase detector has two input signals (a reference signal $\phi_i(t)$ and its output signal $\phi_o(t)$), and can detect phase differences ranging from 0 to π radians.

Hence, in a three-input phase detector based on an XOR gate, as shown in Fig. 2(a), two inputs are used to detect the phase difference between two signals, while the other input is used for π-radian phase shifting. The truth table is given in Tab. 1, and it can be seen that when the data bit is in the low state (L), the three-input phase detec-

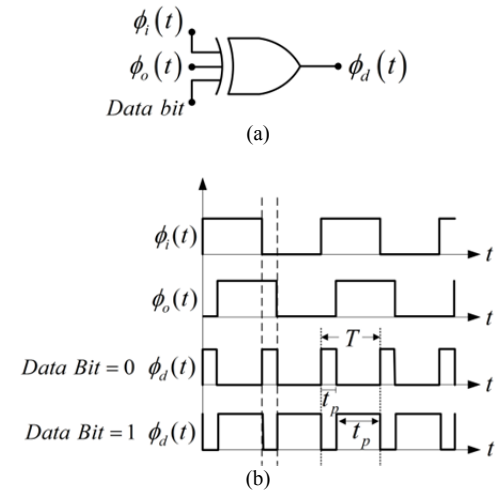


Fig. 2. Phase detector based on an XOR gate: (a) Three-input phase detector based on an XOR gate. (b) Three-input phase detector timing diagram.

Data bit	$\phi_i(t)$	$\phi_o(t)$	$\phi_d(t)$
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Tab. 1. Truth table of a 3-input XOR gate.

tor will operate in the same manner as the conventional phase detector. However, when the data bit is in the high state (H), this phase detector's output is the inverse of the output of the low state (L). The relationship between the input signals of the phase detector is demonstrated in Fig. 2(b). From Fig. 2(b), the duty cycle when the data bit is L and H can be expressed as (20) and (21), respectively.

$$Duty\ cycle\left(\phi_d(t)\right)=\frac{t_p}{T}, \tag{20}$$

$$Duty\ cycle\left(\phi_d(t)\right)=1-\frac{t_p}{T}. \tag{21}$$

With this principle, the proposed PLL can shift the phase by π radians, and this principle can be used to generate a QPSK signal with a PLL. The next section will describe the proposed QPSK modulator, which is based on a summing circuit, and the adaptation of the operation of the phase detector by using the data bit.

3. Proposed QPSK Modulator

As it is clear from the previous subsections, one advantage of a QPSK modulator based on a PLL with a summing circuit is that the QPSK signal produced has a continuous phase change, thus requiring less bandwidth than that of conventional QPSK transmissions. Moreover, demodulation when using this QPSK modulating technique is less complex compared to that when the QPSK modulator based on a PLL with gain control is used, because of the constant phase shifting. In addition, the phase detector based on a three-input XOR gate provides full-range phase shifting. Hence, a new QPSK modulator is proposed, as depicted in Fig. 3. As shown in the figure, the input data bits are used as the switching control signal and the input signal of the phase detector. Thus, the D/A component is not required in this system. The data bits D0 and $\overline{D0}$ are used as the switching control signals for S0 and S1, respectively. The data bit D1, which is also an input signal of the phase detector, is employed to control the phase detector output, either inverting or non-inverting for the low state or the high state, respectively. The designed modulation code is given in Tab. 2.

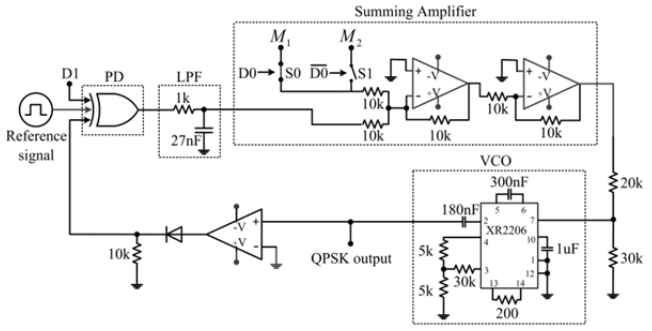


Fig. 3. Proposed QPSK modulator.

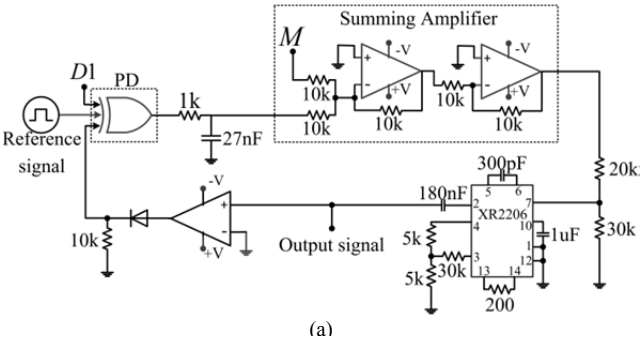
Phase shift	D1	D0	S1	S0
-3π/4	L	L	OFF	ON
–π/4	L	H	ON	OFF
π/4	H	L	OFF	ON
3π/4	H	H	ON	OFF

Tab. 2. The designed modulation code.

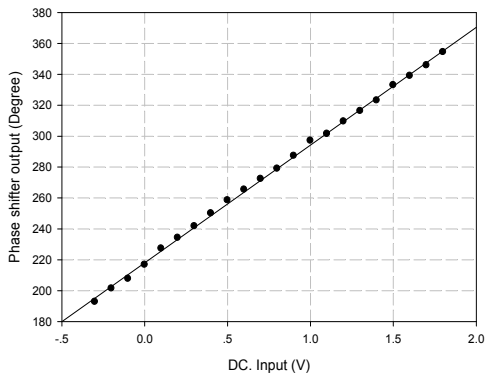
4. Experimental and Simulation Results

4.1 Relationship between the DC Level and the Phase Shift of the QPSK Signal

An experiment using the proposed technique was conducted to verify that this technique can be implemented in real-world applications. The experimental setup and the results are presented in this subsection. A circuit based on the proposed PLL is illustrated in Fig. 4(a). It is composed of a three-input phase detector based on an XOR gate, a summing circuit, a low-pass filter (with its cut-off frequency at 5.89 kHz), and a voltage-controlled oscillator using the XR2206 integrated circuit (which generates a signal whose maximum frequency is 86.73 kHz and has a gain of −17 kHz/V). The relationship between the DC level *M* and the phase shift was first examined in this experiment. The data bit D1 was set to 0 (the low state), the reference signal frequency was set to 70 kHz, and the information signal of the summing circuit was set to be a DC signal. The obtained phase shift output in accordance with



(a)



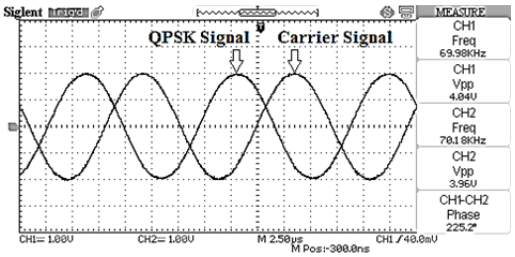
(b)

Fig. 4. Experimental circuit and its phase shift results: (a) Experimental circuit for verifying the relationship between the information signal and the phase shift output. (b) Phase shift of the output signal versus the DC input voltage of the proposed QPSK modulator.

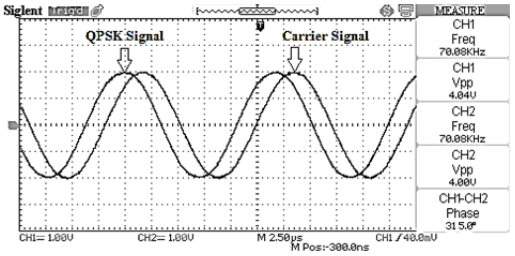
the input DC level M is demonstrated in Fig. 4(b). It can be seen that for DC input voltage levels varying from −0.02 V to 1.32 V, the output signal phase is shifted from $-3\pi/4$ to $-\pi/4$ radians.

4.2 QPSK Modulating Signal

The experimental setup for the proposed QPSK modulator circuit illustrated in Fig. 3 is described in this section. The D0 and $\overline{D0}$ data bits are used to control switches S0 and S1, respectively. The D1 data bit is the input of the phase detector. In addition, two DC levels, M_1 and M_2, are set as −0.02 V and 1.32 V, respectively, to obtain phase shifts of $-3\pi/4$ radians (225°) and $-\pi/4$ radians (315°). The resulting QPSK signals for $-3\pi/4$, $-\pi/4$, $\pi/4$ and $3\pi/4$ phase shifts are shown in Fig. 5.



(a)



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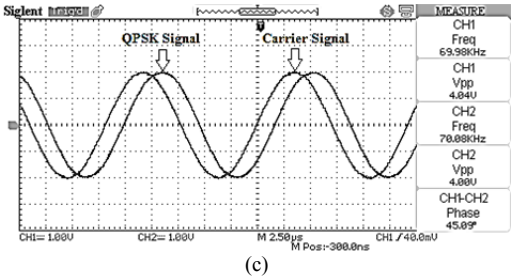
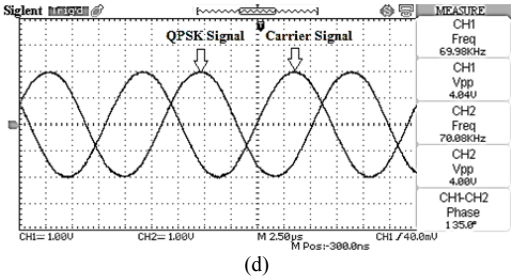
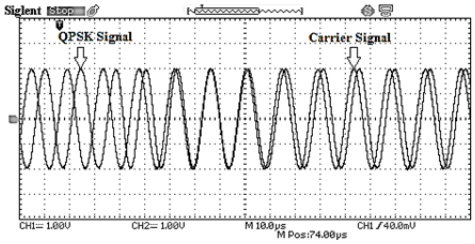


(c)

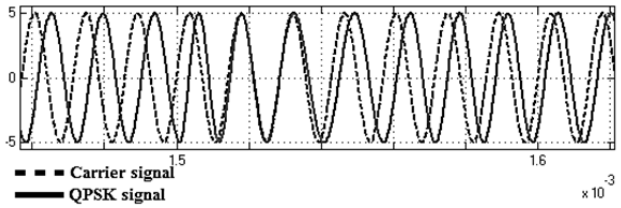


(d)

Fig. 5. Resulting QPSK signals: (a) For a phase shift of $-3\pi/4$ radians. (b) For a phase shift of $-\pi/4$ radians. (c) For a phase shift of $\pi/4$ radians. (d) For a phase shift of $3\pi/4$ radians.



(a)



(b)

Fig. 6. Example of the continuously changing phase of the QPSK signal: (a) Phase changing from $3\pi/4$ radians to $\pi/4$ radians (experimental results). (b) Phase changing from $3\pi/4$ radians to $\pi/4$ radians (simulation results).

For each change in the data bits, the natural response is conclusively removed, and the system reaches the steady state as the phase of the QPSK signal simultaneously reaches the specified value. Because of the continuous phase shift characteristic of the proposed modulator, no high-frequency harmonics occur, and less bandwidth is required than for a conventional QPSK modulator. Figure 6 shows an example of the output phase changing from $3\pi/4$ radians to $\pi/4$ radians.

In addition, the proposed technique was verified by computer simulation using MATLAB/Simulink. The simulation results obtained for an example phase change are shown in Fig. 6(b).

4.3 Reducing Phase-Shifting Time by Changing the Filter's Cut-Off Frequency

According to the analysis and experimental results, it can be seen that the generated QPSK signal has a continuous phase shift when the input data bit is changed. The phase-shifting time can be reduced without affecting the system output by adjusting the cut-off frequency of the low-pass filter in (18). As observed in (18), the cut-off frequency of the low-pass filter affects only the natural response. Hence, making the natural response vanish quickly makes the phase-shifting process faster as well. In other words, phase-shifting time is directly proportional to convergence time to the steady state of the natural response. However, in practice, the complete phase-shifting process is unknown. To determine the completion time of the phase-shifting process, the output of the loop filter must be considered, because the phase-shifting process is truly complete only when the output of the loop filter is in the steady state.

In the experiment and the simulation, phase shifts from $-3\pi/4$ radians to $-\pi/4$ radians were obtained when the cut-off frequency was set to 37,037 rad/s, 50,000 rad/s, and

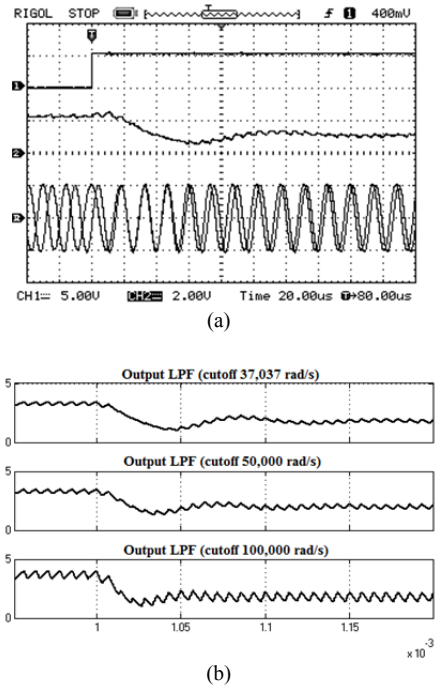


Fig. 7. Experimental and simulation results for different cut-off frequencies: (a) Phase transition of the QPSK signal for a cut-off frequency of 37,037 rad/s. (b) Simulation results of the LPF output for cut-off frequencies of 37,037 rad/s, 50,000 rad/s and 100,000 rad/s.

100,000 rad/s. Figure 7(a) shows an example of phase transition of the QPSK signal for a cut-off frequency of 37,037 rad/s. In this subfigure, the top, middle, and bottom traces are the data, the low-pass filter output, and the QPSK signal and its reference signal, respectively. In addition, the simulation results for the low-pass filter outputs for the three different cut-off frequencies are shown in Fig. 7(b). From this subfigure, it can be seen that an increase in the cut-off frequency can decrease the time it takes for the filter output to reach the steady-state (thus reducing phase-shifting time). As a result, the system will be able to increase the transmission bit rate.

4.4 Power Spectral Densities for Conventional QPSK, QPSK from PLL with a Gain Control and QPSK from PLL with a Summing Circuit

The simulation results for comparing the power spectral densities (PSDs) obtained from conventional QPSK, QPSK from PLL with gain control, and QPSK from PLL with a summing circuit are shown in Fig. 8. The theoretical analysis and the experimental results coherently show that the proposed QPSK modulator provides continuous phase change, which directly affects the PSD of the signal. From Fig. 8(a), it can be seen that the main lobe and the first nulls of the conventional QPSK spectrum occur at the same frequencies as that of the spectra of QPSK from PLL with a summing circuit and the QPSK from PLL with a gain control. However, the difference between the null and peak of its side lobe Ψ is greater than that of the proposed QPSK based on PPL σ. This shows that most of the proposed QPSK signal is contained within the main lobe of the spectrum, resulting in a lower bandwidth than that of conventional QPSK. The spectrums of the bandpass filter outputs can be compared in Fig. 8(b) when the frequency range of the bandpass filter used in the simulation is placed between 63.7-76.3 kHz. According to Fig. 8(b), the spectrum of the filtered QPSK from PLL with summing shows the superior null and peak of the sidelobe than that of the conventional QPSK.

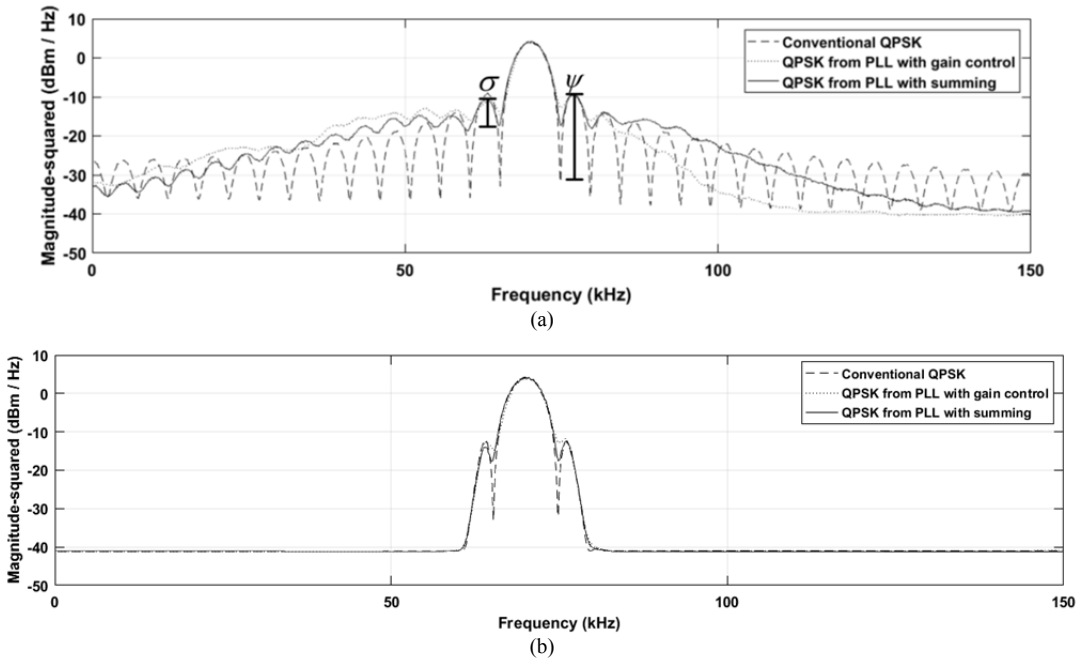


Fig. 8. The comparison of PSDs obtained from different modulation techniques: (a) The spectrum of QPSK signals before filtering. (b) The spectrum of QPSK signals after filtering.

5. Error Analysis

An analysis of phase error in the QPSK signal is presented in this section. Generally, phase detectors, especially XOR gates, generate an output in the form of a pulse-width modulated (PWM) signal, as exemplified in Fig. 9(a). Hence, the phase difference resulting from the phase detector is directly proportional to the DC component of the PWM signal [18], as expressed by the following equation.

$$v_{PWM}(t) = \frac{A_d t_p}{T} + \frac{A_d}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\sin\left(n\omega_0 t\right) - \frac{1}{n}\sin\left(n\omega_0\left(t-t_p\right)\right)\right]. \quad (22)$$

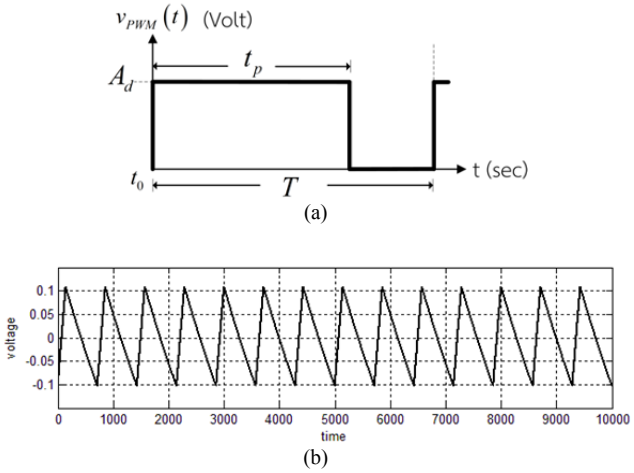


Fig. 9. Error analysis of fluctuating-output of LPF that affects phase shifting of QPSK signal: (a) Realization of the phase detector output. (b) Illustration of the second term of equation (28) using computer simulation.

In (22), A_d is the amplitude of the PWM signal from the XOR gate, t_p is the time for which the signal is high, T is the total period of the signal, and ω_0 is the angular frequency of $\phi_d(t)$. Therefore, the relationship between t_p and the DC component of $v_{PWM}(t)$ can be rewritten as

$$t_p = \frac{Tk_d\phi_d(t)}{A_d} \quad (23)$$

where k_d is the gain of the phase detector. Substituting (23) in (22) yields (24).

$$v_{PWM}(t) = k_d\phi_d(t) + \frac{A_d}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\sin\left(n\omega_0 t\right) - \frac{1}{n}\sin\left(n\omega_0\left(t-\frac{Tk_d\phi_d(t)}{A_d}\right)\right)\right]. \quad (24)$$

After $v_{PWM}(t)$ passes through the low-pass filter, the magnitude and phase responses are (25) and (26), respectively.

$$\left|\frac{v_o(\omega)}{v_i(\omega)}\right| = \frac{1}{\sqrt{1+\left(\omega/\omega_c\right)^2}}, \quad (25)$$

$$\angle v_o = -\arctan\left(\frac{\omega}{\omega_c}\right) \quad (26)$$

where v_i is the magnitude of the input signal, v_o is the magnitude of the output signal, $\angle v_o$ is the output phase, and ω_c is the low-pass filter's cut-off frequency. The low-pass filter output for the input signal $v_{PWM}(t)$ is thus expressed in (27). By using the approximation $\sqrt{1+\left(n\omega_0/\omega_c\right)^2} \approx n\omega_0/\omega_c$, (27) can be rewritten as (28).

$$v_L(t) = k_d\phi_d(t) + \frac{A_d}{\pi}\sum_{n=1}^{\infty}\left[\frac{1}{n}\cdot\frac{1}{\sqrt{1+\left(\frac{n\omega_0}{\omega_c}\right)^2}}\sin\left(n\omega_0 t - \arctan\left(\frac{n\omega_0}{\omega_c}\right)\right) - \frac{1}{n}\cdot\frac{1}{\sqrt{1+\left(\frac{n\omega_0}{\omega_c}\right)^2}}\sin\left(n\omega_0\left(t-\frac{Tk_d\phi_d(t)}{A_d}\right) - \arctan\left(\frac{n\omega_0}{\omega_c}\right)\right)\right], \quad (27)$$

$$v_L(t) = k_d\phi_d(t) + \frac{A_d\omega_c}{\pi\omega_0}\sum_{n=1}^{\infty}\left[\frac{1}{n^2}\sin\left(n\omega_0 t - \arctan\left(\frac{n\omega_0}{\omega_c}\right)\right) - \frac{1}{n^2}\sin\left(n\omega_0\left(t-\frac{Tk_d\phi_d(t)}{A_d}\right) - \arctan\left(\frac{n\omega_0}{\omega_c}\right)\right)\right]. \quad (28)$$

By considering (28), it is clear that the first term is the DC component $k_d\phi_d(t)$ and that the second term is a triangular signal with asymmetric slopes, as illustrated in Fig. 9(b). From (28) and Fig. 9(b), the minimum and maximum error voltage range is found to lie between $-A_d\omega_c/\pi\omega_0$ and $+A_d\omega_c/\pi\omega_0$. The magnitude of the error voltage is thus expressed in (29). The PLL can support a maximum phase shift of π radians, corresponding to the highest output voltage of the low pass filter, A_d. Hence, according to (29), the magnitude of the phase error can be expressed by (30).

$$\left|V_{\text{error}}\right| = \frac{A_d\omega_c}{\pi\omega_0}, \quad (29)$$

$$\left|phase\ error\left(\theta_{\text{error}}\right)\right| = \frac{2\omega_c}{\omega_0}. \quad (30)$$

As shown in (30), the phase error is proportional to the low-pass filter's cut-off frequency. A technique to eliminate this phase error is currently under investigation.

5.1 Phase Noise

Phase noise in the proposed QPSK modulator, which is caused by the phase error signal or the amplitude fluctuation of the VCO input signal as described in (28), can be measured by considering the power spectral density $S(\omega)$ of the periodic phase error signal expressed in (31):

$$S(\omega)=\sum_{n=-\infty}^{\infty}|c_n|^2\,\delta(\omega-n\omega_0) \tag{31}$$

where $|c_n|$ is the magnitude of the spectrum, and ω_0 is the angular frequency of the signal. The phase error signal is the low-pass filter output signal, and the magnitude of the spectrum $|c_n|$ is calculated from coefficients a_n and b_n of the phase detector output signal as described in (32).

$$|c_n|=\sqrt{a_n^2+b_n^2}= \\ =\sqrt{\left(\frac{2A}{nT\omega_0}\sin\left(n\omega_0 t_p\right)\right)^2+\left(-\frac{2A}{nT\omega_0}\left[\cos\left(n\omega_0 t_p\right)-1\right]\right)^2}. \tag{32}$$

By letting $d = 2A/(nT\omega_0)$ and because $\sin^2(\theta/2) = ½(1-\cos\theta)$, (32) can be rewritten as (33).

$$|c_n|=2d\sin\left(\frac{n\omega_0 t_p}{2}\right). \tag{33}$$

By substituting (33) into (31), the PSD can be expressed as (34).

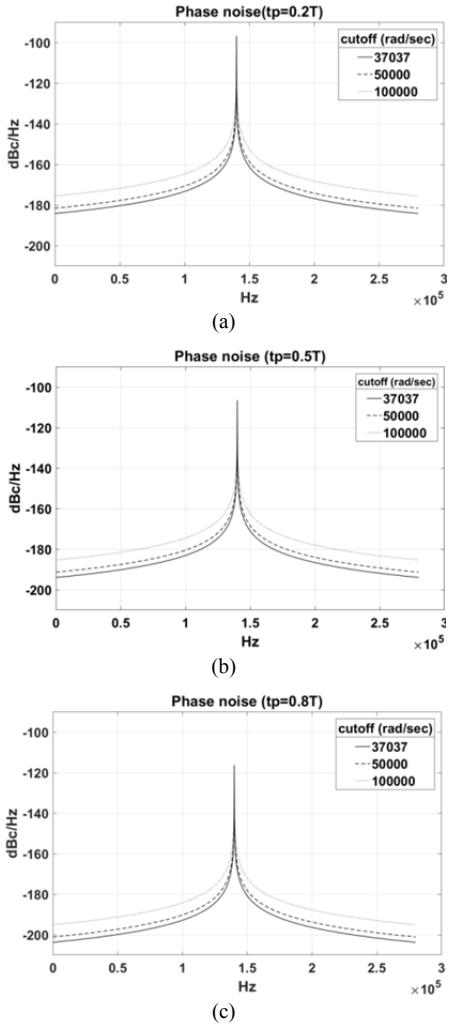


Fig. 10. Phase noise charts for different duty cycle values. (a) Phase noise for a duty cycle of 20%. (b) Phase noise for a duty cycle of 50%. (c) Phase noise for a duty cycle of 80%.

$$S(\omega)=\sum_{n=-\infty}^{\infty}4d^2\sin^2\left(\frac{n\omega_0 t_p}{2}\right)\delta(\omega-n\omega_0). \tag{34}$$

According to the transfer function of the low-pass filter described in (25), the PSD can be expressed by (35)

$$S_o(\omega)=\left|\frac{v_o(\omega)}{v_i(\omega)}\right|^2 S(\omega)= \\ =\frac{1}{1+(\omega/\omega_c)^2}\sum_{n=-\infty}^{\infty}\left(\frac{4A\sin\left(\frac{n\omega_0 t_p}{2}\right)}{nT\omega_0}\right)^2\delta(\omega-n\omega_0). \tag{35}$$

Thus, the phase noise can be described as (36)

$$phase\ noise=10\log\left(S_0(\omega)\right)= \\ =10\log\left[\frac{1}{1+\left(\frac{\omega}{\omega_c}\right)^2}\sum_{n=-\infty}^{\infty}\left(\frac{4A\sin\left(\frac{n\omega_0 t_p}{2}\right)}{nT\omega_0}\right)^2\delta(\omega-n\omega_0)\right]. \tag{36}$$

According to (36), phase noise charts, such as the ones presented in Fig. 10, can be generated, showing the inverse proportionality between the phase noise and the duty cycle t_p. As can be seen, the more the duty cycle is the less phase noise in the QPSK signal of the proposed scheme.

5.2 Error Vector Magnitude (EVM)

The concept of error vector magnitude (EVM) is explained in this subsection. An error vector is a vector in the I-Q plane between the error point (I_{error}, Q_{error}) and the ideal constellation point (I_{n}, Q_{n}), which can be calculated from the expression of QPSK as shown in (37):

$$s(t)=A\cos\left(\omega_c t+\theta_n\right) \tag{37}$$

which can be rewritten as (38)

$$s(t)=A\cos(\theta_n)\cos(\omega_c t)-A\sin(\theta_n)\sin(\omega_c t). \tag{38}$$

Hence, the ideal constellation point can be described by (39) and (40) as follows

$$I_n=A\cos(\theta_n), \tag{39}$$

$$Q_n=A\sin(\theta_n). \tag{40}$$

Likewise, the error point (I_{error}, Q_{error}) of the proposed QPSK technique can be described by (41) and (42)

$$I_{\text{error}}=A\cos(\theta_{\text{error}}), \tag{41}$$

$$Q_{\text{error}}=A\sin(\theta_{\text{error}}). \tag{42}$$

From (30), the calculated phase error (θ_{error}) is directly proportional to the LPF's cut-off frequency, which affects to the EVM.

$$EVM = \frac{\sqrt{\sum_{n=0}^{3}\left\{\left(I_{\text{error}} - I_n\right)^2 + \left(Q_{\text{error}} - Q_n\right)^2\right\}}}{\sum_{n=0}^{3}\left(I_n^2 + Q_n^2\right)}. \quad (43)$$

Using (43), the EVM ratios obtained from the theoretical calculations and the experimental results can be compared, as shown in Tab. 3. The cut-off frequency ω_c is inversely proportional to EVM value.

Low-pass filter cut-off frequency ω_c [rad/s]	EVM		
	Prediction	Simulation	Experimental
100,000	0.275	0.341	0.356
50,000	0.329	0.382	0.392
37,037	0.343	0.403	0.421

Tab. 3. Comparison of the error vector magnitude ratios.

6. Conclusion

In this article, a QPSK modulator was proposed based on a new scheme for phase shifting using a PLL. The PLL employed in the proposed technique is able to control phase shifting by using a summing circuit and an input DC level. It is also able to invert the phase of the QPSK signal by controlling the phase detector. In comparison to the conventional PLL circuit, the proposed system consists of a summing circuit between the loop filter and the VCO, and it uses a three-input phase detector instead of the conventional phase detector. Furthermore, the D/A component is not required in the proposed scheme, which differs from the conventional QPSK modulator circuit. The simulation and experimental results confirm that the proposed technique provides continuous phase shift in the QPSK signal. Hence, the bandwidth consumption of a QPSK signal obtained from the proposed QPSK modulator is less than that of a QPSK signal obtained from a conventional modulator. In addition, the time required for phase shifting when using the proposed technique is always constant, and thus, there are no complications in the implementation of the demodulation process. Furthermore, the phase-shifting speed can be adjusted by varying the cut-off frequency of the low-pass filter. From the study of phase noise and EVM, it is found that the cut-off frequency ω_c is inversely proportional to phase noise and EVM of the QPSK signal based on the proposed scheme.

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