An Effect of Output Capacitor ESL on Hysteretic PLL Controlled Multiphase Buck Converter

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Abstract. *This paper provides analysis of output capacitor effects to phase stability of a hysteretic mode controlled buck converter. The hysteretic control method is a simple and fast control technique for switched-mode converters, but the hysteresis control is not oscillator referenced. It results in difficulty to achieve stable switching phase and frequency. In recent papers, the authors propose a use of phase locked loops (PLL) to permit interleaved multiphase operation where each voltage regulator (VR) module is coupled together via output node and leads to a strong loop interaction. In this work analysis of this interaction is studied by Matlab Simulink simulations and a new solution how to partially suppress this effect is given. The proposed method confirms the theoretical analysis.*

Keywords

SMPS, Buck, hysteretic mode control, interleaving, PLL, multiphase

1. Introduction

Today's portable devices, such as smartphones, tablets, usually require decreasing their battery cell voltage to 1 V or even lower voltage level. Due to the quickly changing nature of the load, which is often determined by the software application, the supplies are required to have a fast dynamic response and high efficiency over the full range of operation. These requirements can be achieved by switching regulators that have been used in ICs for many years. These regulators are still considered tricky to design. Multi-phase buck topologies are being adopted to power the next generation portable electronics systems that require low supply voltage and high current in the order of units of amperes. PC motherboards use multiphase synchronous buck converters for a long time. Interleaving and phase-shedding techniques are pillars that help to improve efficiency and ripple cancellation effect. Several works have been recently focused on the hysteretic mode controlled SMPS (Switched-Mode Power Supply) converters [1–6]. This type of control grows in popularity for fast transient response. Moreover, designers have not to deal with frequency compensation, as the simplest form consists of a comparator. Thus its response to transients is limited only by the propagation delays in the comparator and gate driver in a power stage. The hysteretic mode controlled SMPS can be very simple and has many benefits as low quiescent power consumption, implement-ability, adapt-ability, etc. [7].

Beside the hysteretic control mode, commonly used strategies are voltage mode and various types of current mode. Since they take use of linear compensation network in a sampled data system, their maximum bandwidth is limited to 1/2 the switching frequency resulting from the Nyquist theorem. The bandwidth is designed much lower to reach sufficient stability. On the contrary, a hysteretic controller generates switching command directly by comparing the output and reference voltage. In Fig. 1, a small portion of inductor current ripple is fed into the comparator to improve noise immunity. When a robust control method like SMC (Sliding Mode Control) theory is used to design a hysteretic controller, then the output capacitor current instead of the inductor current is needed, since a variable and its first derivative, in this case, capacitor voltage and capacitor current are required for generating the switching function in agreement with SMC theory [8–10].

As the hysteretic converter is not oscillator referenced, some applications, especially electromagnetic-interference-sensitive applications, need a constant frequency. Thus additional circuitry is needed to control the switching frequency that could move up and down according to external conditions. There exist two possible ways: the first one is to feed-forward the switching frequency and do a suitable action, i.e., to compensate condition's changes without a closed loop system. This method has been published by Feng Su [1]. The second method, described by Chung-Hsien Tso [2], uses an adjusting loop which is controlled by PLL or FLL (Phase or Frequency Locked Loop) system. This paper focuses on the second solution, as the goal is to take advantage of the soft synchronization hysteretic mode control and the interleaved multiphase operation. The idea is to have phase and frequency under control in steady state operation. Synchronization may be lost during transients. Employing multiphase approach the ripple cancellation effect is achieved and as a result, the needed output capacitor value is reduced.

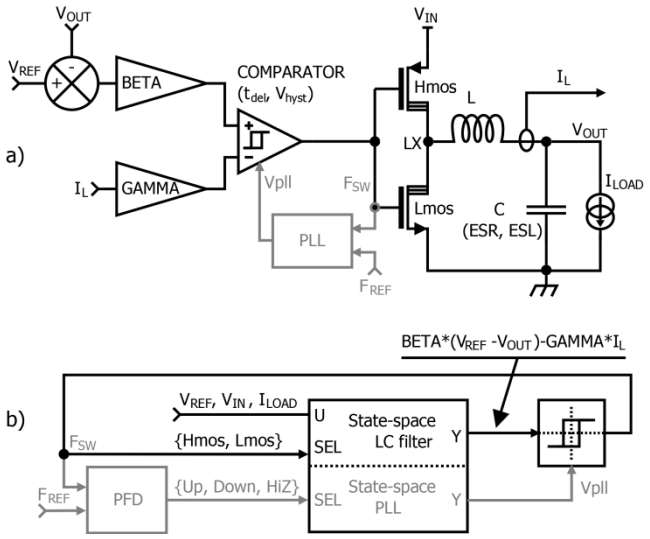

Fig. 1. Simplified hysteretic mode buck converter (a) and its Simulink model implementation (b).

This paper presents an observed issue of recently presented topology –hysteretic mode PLL controlled multiphase buck converter– and proposes how to deal with the described obstacles. The proposed design methodology is verified by simulation.

2. Basic Principles

2.1 Switching Frequency

Figure 1a) shows the simplified block diagram of the conventional hysteretic buck converter with the frequency changing loop depicted in gray. The switching action could be derived directly from the LX node or indirectly from the comparator output. The switching action is compared with a clock reference F_{REF} and the result V_{pll} is fed back into the main loop. The traditional approach described in [2], [5] uses the frequency loop adjusting the delay of the main comparator. The comparator hysteresis band is adjusted in another approach mentioned in [3]. Both approaches lead to switching frequency control. The switching frequency F_{SW} (1c) mainly depends on control scheme and component parameters, for more details see [4], [11]. The only condition for controllable frequency is the peak to peak voltage value across the output capacitor ESL (Equivalent Series Inductance) does not exceed the comparator hysteresis band V_{hyst}.

$$V_{\mathrm{hyst}} = -BETA \cdot \hat{V}_{\mathrm{hyst}} + GAMMA \cdot I_{\mathrm{L(p-p)}}, \tag{1a}$$

$$\hat{V}_{\mathrm{hyst}} = V_{\mathrm{C}} + V_{\mathrm{ESR}} + V_{\mathrm{ESL}}, \tag{1b}$$

$$F_{\mathrm{SW}} = \frac{V_{\mathrm{OUT}}(V_{\mathrm{IN}} - V_{\mathrm{OUT}})(ESR - \frac{t_{\mathrm{del}}}{C})}{V_{\mathrm{IN}}(V_{\mathrm{IN}} \cdot ESR \cdot t_{\mathrm{del}} + \hat{V}_{\mathrm{hyst}} \cdot L - ESL \cdot V_{\mathrm{IN}})}, \tag{1c}$$

$$VCO_{\mathrm{GAIN}} = \frac{\partial F_{\mathrm{SW}}}{\partial V_{\mathrm{hyst}}(V_{\mathrm{pll}})} = \frac{\partial F_{\mathrm{SW}}}{\partial t_{\mathrm{del}}(V_{\mathrm{pll}})} \tag{1d}$$

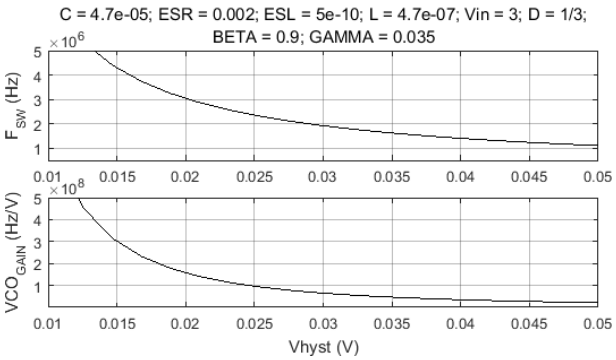

Fig. 2. Calculation of F_{sw} and VCO_{GAIN} as a function of V_{hyst} in a single-phase buck converter.

where *BETA* and *GAMMA* are gains of the voltage and current path respectively, V_{hyst} is hysteresis of the comparator, $I_{\mathrm{L(p-p)}}$ is inductor peak to peak current, *ESR*, *ESL* and *C* are components of the output capacitor RLC serial model, V_{C}, V_{ESR}, V_{ESL} are voltage differences on the output capacitor model components between start and end of the on/off-state. By rearranging the equations above, the gain of the voltage controlled oscillator VCO_{GAIN} can be extracted if $V_{\mathrm{hyst}}/V_{\mathrm{pll}}$ or $t_{\mathrm{del}}/V_{\mathrm{pll}}$ transfer characteristic is known. In our case the $V_{\mathrm{hyst}}/V_{\mathrm{pll}}$ ratio is ¼ and it is given by the comparator hysteresis generation, the comparator Vpll input consists of a small differential pair shadowing the comparator input differential pair. In Fig. 2, an example of the VCO behavior is shown; it can be seen that the switching frequency as a function of the hysteresis band is not linear.

Regarding the capacitor selection, the high ESR (Equivalent Series Resistance) provides enough ripple that stabilizes the converter, and brings information about the dynamics of the output voltage ($\mathrm{d}V_{\mathrm{out}}/\mathrm{d}t$ ~ capacitor current). In our case, we use Murrata MLCCs, two GRM21BR60J226ME39 in parallel or GRM31CR61A476KE15L. ESL and ESR value is very small, less than 0.5 nH and about 2 mΩ respectively. As the low ESR capacitor is used, some technique to substitute the low ESR drawback should be used. The most common techniques are:

1) RC ripple reconstruction networks [12], [13],
2) on-chip ramp generators [13].

It is not critical how the ESR is emulated; the problem is generalized in our case. The parameter *GAMMA* substitutes the lack of ESR.

2.2 PLL Design

A phase locked loop is a control system that generates a signal synchronized with an input signal. The VCO switching action is the synchronized signal and the input signal is a clock reference. Conventional PLL consists of a phase-frequency detector PFD, a charge pump CP, a compensating filter and a voltage controlled oscillator VCO. In this case, the hysteretic comparator overtakes the VCO function. The inverting and the non-inverting com-

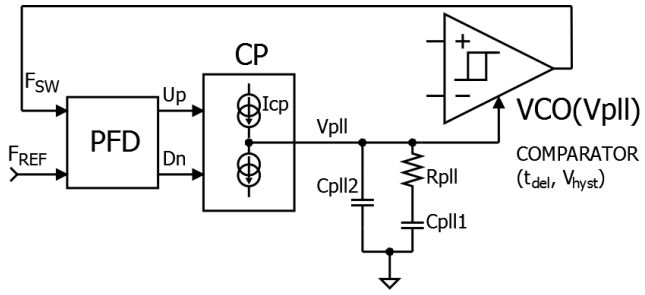

Fig. 3. Frequency loop identified in the hysteretic converter.

parator inputs are connected as mentioned before, input signal levels define gain of the VCO while the comparator setting input Vpll defines the switching frequency. The simplified structure of the frequency loop is depicted in Fig. 3. For further explanation of the system functionality, only the structure should be understood. Detailed explanations of the PLL design and compensation can be found in [14].

The main attention has been set on the interaction between the frequency and voltage regulating loop. For example, K. Lee in [3] uses a non-interaction principle, where both loops are designed and tuned separately. When the frequency loop UGB (Unity Gain Bandwidth) is low, it obviously takes much more time to recover after a transient in comparison with the high UGB setting. When load profile contains some frequency components that are higher than the frequency loop UGB, the frequency loop may never lock as a result. On the other hand, when the frequency loop UGB is too high, it may cause overshoots in output voltage. It compromises the overall design. The frequency loop UGB is a trade-off between converter dynamics and frequency stability.

2.3 Multiphase Configuration

A multiphase buck converter is depicted in Fig. 4. The given example consists of two same modules PH1 and PH2, additional modules would be connected in the same manner. In this case, there are two common nodes. The first one is interleaved clock reference defining phase and frequency setting. The second one is V_{OUT} node. There is a new phenomenon of VCO_{GAIN} variability caused by the loop and VR modules interactions. This was not observed in a single-phase configuration. This phenomenon has several possible causes: a module's mutual phase shift and ripple cancellation effect eliminating the common node output voltage ripple.

A range to which the VCO_{GAIN} changes is approximated by two states: the ideal interleaving state and the synchronous switching state. The higher one occurs when each VR modules switch simultaneously, the VCO_{GAIN} can be derived from (1) with a presumption that the modules are similar and the inductor value used in (1c) is divided by the number of modules. The lower range occurs when modules switching actions are uniformly shifted in time. The ripple cancellation effect manifests itself according to the duty cycle ratio D. The ripple cancellation reaches its

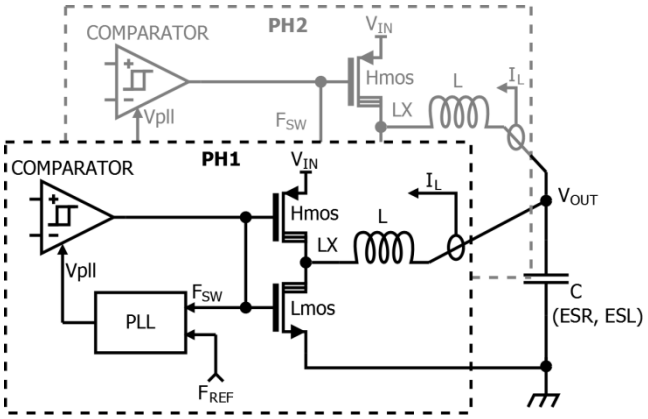

Fig. 4. Principle of multiphase configuration with PLL.

maximum when the sum of phase inductor currents is constant, for example, this happens when D = ½ in a 2-phase interleaved buck converter. The switching frequency is approximately estimated to be

$$F_{SW} = \frac{V_{OUT}}{2 \cdot L \cdot I_{L(p-p)}} = \frac{V_{OUT} \cdot GAMMA}{2 \cdot L \cdot V_{hyst}}. \quad (2)$$

The PLL loop needs to be redesigned to ensure functionality in both extremes. Since the converter is forced to switch interleaved in steady-state and also it is allowed to switch simultaneously, it is almost desirable to source the output as fast as possible to fulfill transient requirements. Therefore a study of VCO_{GAIN} behavior needs to be investigated.

2.4 Effect of Relative Phase Shift

Since now the focus has been given to the frequency estimation. Let's expect the switching frequency is close to the reference, and the interleaving has only left to be achieved. A Simulink model for the 2-phase buck converter was used to investigate V_{hyst} value in each converter module as a function of a mutual phase-shift. The mutual phase (labeled as phase error) starts in an ideal interleaving point and then it is slowly imbalanced from 0 to 162°. The simulated results of Phase error, Hysteresis bands with their difference ΔV_{hyst} are shown in Fig. 6, the simulation setting is on the top. It was set with the accent on clarity and the usage of the most common components. The crucial components are the output capacitor RLC model, inductor, supply voltage, duty cycle, voltage and current gains, switching frequency and PLL unity-gain-bandwidth with phase margin. A state-space representation [15] was used for converter implementation into Simulink. The principle is depicted in Fig. 1b). Each converter state is represented by one set of equations, and then the simulation is possible by dynamic changing of the state-space matrices.

The functionality of PLL is verified by forcing a phase shift, in Fig. 6a). Note that zero phase error means that modules are in an ideal interleaving position Fig. 5a). The VR tracks immediately the phase reference until the phase error reaches a critical phase shift value, where the

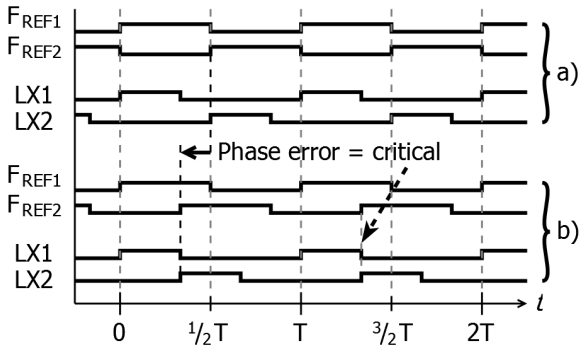

Fig. 5. Clock references and LX nodes waveforms in a 2-phase buck converter with $D = 1/3$, a) ideally interleaved, b) poorly interleaved.

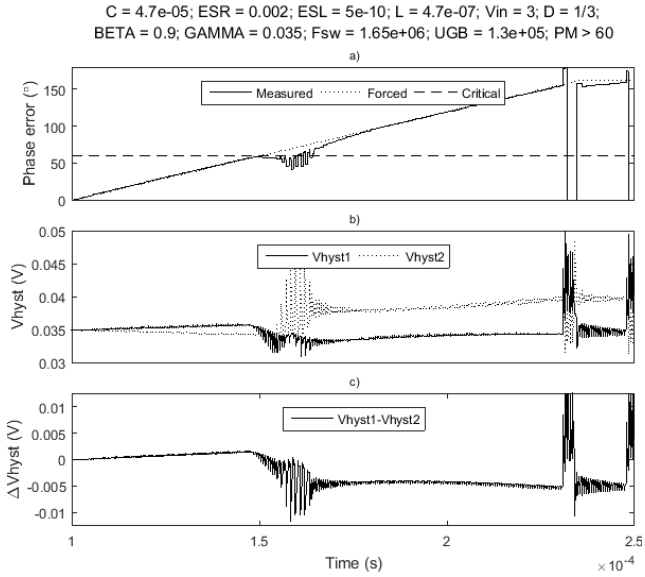

Fig. 6. Transient simulation of phase shifting in the 2-phase buck converter with $D = 1/3$.

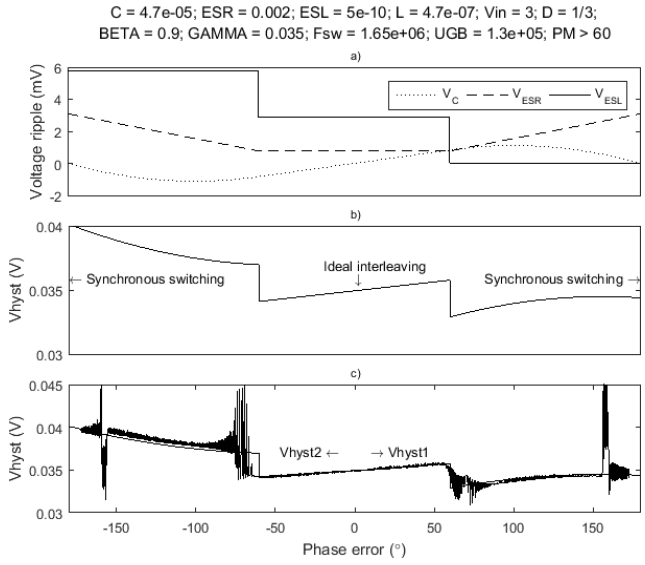

Fig. 7. Calculation of hysteresis band in the 2-phase buck converter.

hysteresis band jumps, and the PLL is facing a discontinuity. This can be seen in Fig. 6b), where V_{hyst1} and V_{hyst2} are relevant module hysteresis band setting. The critical value of phase shift is defined by the overlapping first occurrence in Fig. 5b), it is ±60° for the given duty cycle ratio D and two modules. Note that when both modules are forced to switch almost simultaneously, PLLs hardly control the switching sequence order, it is visible on the right side of Fig. 6. Due to the current distribution among modules, the phase error jumps between ±180° and it needs different hysteresis band setting. The purpose of this transient simulation is to confirm an assumption that the hysteresis setting V_{hyst} is a function of the module's mutual phase shift.

A calculated decomposition of the output voltage ripple seen on comparator inputs as a function of phase error is depicted in Fig. 7a), the decomposition is based on C, ESR and ESL output capacitor equivalent model. The basic setting is the same as was used in the transient simulation in Fig. 6. The current imbalance is not taken into account, i.e., both modules carry the same average power. The calculation was performed by shifting two ideal saw-tooth wave representing inductor currents. The voltage swings on C and ESR are continuous functions, and their amplitudes can be minimized by increasing C and by decreasing ESR respectively. The only discontinuity in the PLL is caused by the ESL and is proportional to the current slope in the inductor L during the switching cycle. The hysteresis voltage as a function of phase shift, in Fig. 7b), cannot be locally approximated by a linear function around the critical phase shift. Thus a non-linear system with a hard discontinuity is identified [16]. A current imbalance may explain a little difference between calculated and simulated results in Fig. 7c), the module with a forced phase advance should carry higher power in a realistic scenario.

2.5 Discontinuity Symptoms

The hard nonlinearity symptoms are manifested through oscillations of PLL, visible in Fig. 8. The ESL simulation setting is ten times enlarged to make the symptoms better visible. The interleaved operation is forced in the simulation. Initially, PLL tunes the switching frequency in a simulation time range between 30 to 50 µs.

The PLL is enabled before the end of the converter ramping phase, so that is why the hysteresis goes initially down, see Fig. 8b). The correct interleaved position searching event starts with 60° error. Here the ESL effect must be overcome. The ESL effect is independent of the switching frequency; it depends on L, ESL and Vin. The ESR effect is inversely proportional to the switching frequency. The switching frequency is usually given in order to optimize the converter efficiency. The converter modules are stuck together. When the second converter module goes into off-state the first converter module is initialized and goes into on-state regardless of a small change in the

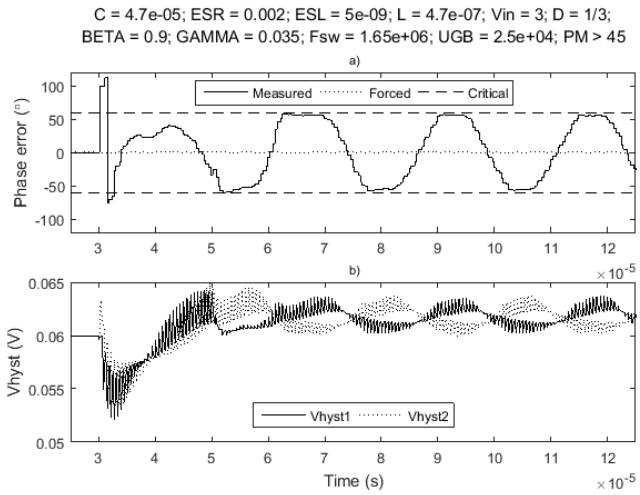

Fig. 8. Transient simulation of the 2-phase buck converter, PLL oscillations.

hysteresis setting. Each time the PLL integrates enough phase error to reach the ideal interleaving equilibrium, the conditions to stay in the equilibrium have been changed as much as the PLL cannot compensate. The PLL is facing to a periodic dead-zone phenomenon.

2.6 Elimination of the Observed Dead Zone

There are not many solutions how to handle a closed loop system in an equilibrium surrounded by two hard discontinuities. There are three intuitive solutions:

- tuning the PLL unity gain bandwidth,
- eliminating the ESL effect,
- compensating the ESL effect.

When the unity gain bandwidth is increased, the converter is more strongly locked with the clock reference and the line and load transient performances are decreased. Also, it may cause the loop to become unstable and permanently losing lock. The maximum recommended PLL unity gain bandwidth is 1/5 of the clock reference to avoid the discrete sampling effect of the phase detector on stability [14]. Moreover, there is a strong interaction between the voltage and phase frequency loop since phase shift affects the inductor current ratios. The overall system cannot be tuned separately. The exact solution is the object of future studies.

The target is to do the ESL effect negligible from the phase control loop point of view. It can be achieved by using low ESL MLCC (multi-layer ceramic capacitor).

The last way is to compensate V_{ESL} in the control loop which may cause obstacles during the real implementation, as a small voltage portion needs to be added into the control loop during each converter on-state. Another drawback is a need for exact values of ESL, L and slope of the inductor current which is V_{IN}, V_{OUT} dependent. The parameters mentioned above vary with a tolerance spread, temperature, assembling and supply demand which all makes a fixed estimation impossible. For evaluation of this theory, an estimator predicting the expected value of V_{ESL} by implementing (3c) is added into common voltage reference. The principal is depicted in Fig. 10. Note that this simple solution bias the voltage loop and thus it moves the output voltage from the desired value, it can be seen in Fig. 9, there are the output voltage $V_{\mathrm{OUT}*}$ seen from the comparator input point of view, the ripple cancellation effect reducing the output capacitor stress (reduced current I_{C}).

$$V_{\mathrm{ESL}} = ESL \cdot F_{\mathrm{SW}} \frac{I_{\mathrm{L(p-p)}}}{D(1-D)}, \tag{3a}$$

$$I_{\mathrm{L(p-p)}} = V_{\mathrm{OUT}} \frac{1-D}{L \cdot F_{\mathrm{SW}}}, \tag{3b}$$

$$V_{\mathrm{ESL}} = V_{\mathrm{IN}} \frac{ESL}{L}. \tag{3c}$$

There is a simulation of the improved solution in Fig. 11. It can be seen that the measured phase follows the forced phase without any glitch at the critical phase when the on-state commands start being overlapped. The simulation setting is similar with the setting used in Fig. 6 simulation. The ESL effect impact on converter instability is proven. Nevertheless, the components aging, temperature effects, coil saturation are not taken into account. It could be overcome by an on-chip L and ESL estimator circuit. The ESL measurement is almost impossible in our case. There are several parasitic inductances in the chain: two bonds (LX and GND pins), PCB (Printed Circuit Board)

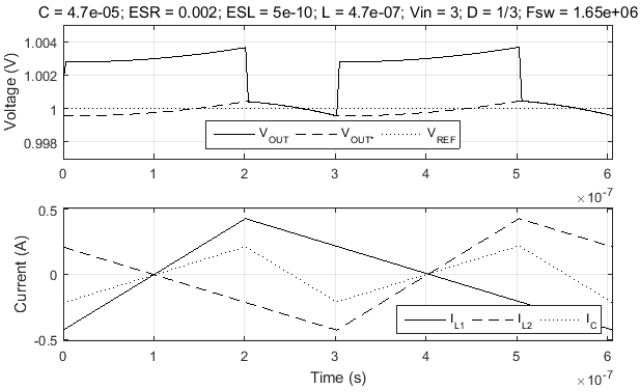

Fig. 9. Calculation of output voltage, inductor currents and output capacitor current in the improved 2-phase buck converter.

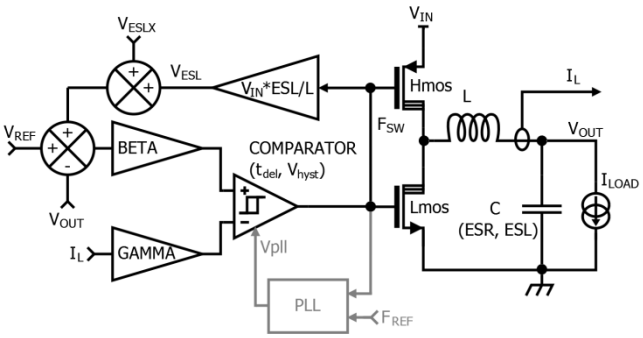

Fig. 10. Improved hysteretic mode buck converter.

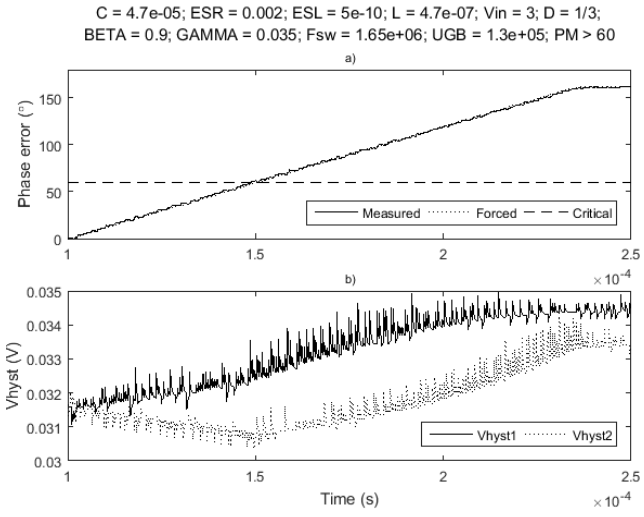

Fig. 11. Transient simulation of phase shifting in the improved 2-phase buck converter with $D = 1/3$.

and coil L. Unfortunately, there are many degrees of freedom and the transient simulations are very time-consuming. Notice, the relevant module hysteresis bands V_{hyst1} and V_{hyst2} seem noisy, the vertical axis is four-times zoomed against Fig. 6b) and thus the low simulation accuracy effects are better seen.

3. Conclusion

Instability study in the PLL controlled hysteretic mode multiphase buck converter has been presented in this paper. The main source of instability is given by the output voltage ripple which is output capacitor dependent. Some conditions which can lead to the instability are determined and analyzed. Consequences of the observed results are also discussed and three methods for suppression the root cause are proposed and compared. The proposed method was validated by Matlab Simulink. The simulation results are consistent with the theoretical assumptions.

Acknowledgments

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