A 28-nm 32 Kb SRAM For Low-$V_{\text{MIN}}$ Applications Using Write and Read Assist Techniques

Satyendra KUMAR 1, Kaushik SAHA 2, Hariom GUPTA 1

1 Dept. of Electronics and Communication Engineering, Jaypee Institute of Information Technology - Noida, India
2 Samsung R & D Institute India - Delhi, India

satyena.kumar@gmail.com, ksaha_2000@yahoo.com, hariom.gupta@jiit.ac.in

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Abstract. In this paper new write and read assist techniques, reduced coupling signal negative bitline (RCS-NBL) and low power disturbance noise reduction (LP-DNR) of 6T static random-access memory (SRAM) to improve its minimal supply voltage ($V_{\text{MIN}}$), have been presented. To observe the improvements in $V_{\text{MIN}}$ and power consumption of SRAM with the help of proposed assist techniques, a 32 Kb capacity SRAM, with 128 words of 256 bits width, is designed and simulated in 28-nm bulk CMOS technology. New RCS-NBL scheme, shows an improvement in SRAM write $V_{\text{MIN}}$ by 295mV and also reduces overstress on pass transistor (PG) of the selected bitcell by 40mV. Proposed LP-DNR scheme demonstrates an improvement in SRAM read $V_{\text{MIN}}$ by 35mV and also shows a saving of the power loss in the existing DNR scheme during the read access which occurs due to continuous flow of current from the cross coupled latch to the discharge block path after the bitlines have settled. The static power consumption of this SRAM macro is improved by 48.9% and 11.7% while dynamic power by 91.7% and 8.1% with the help of proposed write and read assist techniques respectively. Area overheads of these proposed RCS-NBL and LP-DNR assist techniques for this macro are less than 0.79% and 3.70% respectively.

Keywords
Low voltage, low power, SRAM, process variation, write assist, read assist, disturbance noise reduction (DNR)

1. Introduction

In advanced nanometer CMOS technologies, reduction of minimal supply voltage ($V_{\text{MIN}}$) and chip-area are the primary concerns of SRAM design. The reduction in $V_{\text{MIN}}$ of the SRAM cell for scaled devices is limited because of the local threshold voltage variations resulting from random dopant fluctuations and lithographic-dependent patterns have been increasing [1]. Also, with the increased threshold voltage variations in scaled transistors the access-disturbance margin (ADM) [2] and write margin (WM) [3] of the SRAM bitcell have been degrading. Process variations make SRAM design less predictable and controllable, moreover the SRAM design space in terms of prediction and control degrades further as supply voltage ($V_{\text{DD}}$) scales down [5]. Meanwhile, to improve the data stability of the bitcell, dual supply voltage schemes have been suggested [6], [7]. These schemes use higher supply voltage for bitcell array and lower supply voltage for peripheral blocks to improve the ADM of an SRAM. Write margin (WM) of an SRAM bitcell, has been improved by pushing selected bitline to negative voltage or by decreasing the cell voltage [2]. Now a days SRAM read and write assist techniques are widely used approaches to lower the $V_{\text{MIN}}$ of an SRAM [8]. Firstly, with the help of read and write assist techniques SRAM stability and write ability have been increased from their minimum respective levels required for proper read and write in SRAM without any assist techniques, which allows us to reduce the corresponding SRAM $V_{\text{MIN}}$ until the SRAM stability and write ability touch their respective original levels. In this paper, we present 28-nm bulk CMOS technology based 32 Kb 6T SRAM, featuring low $V_{\text{MIN}}$ with new write and read assist techniques. The focus has been to reduce the $V_{\text{MIN}}$ of SRAM since it is one of the most effective approaches to reduce dynamic as well as static power of SRAM.

Remaining part of this paper is organized as follows. Section 2 describes the conventional SRAM assist schemes. Section 3 elaborates the proposed reduced coupling signal negative bitline (RCS-NBL) scheme. Section 4 discusses the proposed low power disturbance noise reduction (LP-DNR) scheme. Section 5 deals with the impact of process variation on various SRAM parameters. Section 6 demonstrates the implementation and simulation results. Finally, we conclude in Sec. 7.

2. SRAM Assist Schemes

As shown in Fig. 1 conventional SRAM assist techniques are categorized into write and read assist schemes.
2.1 Write Assist Schemes

The techniques which aid the bitcell in changing the state during write operation are called write assist techniques and now these techniques are widely used in most low power SRAMs. The basic idea behind the write assist scheme is to decrease the ratio of strength of pull-up transistor to pass transistor of an SRAM cell when the wordline (WL) of the cell is enabled for write operation.

Conventional SRAM write assist schemes are categorized into following four techniques depending on the approach used to lower the ratio of pull-up to pass transistor strength of an SRAM cell during the write operation. Negative bitline (NBL) scheme, Wordline overdrive (WLOD) scheme, Lowering cell V_DD voltage (V_DDCELL) (LCV) scheme [2] and Raising cell ground voltage (V_SSCELL) (RCGV) scheme. Figure 1(a) shows the schematic of an 6T SRAM bitcell and Fig. 1(b) shows these conventional write assist techniques to enhance the write ability of the SRAM bitcell. In NBL scheme the selected bitline is pushed to negative voltage during write operation, which results in an increase of V_GS of the corresponding pass transistor hence the strength of this pass transistor has been enhanced, this improves the WtM of the cell. While in WLOD scheme the strength of pass transistor is increased by boosting the WL voltage i.e. the gate voltage of the pass transistor. In LCV scheme, the strength of pull-up device is reduced by lowering the source voltage (V_DDCELL) of pull-up devices while keeping wordline voltage (V_WL) at V_DD. In RCGV scheme also, the same idea is used to weaken the pull-up device, but in this case it is achieved by weakening the pull-up gate voltage instead of the source voltage, which is realized by raising the V_SSCELL, during the write operation.

2.2 Read Assist Schemes

The read disturb problem can be mitigated by adding a dedicated read port to isolate the bitcell internal nodes from the bitlines, but these resulting 7T, 8T, 9T and 10T SRAM bitcells [9–13] occupy larger area. The access-disturbance margin (ADM) can be improved by reducing the amount of
charge injection from the pre-charged bitline to the ‘0’ node of the active bitcell. This can be achieved by reducing the strength of pass transistor and/or bitline capacitance with slow WL rise [14], [15]. Figure 1(c) shows conventional SRAM read assist scheme, WL underdrive (WLUD), used to improve the ADM of an SRAM bitcell by reducing the strength of the pass transistor.

3. Proposed Reduced Coupling Signal Negative Bitline Scheme

In this work, NBL technique is being used as write assist scheme, since this is the most effective technique to reduce the SRAM $V_{\text{MIN}}$ [16]. Also, this technique shows highest WM without reducing the ADM of the half selected bitcells [2]. To realize NBL write assist scheme, capacitive coupling signal (CCS) approach shown in Fig. 2(a) is being used, which generates negative voltage at the bitline supposed to get down for write operation. In this scheme ENB_NBL signal propagates to NBL_FIRE signal as the falling edge of ENB_NBL signal triggers the fall of NBL_FIRE signal from the voltage level it was sitting before. The NBL_FIRE signal is coupled to negative bias (NVSS) signal through capacitor $C_1$. The pre-charged voltage level of NBL_FIRE signal before it starts to fall is one of the key parameters to determine the negative bias (NVSS) voltage level, which means that for higher $V_{\text{DD}}$ operation the generated voltage level of NVSS signal will be more negative. As shown in Fig. 3(a) with the help of write driver and column multiplexer, NVSS signal is applied to the selected bitline. Thus, coupling technique produces higher negative bitline bias level for higher $V_{\text{DD}}$ operation but there are two main disadvantages of higher negative voltage level at bitline, one stability concern of the half-selected bitcells in the same column and the other one is over stress on pass transistor of the selected bitcell, which is connected to this negative biased bitline, as for this pass transistor $V_{\text{DS}}$ is too large, and this over stress condition is also getting worse for high $V_{\text{DD}}$ operation [1].

To address these two issues, reduced coupling signal (RCS) circuit as shown in Fig. 2(b) is proposed here as write assist scheme. In this scheme, the voltage level of NBL_FIRE signal is reduced with the help of coupling voltage reduction block shown in this figure.

With the reduction in voltage level of NBL_FIRE signal, the negative bias (NVSS) signal level is reduced and hence negative bitline voltage level is reduced. In this work, 32 Kb SRAM with column mux (CM) = 8 i.e. an SRAM with physical rows (PR)=128 and physical columns (PC)=256 has been simulated with CCS-NBL, proposed RCS-NBL and state of the art SCS-NBL [1] write assist schemes. In CM=8 configuration 8-columns of bitcells are muxed with single write driver and hence single write assist block as shown in Fig.3(a). Simulated waveforms are plotted in Fig. 3(b) and 3(c) for comparison of CCS-NBL with RCS-NBL scheme, and RCS-NBL with SCS-NBL schemes respectively. Figure 3(b) and 3(c) demonstrate that the negative voltage level of NVSS is reduced by 40 mV with the help of RCS-NBL scheme as well as SCS-NBL scheme, and which has resulted in reduction of negative bitline voltage by same amount, this reduction will be more significant for higher $V_{\text{DD}}$ operation. Thus RCS-NBL and SCS-NBL schemes ad-
dress both the issues mentioned above. However, as shown in Fig. 3(c) proposed RCS-NBL scheme also improves the performance of write operation of the bitcell as compared to SCS-NBL scheme, because in this scheme the generation of NVSS signal can be triggered at the same time when CLKW signal rises from ‘0’ to ‘1’ while in the case of SCS-NBL scheme generation of NVSS signal will be initiated after At time to get same assist level as in the case of RCS-NBL scheme. With $6\sigma$ process variation, simulation results shown in Fig. 4 demonstrate the improvement in SRAM write $V_{MIN}$ with NBL techniques. In this figure, blue plot shows the required bitline voltage to write the bitcell, red, green and black plots represent coupled NBL voltage levels with CCS-NBL, proposed RCS-NBL and SCS-NBL techniques, respectively. Points A and B represent SRAM write $V_{MIN}$ without and with write assist techniques respectively. It can be observed from this figure that the proposed RCS-NBL as well as the SCS-NBL write assist technique demonstrate improvement in SRAM write $V_{MIN}$ by 295 mV.

4. Proposed Low Power Disturbance Noise Reduction (LP-DNR) Scheme

Read assist scheme WLUD improves the stability of half-selected bitcells but degrades both the read and write performances of selected bitcell [4]. Further WLUD scheme also shows rise in access time of bitcell with reducing $V_{MIN}$, then to improve the $V_{MIN}$, disturbance noise reduction (DNR) scheme was proposed as read assist scheme [2]. In this scheme, both the bitlines are lowered simultaneously, before the WL is activated to reduce the level of noise injection to the bitcell nodes, by discharging through clamping and discharge blocks. With lowering the bitlines voltage level at WL enabled time ADM increases to a certain level and thus the bitlines voltage level at which ADM is getting its maximum value, is defined as bitline safe-voltage level ($V_{SAFE}$).

However, ADM degrades drastically as bitline voltage level goes below $V_{SAFE}$ [2]. Figure 5 shows the plot of simulated results of ADM versus bitline voltage level at WL enabled time with $6\sigma$ process variation for the bitcell being used in this work and these results also endorse the same trend of steep degradation of ADM with bitline voltage level below $V_{SAFE}$. Thus to ensure enough data stability of the selected bitcells, proposed circuit must provide bitline voltage level at WL enable timing, more than or equal to $V_{SAFE}$ but not below it. Hence here for $6\sigma$ process variation cross-coupled latch, clamping and discharge circuits have been designed to keep bitline lowest voltage level to $V_{SAFE}$. Figure 6 shows the simulated results of bitline voltage level provided by DNR block with process variation ($\sigma$).

Fig. 4. Simulated write $V_{MIN}$ for the NBL schemes.

Fig. 5. Simulation result of ADM(V) versus bitline voltage level (V) for $6\sigma$ process variation.

Fig. 6. Simulated minimum bitline voltage(V) at WL rise time with process variation($\sigma$).
latch for which this bitline is acting as its gate. Thus as per the action of cross-coupled latch, this bitline goes down to ‘0’ and other one goes to (VSAFE+ΔV). PMOS which is ON keeps one of the two bitlines at (VSAFE+ΔV) for the period WL enabled time to the time at which the bitline is pre-charged to VDD again. For this period, pass transistor of the bitcell connected to the same bitline supplies current to it since this pass transistor is working very close to the subthreshold region. Thus, during this time period, a sum of ILOSS path shut-off circuit, subsequently shut-off signal pulls the bitline BT enough low to turned-on PMOS P10 devices, which results in stop of the flow of ILoss but in case of DNR scheme this flow continues throughout SHUT_PCH window. In proposed LP-DNR scheme, as the flow of ILOSS is blocked by turning off P2 device, the bitline BB starts to charge towards VDD while BT remains at 0V, finally bitlines, BB & BT are synchronized with cell data, hence neither ‘1’ noise nor ‘0’ noise can inject to the cell which results in highest stability of the bitcell. Also, with this synchronization of bitlines with cell data the active current drawn from power supply VDD is diminished.

5. Impact of Process Variability

In modern technologies intrinsic device variability of scaled devices dominates the traditional (worst-case) overall process spread that is generally used to determine the design window for the digital design community [17]. Transistor threshold voltage standard deviation \( \sigma V_T \) can be used to represent the intrinsic device variability, which is expressed as follows [18]

\[
\sigma V_T = 3.19 \times 10^{-6} \frac{\sqrt{L}}{W} A_{eff}^{0.401} [V]. \tag{1}
\]

To simulate various SRAM parameters, with the impact of process variation, \( \sigma V_T \) for all the concerned devices have been obtained using (1).

The simulation results for 6.5\( \sigma \) weak bitcell, shown in Fig. 8 demonstrate the need of LP-DNR circuit to combat the access disturbance of the cell. For SRAM read operation bitlines are pre-charged to VDD before the access of the cell, and access of the cell is obtained by turning ON pass transistors (PG1,PG2) of the cell by enabling WL. Figure 8(a) shows the simulated waveforms for read operation, as the bitcell is accessed, noise from BT will be injected to the cell storage node XT storing ‘0’ data before this access of the cell, thus XT node voltage rises to the voltage level which is sufficient to flip the cell, which results in functional failure. Further, the required voltage level at XT to flip the cell is also degrading as the cell gets weaker due to process variation. Figure 8(b) shows that the bitlines are lowered by LP-DNR circuit before the access of the cell hence the level of noise injection from BT to bitcell node XT storing ‘0’ data before the access of the cell, is reduced which results in successful read operation of the cell.

Simulation results shown in Fig. 9, demonstrate the improvement in read VMIN with the help of LP-DNR and DNR schemes respectively. In this figure, green curve shows the
Fig. 8. LP-DNR effect on disturbance failure for weak bitcell
(a) Simulated waveform without LP-DNR (b) Simulated waveform with LP-DNR.

Fig. 9. Simulated read $V_{\text{MIN}}$ for LP-DNR and DNR schemes.

minimum bitline voltage for non-destructive read operation of the cell, blue and red curves represent the bitline voltage level provided by LP-DNR and DNR schemes respectively. Here points A and B are representing SRAM read $V_{\text{MIN}}$ without and with read assist techniques, respectively. It can be observed from these results that with the help of both the proposed as well as the DNR scheme, SRAM read $V_{\text{MIN}}$ has improved by 35 mV.

Fig. 10. Layout of 6T SRAM bitcell (a). Layout of 3×3 miniarray for 6T SRAM cell (b).

Fig. 11. Layout of Capacitive coupling signal (CCS) circuit (a) and proposed Reduced coupling signal (RCS) circuit (b).

6. Implementation and Simulation Results

In this paper, all the layouts have been carried out using Synopsys Custom Designer Layout Editor (CDLE) and verified for DRC and LVS checks using IC Validator for 28-nm CMOS technology node while the RC parasitic extraction has been done using Synopsys Tool STAR-RC for the same technology node. Layouts of 6T SRAM bitcell as well as 3×3 miniarray are shown in Fig. 10(a) and (b).

Parasitics of centred 6T-SRAM bitcell of miniarray have been deduced from the extracted netlist of miniarray. Fig-
Figures 11(a) and (b) show the layouts of capacitive coupling signal (CCS) circuit and proposed reduced coupling signal (RCS) circuit respectively. Layouts of DNR and LP-DNR circuits are as shown in Fig. 12(a) and (b). In this work, the simulation setup for 32 Kb SRAM with CM=8, is made using center decode architecture as shown in Fig. 13. To get the loading netlist for this SRAM instance each bitcell in array is replaced by its extracted netlist deduced from miniaarray as discussed above. To observe the impact of proposed assist schemes with respect to no assist circuits and with assist circuits, extracted netlists for existing assist circuits, CCS and DNR have been used. For the proposed assist circuits RCS-NBL and LP-DNR, extracted netlists of the respective blocks have been used.

Fig. 13. Architecture used for simulation 32 Kb SRAM.

Figure 14 depicts the sigma-qualification of SRAM. In this figure, red square, blue dot and green rhombus represent SRAM $V_{\text{MIN}}$ to qualify for a particular level of process variation ($\sigma$) for no write assist scheme, with proposed write assist scheme (RCS-NBL) and for retention mode, respectively.

Power numbers along with $V_{\text{MIN}}$ of above mentioned SRAM macro, collected with the help of simulations, for respective write assist and read assist schemes as well as without assist schemes are shown in Tab. 1 (a) and (b) respectively.

<table>
<thead>
<tr>
<th>SCHEME</th>
<th>$V_{\text{MIN}}$ (V)</th>
<th>POWER (µW)</th>
<th>DYNAMIC</th>
<th>STATIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/O WRITE ASSIST</td>
<td>0.905</td>
<td>975</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>CCS-NBL</td>
<td>0.61</td>
<td>75.2</td>
<td>9.82</td>
<td></td>
</tr>
<tr>
<td>RCS-NBL</td>
<td>0.61</td>
<td>81.3</td>
<td>11.3</td>
<td></td>
</tr>
<tr>
<td>State of the art (CCS-NBL)</td>
<td>0.61</td>
<td>76.2</td>
<td>9.82</td>
<td></td>
</tr>
</tbody>
</table>

(a)

<table>
<thead>
<tr>
<th>SCHEME</th>
<th>$V_{\text{MIN}}$ (V)</th>
<th>POWER (µW)</th>
<th>DYNAMIC</th>
<th>STATIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/O READ ASSIST</td>
<td>0.834</td>
<td>311</td>
<td>26.31</td>
<td></td>
</tr>
<tr>
<td>LP-DNR</td>
<td>0.799</td>
<td>286</td>
<td>23.20</td>
<td></td>
</tr>
<tr>
<td>State of the art (DNR)</td>
<td>0.799</td>
<td>334</td>
<td>23.21</td>
<td></td>
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</tbody>
</table>

(b)
Tab. 2. Static power-improvement with assist circuits.

7. Conclusions

We have proposed new write and read assist circuits, RCS and LP-DNR respectively, to improve SRAM $V_{MIN}$ for 28-nm bulk CMOS technology. Simulation results with 6σ process variation for 32 Kb SRAM CM=8 macro, demonstrate that SRAM write $V_{MIN}$ is lowered to 0.61 V, which is an improvement of 295 mV with respect to without any write assist scheme.

SRAM read $V_{MIN}$ has been lowered to 0.799 V, which is an improvement of 35 mV as compared to without any read assist scheme. Table 2 summarizes the improvements in the respective SRAM $V_{MIN}$, dynamic power and static power consumption for this SRAM macro with the help of corresponding assist techniques.

LP-DNR scheme also improves dynamic power consumption by 16.8 % as compared to DNR scheme, while in the case of RCS-NBL scheme dynamic power consumption degrades by 6.3 % as compared with SCS-NBL write assist scheme. Over stress on PG transistor of selected bitcell as well as the stability issue of half-selected bitcells in the existing CCS-NBL scheme especially at higher operating voltages has been addressed in the proposed RCS-NBL scheme at the cost of power degradation during the short duration of clock inactive window. Area overheads of these proposed RCS-NBL and LP-DNR assist techniques for this macro are less than 0.79 % and 3.70 % respectively.

References


About the Authors . . .

Satyendra KUMAR was born in Muzaffarnagar, India. He obtained his B.E. and M.Tech. degrees from Indian Institute of Technology, Roorkee, India, in 1998 and 2002 respectively. He is currently working as Assistant Professor in the Department of Electronics and Communication Engineering at Jaypee Institute of Information Technology, Noida, India. Previously, he has worked in the semiconductor industry on a number of projects for development and characterization of 90nm, 65nm and 55 nm memory compilers for different foundries like TSMC, IBM, UMC and others. His research interests include SRAM Design For Low Power Applications.

Kaushik SAHA was born in Kolkata, India. He received his B.Tech., M.Tech. and Ph.D. degrees from Indian Institute of Technology, Delhi, India, in 1987, 1989 and 1996 respectively. In 1996 he joined STMicroelectronics Ltd., as a designer of semiconductor memories. At present he is Chief Technology Officer, Advanced Software Team, Samsung R&D Institute India, Delhi. His research interests are in the areas of Advanced Processor Architectures and Low voltage SoC design. He is also associated with the Indian Institute of Technology, Delhi, India, in the capacity of Adjunct Faculty, teaching advanced topics in VLSI design. He has published a number of papers in reputed journals.

Hariom GUPTA was born in Agra, India. He obtained his B.E. in Electrical Engineering from the Government Engineering College, Jabalpur, India. He received his M.E. and Ph.D. from Indian Institute of Technology, Roorkee in 1975 and 1980, respectively. Presently he is working as Director, Jaypee Institute of Information Technology, Noida, India. He has published over 300 research papers and 35 technical reports. His total citations are over 2300. He has supervised 31 Ph.Ds.