A 28-nm 32 Kb SRAM For Low-V_{MIN} Applications Using Write and Read Assist Techniques

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Abstract. *In this paper new write and read assist techniques, reduced coupling signal negative bitline (RCS-NBL) and low power disturbance noise reduction (LP-DNR) of 6T static random-access memory (SRAM) to improve its minimal supply voltage (V_{MIN}), have been presented. To observe the improvements in V_{MIN} and power consumption of SRAM with the help of proposed assist techniques, a 32 Kb capacity SRAM, with 128 words of 256 bits width, is designed and simulated in 28-nm bulk CMOS technology. New RCS-NBL scheme, shows an improvement in SRAM write V_{MIN} by 295 mV and also reduces overstress on pass transistor (PG) of the selected bitcell by 40 mV. Proposed LP-DNR scheme demonstrates an improvement in SRAM read V_{MIN} by 35 mV and also shows a saving of the power loss in the existing DNR scheme during the read access which occurs due to continuous flow of current from the cross coupled latch to the discharge block path after the bitlines have settled. The static power consumption of this SRAM macro is improved by 48.9 % and 11.7 % while dynamic power by 91.7 % and 8.1 % with the help of proposed write and read assist techniques respectively. Area overheads of these proposed RCS-NBL and LP-DNR assist techniques for this macro are less than 0.79 % and 3.70 % respectively.*

Keywords

Low voltage, low power, SRAM, process variation, write assist, read assist, disturbance noise reduction (DNR)

1. Introduction

In advanced nanometer CMOS technologies, reduction of minimal supply voltage (V_{MIN}) and chip-area are the primary concerns of SRAM design. The reduction in V_{MIN} of the SRAM cell for scaled devices is limited because of the local threshold voltage variations resulting from random dopant fluctuations and lithographic-dependent patterns have been increasing [1]. Also, with the increased threshold voltage variations in scaled transistors the access-disturbance margin (ADM) [2] and write margin (WM) [3] of the SRAM bitcell have been degrading. Process variations make SRAM design less predictable and controllable, moreover the SRAM design space in terms of prediction and control degrades further as supply voltage (V_{DD}) scales down [5]. Meanwhile, to improve the data stability of the bitcell, dual supply voltage schemes have been suggested [6], [7]. These schemes use higher supply voltage for bitcell array and lower supply voltage for peripheral blocks to improve the ADM of an SRAM. Write margin (WM) of an SRAM bitcell, has been improved by pushing selected bitline to negative voltage or by decreasing the cell voltage [2]. Now a days SRAM read and write assist techniques are widely used approaches to lower the V_{MIN} of an SRAM [8]. Firstly, with the help of read and write assist techniques SRAM stability and write ability have been increased from their minimum respective levels required for proper read and write in SRAM without any assist techniques, which allows us to reduce the corresponding SRAM V_{MIN} until the SRAM stability and write ability touch their respective original levels. In this paper, we present 28-nm bulk CMOS technology based 32 Kb 6T SRAM, featuring low V_{MIN} with new write and read assist techniques. The focus has been to reduce the V_{MIN} of SRAM since it is one of the most effective approaches to reduce dynamic as well as static power of SRAM.

Remaining part of this paper is organized as follows. Section 2 describes the conventional SRAM assist schemes. Section 3 elaborates the proposed reduced coupling signal negative bitline (RCS-NBL) scheme. Section 4 discusses the proposed low power disturbance noise reduction (LP-DNR) scheme. Section 5 deals with the impact of process variation on various SRAM parameters. Section 6 demonstrates the implementation and simulation results. Finally, we conclude in Sec. 7.

2. SRAM Assist Schemes

As shown in Fig. 1 conventional SRAM assist techniques are categorized into write and read assist schemes.

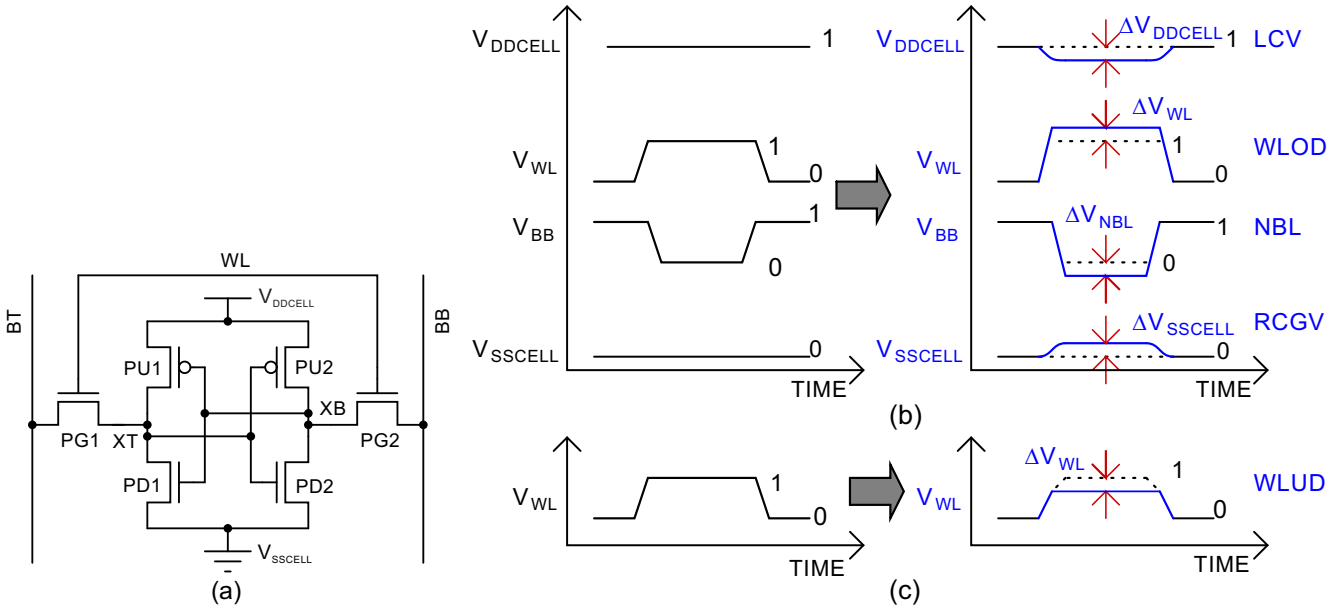


Fig. 1. (a) SRAM bitcell. (b) Timing diagram of write-assist techniques LCV, WLOD, NBL [2] and RCGV technique (c) Timing diagram of read-assist technique WLUD.

2.1 Write Assist Schemes

The techniques which aid the bitcell in changing the state during write operation are called write assist techniques and now these techniques are widely used in most low power SRAMs. The basic idea behind the write assist scheme is to decrease the ratio of strength of pull-up transitor to pass transistor of an SRAM cell when the wordline (WL) of the cell is enabled for write operation.

Conventional SRAM write assist schemes are categorized into following four techniques depending on the approach used to lower the ratio of pull-up to pass transistor strength of an SRAM cell during the write operation. Negative bitline (NBL) scheme, Wordline overdrive (WLOD) scheme, Lowering cell V_{DD} voltage (V_{DDCELL}) (LCV) scheme [2] and Raising cell ground voltage (V_{SSCELL}) (RCGV) scheme. Figure 1(a) shows the schematic of an 6T SRAM bitcell and Fig. 1(b) shows these conventional write assist techniques to enhance the write ability of the SRAM bitcell. In NBL scheme the selected bitline is pushed to negative voltage during write operation, which results in an increase of V_{GS} of the corresponding pass transistor hence the strength of this pass transistor has been enhanced, this improves the WM of the cell. While in WLOD scheme the strength of pass transistor is increased by boosting the WL voltage i.e. the gate voltage of the pass transistor. In LCV scheme, the strength of pull-up device is reduced by lowering the source voltage (V_{DDCELL}) of pull-up devices while keeping wordline voltage (V_{WL}) at V_{DD}. In RCGV scheme also, the same idea is used to weaken the pull-up device, but in this case it is achieved by weakening the pull-up gate voltage instead of the source voltage, which is realized by raising the V_{SSCELL}, during the write operation.

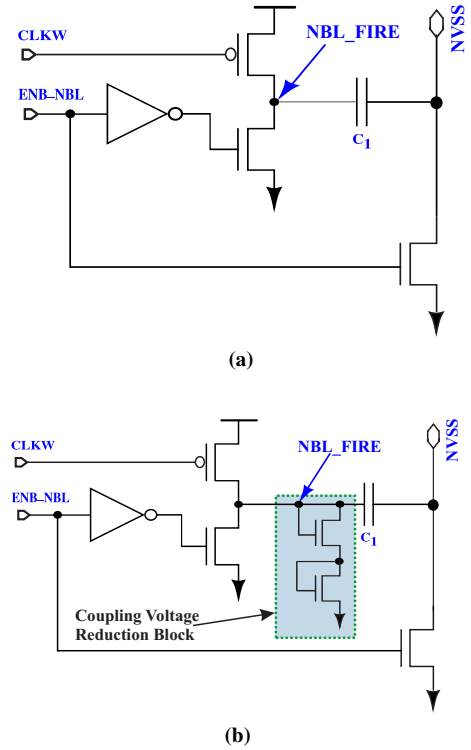


Fig. 2. Schematic of (a) Capacitive coupling signal (CCS) circuit (b) Proposed Reduced coupling signal (RCS) circuit.

2.2 Read Assist Schemes

The read disturb problem can be mitigated by adding a dedicated read port to isolate the bitcell internal nodes from the bitlines, but these resulting 7T, 8T, 9T and 10T SRAM bitcells [9–13] occupy larger area. The access-disturbance margin (ADM) can be improved by reducing the amount of

charge injection from the pre-charged bitline to the '0' node of the active bitcell. This can be achieved by reducing the strength of pass transistor and/or bitline capacitance with slow WL rise [14], [15]. Figure 1(c) shows conventional SRAM read assist scheme, WL underdrive (WLUD), used to improve the ADM of an SRAM bitcell by reducing the strength of the pass transistor.

3. Proposed Reduced Coupling Signal Negative Bitline Scheme

In this work, NBL technique is being used as write assist scheme, since this is the most effective technique to reduce the SRAM V_{MIN} [16]. Also, this technique shows highest WM without reducing the ADM of the half selected bitcells [2]. To realize NBL write assist scheme, capacitive coupling signal (CCS) approach shown in Fig. 2(a) is being used, which generates negative voltage at the bitline supposed to get down for write operation. In this scheme ENB_NBL signal propagates to NBL_FIRE signal as the falling edge of ENB_NBL signal triggers the fall of NBL_FIRE signal from the voltage level it was sitting before. The NBL_FIRE signal is coupled to negative bias (NVSS) signal through capacitor C_1. The pre-charged voltage level of NBL_FIRE signal before it starts to fall is one of the key parameters to determine the negative bias (NVSS) voltage level, which means that for higher V_{DD} operation the generated voltage level of NVSS signal will be more negative. As shown in Fig. 3(a) with the help of write driver and column multiplexer, NVSS signal is applied to the selected bitline. Thus, coupling technique produces higher negative bitline bias level for higher V_{DD} operation but there are two main disadvantages of higher negative voltage level at bitline, one stability concern of the half-selected bitcells in the same column and the other one is overstress on pass transistor of the selected bitcell, which is connected to this negative biased bitline, as for this pass transistor V_{GS} is too large, and this overstress condition is also getting worse for high V_{DD} operation [1].

To address these two issues, reduced coupling signal (RCS) circuit as shown in Fig. 2(b) is proposed here as write assist scheme. In this scheme, the voltage level of NBL_FIRE signal is reduced with the help of coupling voltage reduction block shown in this figure.

With the reduction in voltage level of NBL_FIRE signal, the negative bias (NVSS) signal level is reduced and hence negative bitline voltage level is reduced. In this work, 32 Kb SRAM with column mux (CM) = 8 i.e. an SRAM with physical rows (PR)=128 and physical columns (PC)=256 has been simulated with CCS-NBL, proposed RCS-NBL and state of the art SCS-NBL [1] write assist schemes. In CM=8 configuration 8-columns of bitcells are muxed with single write driver and hence single write assist block as shown in Fig.3(a). Simulated waveforms are plotted in Fig. 3(b) and 3(c) for comparison of CCS-NBL with RCS-NBL scheme, and RCS-NBL with SCS-NBL schemes

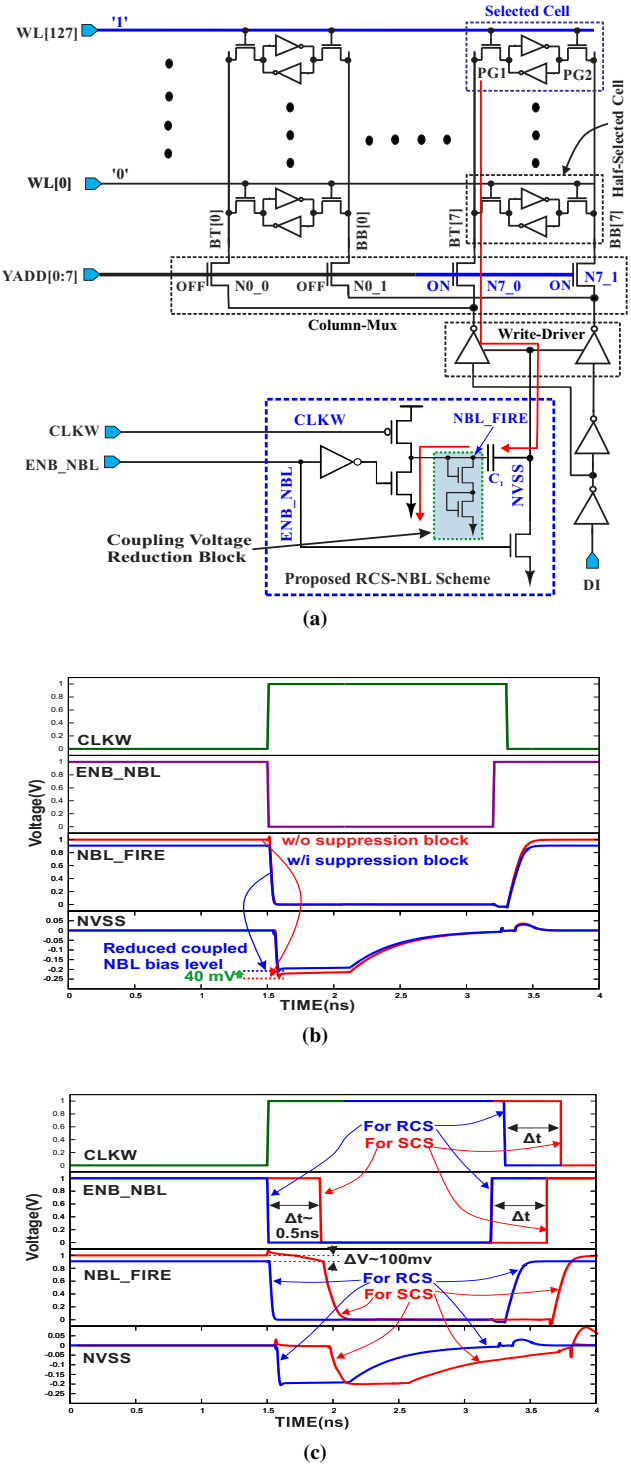


Fig. 3. (a) Proposed RCS-NBL write assist scheme (b) Simulation waveforms of CCS-NBL and RCS-NBL write assist schemes (c) Simulation waveforms of RCS-NBL and SCS-NBL write assist schemes.

respectively. Figure 3(b) and 3(c) demonstrate that the negative voltage level of NVSS is reduced by 40 mV with the help of RCS-NBL scheme as well as SCS-NBL scheme, and which has resulted in reduction of negative bitline voltage by same amount, this reduction will be more significant for higher V_{DD} operation. Thus RCS-NBL and SCS-NBL schemes ad-

dress both the issues mentioned above. However, as shown in Fig. 3(c) proposed RCS-NBL scheme also improves the performance of write operation of the bitcell as compared to SCS-NBL scheme, because in this scheme the generation of NVSS signal can be triggered at the same time when CLKW signal rises from '0' to '1' while in the case of SCS-NBL scheme generation of NVSS signal will be initiated after Δt time to get same assist level as in the case of RCS-NBL scheme. With 6σ process variation, simulation results shown in Fig. 4 demonstrate the improvement in SRAM write V_{MIN} with NBL techniques. In this figure, blue plot shows the required bitline voltage to write the bitcell, red, green and black plots represent coupled NBL voltage levels with CCS-NBL, proposed RCS-NBL and SCS-NBL techniques, respectively. Points A and B represent SRAM write V_{MIN} without and with write assist techniques respectively. It can be observed from this figure that the proposed RCS-NBL as well as the SCS-NBL write assist technique demonstrate improvement in SRAM write V_{MIN} by 295 mV.

4. Proposed Low Power Disturbance Noise Reduction (LP-DNR) Scheme

Read assist scheme WLUD improves the stability of half-selected bitcells but degrades both the read and write performances of selected bitcell [4]. Further WLUD scheme also shows rise in access time of bitcell with reducing V_{MIN}, then to improve the V_{MIN}, disturbance noise reduction (DNR) scheme was proposed as read assist scheme [2]. In this scheme, both the bitlines are lowered simultaneously, before the WL is activated to reduce the level of noise injection to the bitcell nodes, by discharging through clamping and discharge blocks. With lowering the bitlines voltage level at WL enabled time ADM increases to a certain level and thus the bitlines voltage level at which ADM is getting its maximum value, is defined as bitline safe-voltage level (V_{SAFE}).

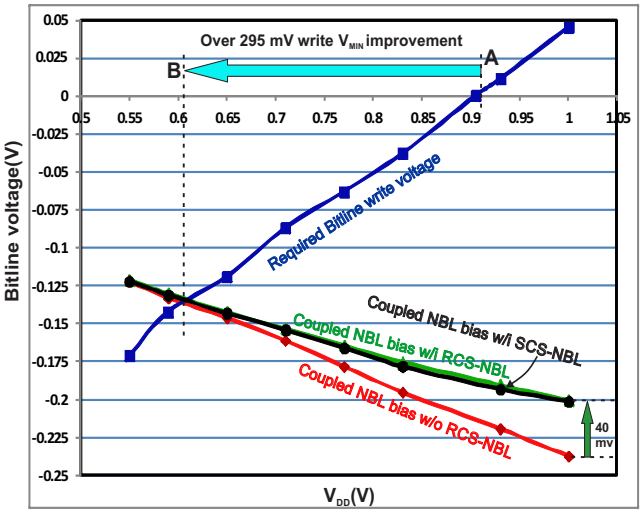


Fig. 4. Simulated write V_{MIN} for the NBL schemes.

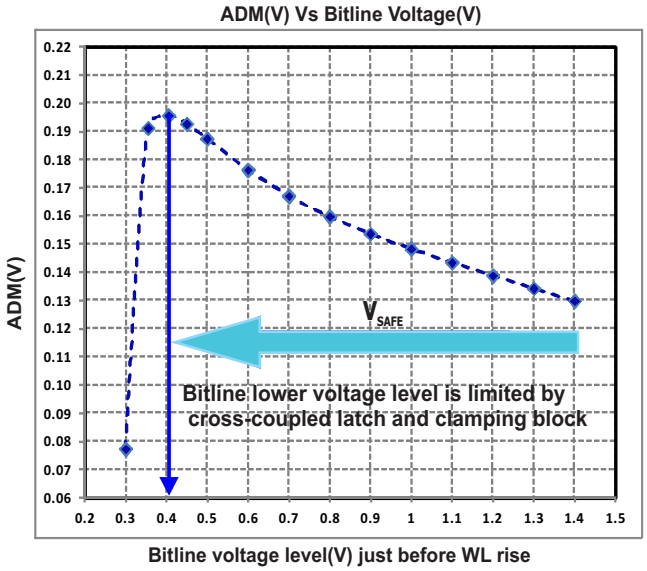


Fig. 5. Simulation result of ADM(V) versus bitline voltage level (V) for 6σ process variation.

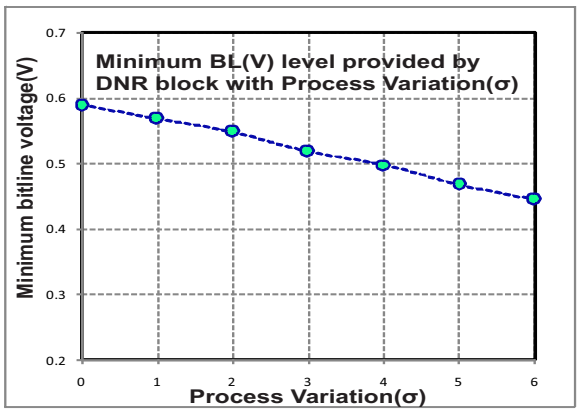


Fig. 6. Simulated minimum bitline voltage(V) at WL rise time with process variation(σ).

However, ADM degrades drastically as bitline voltage level goes below V_{SAFE} [2]. Figure 5 shows the plot of simulated results of ADM versus bitline voltage level at WL enabled time with 6σ process variation for the bitcell being used in this work and these results also endorse the same trend of steep degradation of ADM with bitline voltage level below V_{SAFE} . Thus to ensure enough data stability of the selected bitcells, proposed circuit must provide bitline voltage level at WL enable timing, more than or equal to V_{SAFE} but not below it. Hence here for 6σ process variation cross-coupled latch, clamping and discharge circuits have been designed to keep bitline lowest voltage level to V_{SAFE}. Figure 6 shows the simulated results of biltline voltage level provided by DNR block with process variation for V_{DD} = 1.0 V. These results demonstrate that DNR block being used in this work is providing bitline voltage level which is more than or equal to V_{SAFE} as indicated in Fig. 5. In DNR scheme, after the lowering of bitlines, as WL is activated bitcell read current (I_{Read}) from bitline to cell node storing '0' , in addition to bitline discharge current pulls down the corresponding bitline low enough to put ON one of the two PMOSs of cross-coupled

latch for which this bitline is acting as its gate. Thus as per the action of cross-coupled latch, this bitline goes down to '0' and other one goes to (V_{SAFE}+ΔV). PMOS which is ON keeps one of the two bitlines at (V_{SAFE}+ΔV) for the period WL enabled time to the time at which the bitline is pre-charged to V_{DD} again. For this period, pass transistor of the bitcell connected to the same bitline supplies current to it since this pass transistor is working very close to the subthreshold region. Thus, during this time period, a sum of PMOS ON current and pass transistor subtheshold current, I_{LOSS}, is drawn from supply V_{DD} and pushed to discharge block through the pair of clamping PMOS devices connected to the bitline settled at (V_{SAFE}+ΔV).

To save this loss of power contributed by I_{LOSS}, DNR circuit [2] has been modified and resulting circuit shown in Fig. 7(a) is proposed here as a new low power disturbance noise reduction (LP-DNR) read assist scheme. Fig.7(b) shows the timing diagram of proposed LP-DNR circuit for an access operation of the bitcell. As shown in this figure after WL is enabled, I_{Read} in addition to discharge current pulls the bitline BT enough low to turned-on PMOS P10 of I_{LOSS} path shut-off circuit, subsequently shut-off signal is activated (shut-off='1') with LP_DNR='1'. Thus during SHUT_PCH window, active shut-off signal turns off P2 & P3 devices, which results in stop of the flow of I_{Loss} but in case of DNR scheme this flow continues throughout SHUT_PCH window. In proposed LP-DNR scheme, as the flow of I_{LOSS} is blocked by turning off P2 device, the bitline BB starts to charge towards V_{DD} while BT remains at 0V, finally bitlines, BB & BT are synchronized with cell data, hence neither '1' noise nor '0' noise can inject to the cell which results in highest stability of the bitcell. Also, with this synchronization of bitlines with cell data the active current drawn from power supply V_{DD} is diminished.

5. Impact of Process Variability

In modern technologies intrinsic device variability of scaled devices dominates the traditional (worst-case) overall process spread that is generally used to determine the design window for the digital design community [17]. Transistor threshold voltage standard deviation σV_T can be used to represent the intrinsic device variability, which is expressed as follows [18]

$$\sigma V_T = 3.19 \times 10^{-8} \frac{t_{ox}.N_A^{0.401}}{\sqrt{L_{eff} W_{eff}}} \quad [V]. \qquad (1)$$

To simulate various SRAM parameters, with the impact of process variation, σV_T for all the concerned devices have been obtained using (1).

The simulation results for 6.5σ weak bitcell, shown in Fig. 8 demostrate the need of LP-DNR circuit to combat the access disturbance of the cell. For SRAM read operation bitlines are pre-charged to V_{DD} before the access of the cell, and access of the cell is obtained by turning ON pass transistors

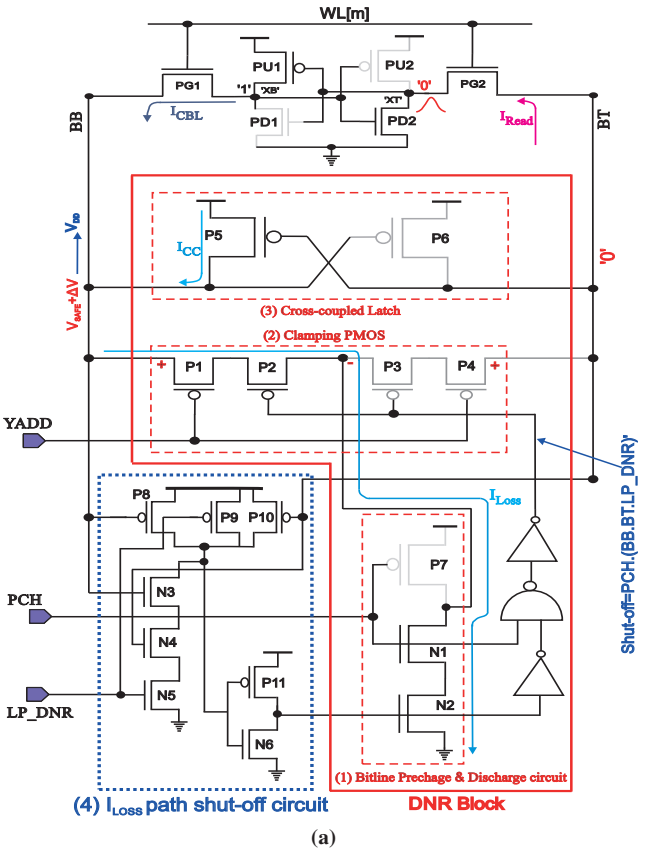


Fig. 7. (a) Proposed LP-DNR circuit (b) Timing diagram of the proposed LP-DNR read assist scheme.

(PG1,PG2) of the cell by enabling WL. Figure 8(a) shows the simulated waveforms for read operation, as the bitcell is accessed, noise from BT will be injected to the cell storage node XT storing '0' data before this access of the cell, thus XT node voltage rises to the voltage level which is sufficient to flip the cell, which results in functional failure. Further, the required voltage level at XT to flip the cell is also degrading as the cell gets weaker due to process variation. Figure 8(b) shows that the bitlines are lowered by LP-DNR circuit before the access of the cell hence the level of noise injection from BT to bitcell node XT storing '0' data before the access of the cell, is reduced which results in successful read operation of the cell.

Simulation results shown in Fig. 9, demonstrate the improvement in read V_{MIN} with the help of LP-DNR and DNR schemes respectively. In this figure, green curve shows the

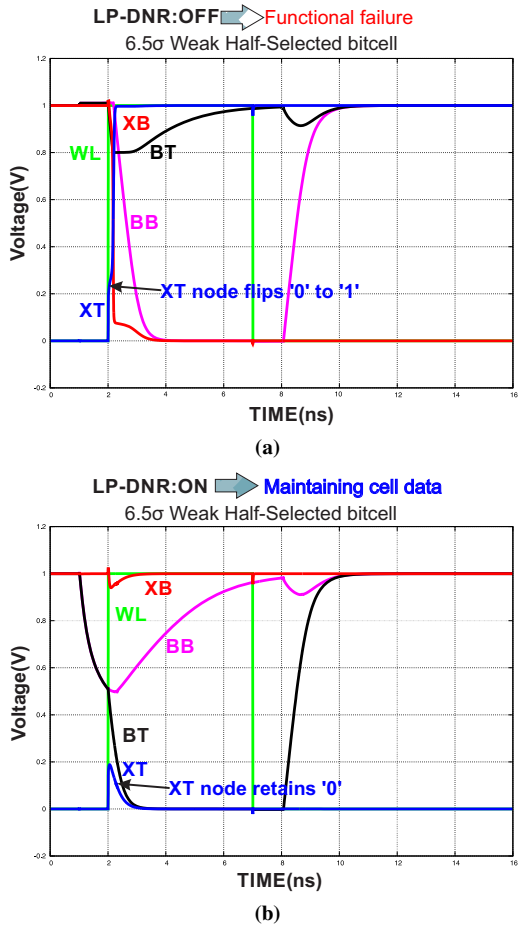


Fig. 8. LP-DNR effect on disturbance failure for weak bitcell (a) Simulated waveform without LP-DNR (b) Simulated waveform with LP-DNR.

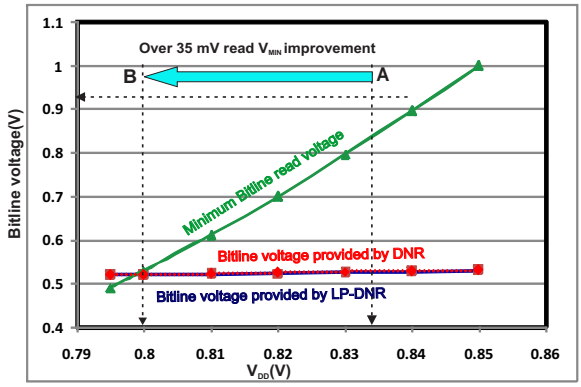


Fig. 9. Simulated read V_{MIN} for LP-DNR and DNR schemes.

minimum bitline voltage for non-destructive read operation of the cell, blue and red curves represent the bitline voltage level provided by LP-DNR and DNR schemes respectively. Here points A and B are representing SRAM read V_{MIN} without and with read assist techniques, respectively. It can be observed from these results that with the help of both the proposed as well as the DNR scheme, SRAM read V_{MIN} has improved by 35 mV.

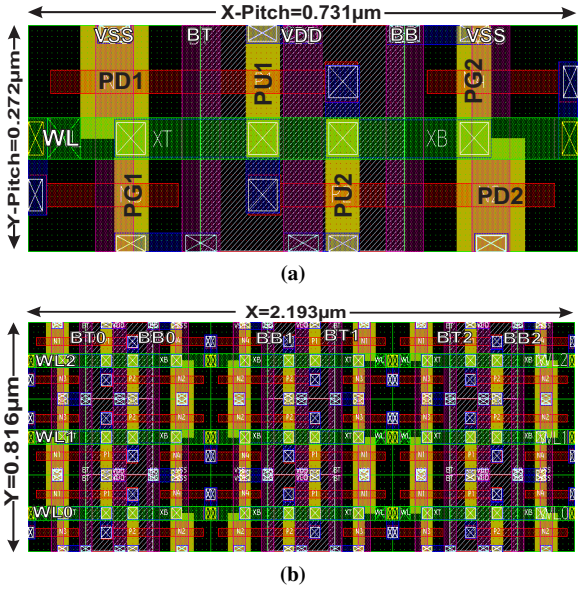


Fig. 10. Layout of 6T SRAM bitcell (a). Layout of 3×3 miniarray for 6T SRAM cell (b).

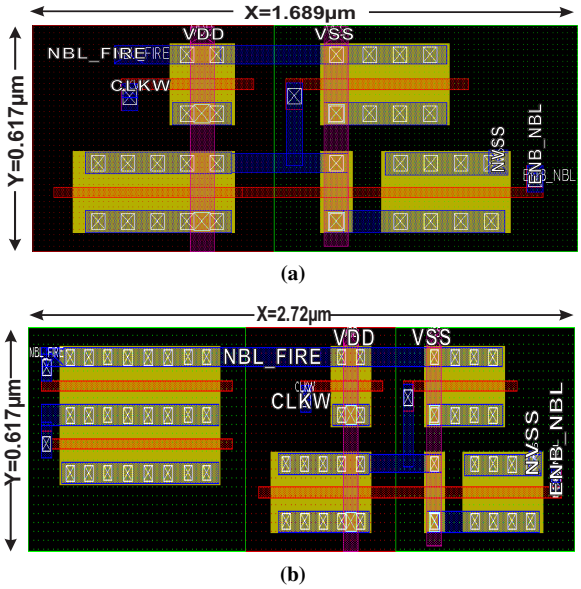


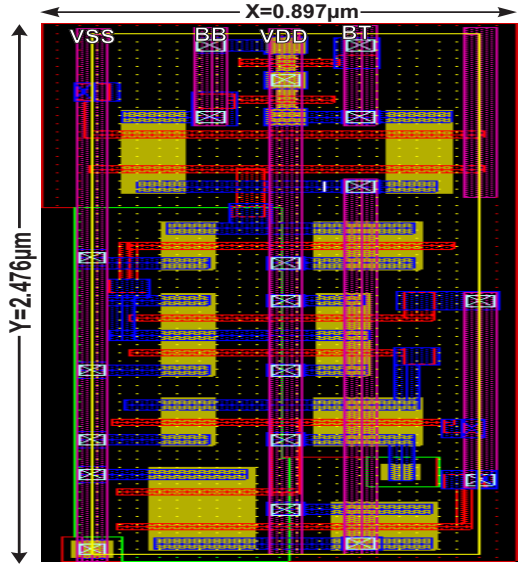
Fig. 11. Layout of Capacitive coupling signal (CCS) circuit (a) and proposed Reduced coupling signal (RCS) circuit (b).

6. Implementation and Simulation Results

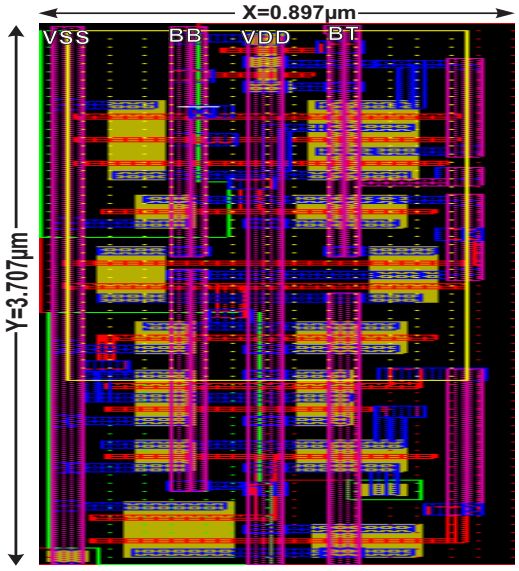
In this paper, all the layouts have been carried out using Synopsys Custom Designer Layout Editor (CDLE) and verified for DRC and LVS checks using IC Validator for 28-nm CMOS technology node while the RC parasitic extraction has been done using Synopsys Tool STAR-RC for the same technology node. Layouts of 6T SRAM bitcell as well as 3×3 miniarray are shown in Fig. 10(a) and (b).

Parasitics of centred 6T-SRAM bitcell of miniarray have been deduced from the extracted netlist of miniarray. Fig-

ures 11(a) and (b) show the layouts of capacitive coupling signal (CCS) circuit and proposed reduced coupling signal (RCS) circuit respectively. Layouts of DNR and LP-DNR circuits are as shown in Fig. 12(a) and (b). In this work, the simulation setup for 32 Kb SRAM with CM=8 , is made using center decode architecture as shown in Fig. 13. To get the loading netlist for this SRAM instance each bitcell in array is replaced by its extracted netlist deduced from miniarray as discussed above. To observe the impact of proposed assist schemes with respect to no assist circuits and with assist circuits, extracted netlists for existing assist circuits, CCS and DNR have been used. For the proposed assist circuits RCS-NBL and LP-DNR, extracted netlists of the respective blocks have been used.



(a)



(b)

Fig. 12. Layout of DNR circuit (a). Proposed LP-DNR circuit (b).

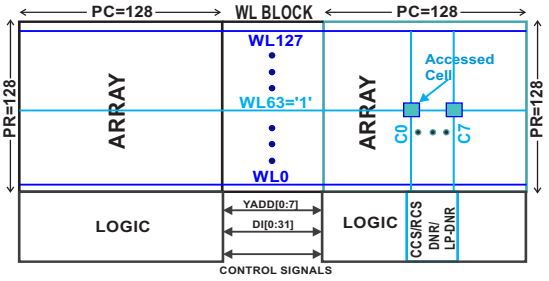


Fig. 13. Architecture used for simulation 32 Kb SRAM.

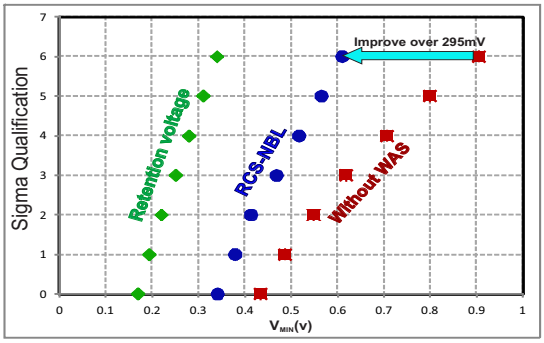


Fig. 14. Simulated SRAM V_{MIN} with process variation(σ).

Figure 14 depicts the sigma-qualification of SRAM. In this figure, red square, blue dot and green rhombus represent SRAM V_{MIN} to qualify for a particular level of process variation(σ) for no write assist scheme, with proposed write assist scheme (RCS-NBL) and for retention mode, respectively.

Power numbers along with V_{MIN} of above mentioned SRAM macro, collected with the help of simulations, for respective write assist and read assist schemes as well as without assist schemes are shown in Tab. 1 (a) and (b) respectively.

SCHEME	V_{MIN}(V)	POWER(µW)	
		DYNAMIC	STATIC
W/O WRITE ASSIST	0.905	975	22
CCS-NBL	0.61	75.2	9.82
RCS-NBL	0.61	81.3	11.3
State of the art (SCS-NBL)	0.61	76.2	9.82

(a)

SCHEME	V_{MIN}(V)	POWER(µW)	
		DYNAMIC	STATIC
W/O READ ASSIST	0.834	311	26.31
LP-DNR	0.799	286	23.20
State of the art (DNR)	0.799	334	23.21

(b)

Tab. 1. Dynamic and static power-numbers along with V_{MIN} for (a) write assist schemes (b) read assist schemes.

SCHEME	V_{MIN}[V]		DYNAMIC POWER RATIO	STATIC POWER RATIO
	W/O ASSIST	W/I ASSIST		
RCS-NBL	0.905	0.61	91.7% ↓	48.9% ↓
LP-DNR	0.834	0.799	8.1% ↓	11.7% ↓

Tab. 2. Static power-improvement with assist circuits.

7. Conclusions

We have proposed new write and read assist circuits, RCS and LP-DNR respectively, to improve SRAM V_{MIN} for 28-nm bulk CMOS technology. Simulation results with 6σ process variation for 32 Kb SRAM CM=8 macro, demonstrate that SRAM write $V_{MIN}$is lowered to 0.61 V, which is an improvement of 295 mV with respect to without any write assist scheme.

SRAM read V_{MIN} has been lowered to 0.799 V, which is an improvement of 35 mV as compared to without any read assist scheme. Table 2 summarizes the improvements in the respective SRAM V_{MIN}, dynamic power and static power consumption for this SRAM macro with the help of corresponding assist techniques.

LP-DNR scheme also improves dynamic power consumption by 16.8 % as compared to DNR scheme, while in the case of RCS-NBL scheme dynamic power consumption degrades by 6.3 % as compared with SCS-NBL write assist scheme. Over stress on PG transistor of selected bitcell as well as the stability issue of half-selected bitcells in the existing CCS-NBL scheme especially at higher operating voltages has been addressed in the proposed RCS-NBL scheme at the cost of power degradation during the short duration of clock inactive window. Area overheads of these proposed RCS-NBL and LP-DNR assist techniques for this macro are less than 0.79 % and 3.70 % respectively.

References

[1] CHEN, Y.-H., CHAN, W.-M., WU, W.-C., et al. A 16 nm 128 Mb SRAM in high-k metal-gate FinFET technology with write-assist circuitry for low-vmin applications. *IEEE Journal of Solid-State Circuits*, 2015, vol. 50, no. 1, p. 170–177. DOI: 10.1109/JSSC.2014.2349977

[2] SONG, T., RIM, W., JUNG, J., et al. A 14 nm FinFET 128 Mb SRAM with v enhancement techniques for low-power applications. *IEEE Journal of Solid-State Circuits*, 2015, vol. 50, no. 1, p. 158–169. DOI: 10.1109/JSSC.2014.2362842

[3] KUMAR, S., TIKKIWAL, V., GUPTA, H. Read SNM free SRAM cell design in deep submicron technology. In *Proceedings of the International Conference on Signal Processing and Communication*. 2013, p. 375–380. DOI: 10.1109/ICSPCom.2013.6719816

[4] NII, K., YABUUCHI, M., TSUKAMOTO, Y., et al. A 45-nm bulk CMOS embedded SRAM with improved immunity against process and temperature variations. *IEEE Journal of Solid-State Circuits*, 2008, vol. 43, no. 1, p. 180–191. DOI: 10.1109/JSSC.2007.907998

[5] GROSSAR, E., STUCCHI, M., MAEX, K., et al. Read stability and write-ability analysis of SRAM cells for nanometer technologies. *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 11, p. 2577–2588. DOI: 10.1109/JSSC.2006.883344

[6] YAMAOKA, M., OSADA, K., ISHIBASHI, K. 0.4-V logic-library-friendly SRAM array using rectangular-diffusion cell and delta-boosted-array voltage scheme. *IEEE Journal of Solid-State Circuits*, 2004, vol. 39, no. 6, p. 934–940. DOI: 10.1109/JSSC.2004.827796

[7] ZHANG, K., BHATTACHARYA, U., CHEN, Z., et al. A 3-GHz 70-mb SRAM in 65-nm CMOS technology with integrated column-based dynamic power supply. *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 1, p. 146–151. DOI: 10.1109/JSSC.2005.859025

[8] CHANDRA, V., PIETRZYK, C., AITKEN, R. On the efficacy of write-assist techniques in low voltage nanoscale SRAMs. In *Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE)*. 2010, p. 345–350. DOI: 10.1109/DATE.2010.5457179

[9] TAKEDA, K., HAGIHARA, Y., AIMOTO, Y., et al. A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 1, p. 113–121. DOI: 10.1109/JSSC.2005.859030

[10] CHANG, L., FRIED, D. M., HERGENROTHER, J., et al. Stable SRAM cell design for the 32 nm node and beyond. In *Proceedings of the Digest of Technical Papers, Symposium on VLSI Technology*. 2005 , p. 128–129. DOI: 10.1109/.2005.1469239

[11] LIU, Z., KURSUN, V. Characterization of a novel nine-transistor SRAM cell. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2008, vol. 16, no. 4, p. 488–492. DOI: 10.1109/TVLSI.2007.915499

[12] SHIBATA, N., KIYA, H., KURITA, S., et al. A 0.5-V 25-MHz 1-mW 256-kb MTCMOS/SOI SRAM for solar-power-operated portable personal digital equipment - sure write operation by using step-down negatively overdriven bitline scheme. *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 3, p. 728–742. DOI: 10.1109/JSSC.2005.864124

[13] KUMAR, S., SAHA, K., GUPTA, H. Run time write detection in SRAM. In *Proceedings of the International Conference on Signal Processing and Communication*. 2015, p. 328–333. DOI: 10.1109/ICSPCom.2015.7150671

[14] NII, K., YABUUCHI, M., TSUKAMOTO, Y., et al. A 45-nm singleport and dual-port SRAM family with robust read/write stabilizing circuitry under DVFS environment. In *Proceedings of the IEEE Symposium on VLSI Circuits*. 2008, p. 212–213. DOI: 10.1109/VLSIC.2008.4586011

[15] TAKEDA, K., SAITO, T., ASAYAMA, S., et al. Multi-step word-line control technology in hierarchical cell architecture for scaled-down high-density SRAMs. In *Proceedings of the IEEE Symposium on VLSI Circuits*. 2010, p. 101–102. DOI: 10.1109/VLSIC.2010.5560336

[16] ZIMMER, B., TOH, S. O., VO, H., et al. SRAM assist techniques for operation in a wide voltage range in 28-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2012, vol. 59, no. 12, p. 853–857. DOI: 10.1109/TCSII.2012.2231015

[17] TUINHOUT, H. Impact of parametric fluctuations on performance and yield of deepsubmicron technologies. In *Proceedings of the 32nd European Solid-State Device Research Conference*. 2002, p. 95–102. DOI: 10.1109/ESSDERC.2002.194879

[18] ASENOV, A., SAINI, S. Suppression of random dopant-induced threshold voltage fluctuations in sub-0.1- μm MOSFET's with epitaxial and δ-doped channels. *IEEE Transactions on Electron Devices*, 1999, vol. 46, no. 8, p. 1718–1724. DOI: 10.1109/16.777162

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