Guidelines on the Switch Transistors Sizing Using the Symbolic Description for the Cross-Coupled Charge Pump

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Abstract. *This paper presents a symbolic description of the design process of the switch transistors for the cross-coupled charge pump applications. Discrete-time analog circuits are usually designed by the numerical algorithms in the professional simulator software which can be an extremely time-consuming process in contrast to described analytical procedure. The significant part of the pumping losses is caused by the reverse current through the switch transistors due to the continuous-time voltage change on the main capacitors. The design process is based on the analytical expression of the time response characteristics of the pump stage as an analog system with using BSIM model equations. The main benefit of the article is the analytical transistors sizing formula so that the maximum voltage gain is achieved. The diode transistor is dimensioned for the pump requirements, as the maximal pump output ripple voltage, current, etc. The characteristics of the proposed circuit have been verified by simulation in ELDO Spice. Results are valid for N-stage charge pump and also applicable for other model equations as PSP, EKV.*

Keywords

Time response characteristics, reverse current, cross-coupled charge pump, BSIM model, high-voltage

1. Introduction

Charge pumps are switched-capacitor circuits that transport charge between main capacitors to create a higher output voltage. They are used to supply low-power circuits that require relatively high input voltage, for example, EEPROM memories.

The advanced architectures of the modern integrated two–phase charge pump are based on the elimination of the threshold voltage of the active components (Dickson charge pump [1]), that decreases all node voltages. The static charge pumps [2–4] realize the charge transport through the switch transistors, which are controlled by the output voltage from the next stage as is shown in Fig. 1. When the logic levels of the two-phase clock signal are $\phi = 0$ (low) and $\bar{\phi} = V_{\mathrm{DD}}$ (high) and assuming the correct function of the charge pump,

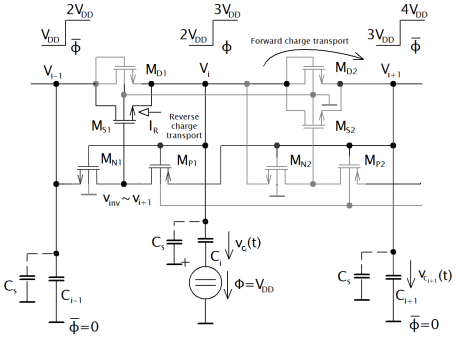

Fig. 1. Reverse current through the switch transistor in the cross-coupled charge pump.

then switch transistor M_{S1} is fully ON, node voltages V_{i-1} and V_{i+1} are pumped up to $2V_{\mathrm{DD}}$ and $3V_{\mathrm{DD}}$ respectively, and main capacitor connected to node i is charged to $2V_{\mathrm{DD}}$. The voltage drop between two nodes is theoretically determined by the saturation voltage of the switch (MOSFET) at the end of the charge transport. Conversely, when $\phi = V_{\mathrm{DD}}$ and $\bar{\phi} = 0$, M_{S1} must be OFF [4], so that capacitor connected to node i can be pumped up to $2V_{\mathrm{DD}}$ and forward charge transport between nodes i and $i + 1$ can be realized. The problem of the reverse current occurs at the same time ($\phi = V_{\mathrm{DD}}$ and $\bar{\phi} = 0$) because the voltage difference $v_{\mathrm{inv}} - v_{i-1}$ may be higher than threshold voltage $V_{\mathrm{TH_{MS1}}}$. Now, the MOSFET electrodes Drain and Source are mutually exchanged and M_{S1} is not OFF in spite of the expectation.

The discharge–reverse current i_{R}, which flows through the switch is undesirable because it decreases the pump voltage gain. The reverse current of the diode transistor is practically zero. The cross–coupled charge pump contains the inverter that controls the switch at the time intervals defined by the clock signal. This topology allows achieving higher efficiency compared with the static charge pump. However, the problem of reverse current still exists [4], [5].

Simulation results show a strong dependence of the pump voltage gain on the strength of the switch transistor(s). Design of discrete-time analog circuits including charge pump circuits represent the fundamental problem, which relates to the solution of the part steps of the design algorithm. The following three key steps are necessary for a successful design: circuit model, simulation and evaluation of the

simulation results. Only transient analyses are allowable. It is a fundamental difference of approach compared to analog circuits [5]. The experimental part including simulation of real properties of the cross-coupled charge pump [5] and their comparison with other architectures (Dickson charge pump, a static charge pump) has been done [1–4], [6], [7]. However, a design process of the circuit has not been known yet. General description methods of discrete-time analog circuits have been published in many books and research papers [5], [8], [9]. Well-known description methods are insufficient because they do not consider the relevant properties (nonidealized structure), that are typical for the behavior of the charge pumps. Optimization is usually circuitous process due to many iterations to achieve of the required parameters (static, dynamic). The different access to solve this task will be offered in this article. The symbolic description of the design process of the cross-coupled charge pump stage as an analog block for high-voltage application will be discussed to find an analytical expression for width and length of the diode and switch transistors so that the voltage gain of the N-stage pump will be maximal. The pump elements (switch, diode, capacitors,..) usually have same parameters at all pump stages. Long channel MOSFET is provided due to high bias voltages (drain-source) in the circuit. Sizing of the switch transistor will be designed so that the reverse current will be suppressed. Sizing of the diode transistor is related to the optimization of pump parameters such as maximation of the load current, minimalization of the output ripple voltage.

The DC characteristics of the pump stage will be firstly found. Because the transistors are operating in strong inversion region, the simplified BSIM model [10] can be used for this purpose. The main part contains an analytical description of the time response characteristics, which are applied in the real circuit. The switch transistors ratio W_s/L_s is set, so that their equivalent resistance value is a compromise between the charge/forward and discharge/reverse current. The ratio is calculated for the worst case of bias voltages because this resistance is nonlinear. The equivalent diode resistance is determined by the change of the pump output voltage. The derived formulas are verified by simulation in ELDO Spice. The effort is to find mentioned solution without using the numerical optimization procedure. The created model including the dominant real properties points to an alternative way to N-stages charge pump draft (static, dynamic parameters). The strong inversion operating region of the MOSFET is expected, in which the behavior of the MOSFET models is correct [11] compared with the real measured curves (BSIM, EKV, PSP, etc.) in the specified technology process.

2. The Static Model of the Pump Stage

One stage of the cross-coupled charge pump is shown in Fig. 2. The drain current of the each MOSFETs is controlled by the input voltage V_{in}. Adjustable DC source voltage is used for analysis instead of the main capacitor in real circuits. All other DC voltages in the diagram are referenced to the ground.

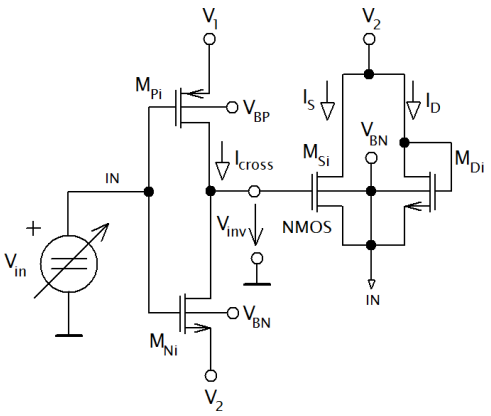

Fig. 2. Diagram of the cross-coupled charge pump stage.

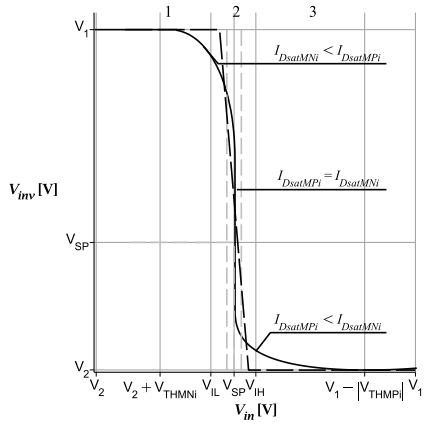

Fig. 3. The voltage transfer characteristics of the CMOS inverter for long channel MOSFET and its linearization.

It is supposed that all transistors are operating in strong inversion region. Hence, the power supply range of the inverter must be adequately high to turn on both of the transistors M_{Ni} and M_{Pi} in the interval $V_{in} \in \langle V_{IL}, V_{IH} \rangle$, see Fig. 3. Pump voltage gain of two stages labeled $G_v = V_1 - V_2$, must be greater than the sum of the threshold voltages of these transistors, labeled $V_{TH_{MNi}}$, $V_{TH_{MPi}}$. The switch transistor must be ON, when the output inverter is at a high logic level, i.e. $v_{inv} = V_1$,

$$V_{TH_{Msi}} < G_v > V_{TH_{MNi}} + |V_{TH_{MPi}}| . \tag{1}$$

The output voltage of the inverter $V_{inv} = f(V_{in})$ is setting the drain current of the switch transistor M_{Si}, labeled I_S. The CMOS inverter voltage transfer characteristic [12–14] is derived based on the fact that the drain current of both MOSFETs must be equal for each of the operating regions.

The complex expression of the voltage transfer characteristics is not necessary for the practical results. Considering the electrical field in structure is much less than critical electrical field [10], then "long channel" can be defined as

$$L_{eff} \gg V_{max} \frac{\mu_{eff}}{2v_{sat}}, \tag{2}$$

where L_{eff} is the effective channel length [10], [12], V_{max} is the maximal bias voltage (drain-source, gate-source), μ_{eff} is effective mobility and v_{sat} is the saturation velocity [10].

Then, the transfer part of the characteristics is well linearized, as it is shown in Fig. 3. Input voltages between the limit values V_{IL} and V_{IH} do not define the valid output logic level [12]. Inverter cross current I_{cross} is the maximal in the switching point when $V_{\mathrm{IN}} = V_{\mathrm{inv}}$ [12]. Analytical equation of V_{SP} is derived in [5]. Now, an analytical estimation of the voltage transfer characteristics has the following form:

$$V_{\mathrm{out}}(V_{\mathrm{in}}) \approx \begin{cases} V_1, & V_{\mathrm{in}} \leq V_{\mathrm{IL}}, \\ \frac{V_1 - V_2}{V_{\mathrm{IL}} - V_{\mathrm{IH}}}(V_{\mathrm{IN}} - V_{\mathrm{IL}}) + V_1, & V_{\mathrm{IH}} > V_{\mathrm{in}} > V_{\mathrm{IL}}, \\ V_2, & V_{\mathrm{in}} \geq V_{\mathrm{IH}}. \end{cases} \tag{3}$$

The slope of the transition part is determined by the Early voltage of MOSFETs, V_{ADIBL}, which is proportional to the voltage V_{GS} and relationship only contains the model parameters of PDIBLC2 and PDIBLCB [10]. So that, difference $V_{\mathrm{IH}} - V_{\mathrm{IL}}$ is very small, $V_{\mathrm{IL}} \to V_{\mathrm{SP}}$, $V_{\mathrm{IH}} \to V_{\mathrm{SP}}$ and the wide of the transition part is negligibly small (zero in the ideal case).

The voltage on the capacitor is changing continuously from 0 to the supply voltage V_2 in the passive time interval and the voltage at the terminal "IN" may be theoretically doubled in the active interval of the clock signal, i.e. $V_{\mathrm{IN}} = 2V_2$. Thus, the drain current I_{S} through the switch transistor M_{Si} (and its orientation) will be analyzed in the interval of the input voltage $V_{\mathrm{in}} \in \langle 0, V_1 \rangle$ (the D,S pins of the switch transistor are not distinguished in the scheme). The direction of the forward–"charging" current (that is required) matches the orientation in the scheme. The control voltages configuration for the setting both the forward ($I_{\mathrm{S_F}}$) and reverse current of the drain ($I_{\mathrm{S_R}}$) of the M_{Si} transistor are shown in Tab 1.

Parameter	Value	
I_{S}	> 0	≤ 0
V_{in}	$V_{\mathrm{in}} \in \langle 0, V_2 \rangle$	$V_{\mathrm{in}} \in \langle V_2, V_1 \rangle$
$V_{\mathrm{DS_{MSi}}}$	$V_2 - V_{\mathrm{in}}$	$V_{\mathrm{in}} - V_2$
$V_{\mathrm{GS_{MSi}}}$	$V_{\mathrm{inv}} - V_{\mathrm{in}} = V_1 - V_{\mathrm{in}}$	$V_{\mathrm{inv}}(V_{\mathrm{in}}) - V_2$
$V_{\mathrm{SB_{MSi}}}$	$V_{\mathrm{in}} - V_{\mathrm{BN}}$	$V_2 - V_{\mathrm{BN}}$

Tab. 1. M_{Si} transistor control voltages configuration for the setting of I_{S}.

Respecting the condition (1), transistor M_{Si} is always ON in the interval $V_{\mathrm{in}} \in \langle 0, V_2 \rangle$. The bulk both of the M_{Ni} and M_{Si} transistors is connected to the same bias voltage V_{BN} (usually to the ground) and $V_{\mathrm{SB_{MSi}}} \leq V_{\mathrm{SB_{MNi}}}$, then $V_{\mathrm{TH_{MSi}}}(V_{\mathrm{SB}}) \leq V_{\mathrm{TH_{MNi}}}(V_{\mathrm{SB}})$ in the same technology process. Moreover, this transistor is operating in the triode region, as it is shown bellow. In this case, the condition $V_{\mathrm{DS}} < V_{\mathrm{DS_{sat}}}$ is valid, where the saturation voltage is calculated from [10], [15]

$$V_{\mathrm{DS_{sat}}} = \frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{A_{\mathrm{bulk}}(V_{\mathrm{GS}}, V_{\mathrm{SB}})}. \tag{4}$$

Substituting the specific values from Tab. 1 into the $V_{\mathrm{DS_{sat}}}$ expression, following inequality is obtained:

$$V_2 < \frac{V_1 - V_{\mathrm{in}} - V_{\mathrm{TH_{MSi}}}(V_{\mathrm{in}}, V_{\mathrm{BN}})}{A_{\mathrm{bulk_{Msi}}}(V_1, V_{\mathrm{in}}, V_{\mathrm{BN}})} + V_{\mathrm{in}}. \tag{5}$$

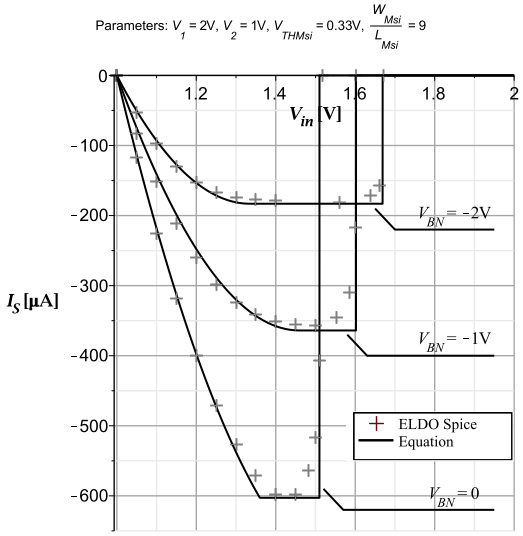

Fig. 4. Reverse current of the switch transistor vs. input voltage.

Expression on the right hand sight of (5) must also satisfy the condition (1). Considering the worst case of the threshold voltage, $V_{\mathrm{TH_{MSi}}} = V_{\mathrm{TH_{MNi}}}$, then

$$|V_{\mathrm{TH_{MPi}}}| + V_{\mathrm{in}} > \underbrace{\left(1 - \frac{1}{A_{\mathrm{bulk_{Msi}}}}\right)}_{\leq 0}(V_1 - V_{\mathrm{TH_{Msi}}} - V_{\mathrm{in}}). \tag{6}$$

Saturation voltage $V_{\mathrm{DS_{sat}}}$ can be approximated by the function $V_{\mathrm{GS}} - V_{\mathrm{TH}}$ near the point $V_{\mathrm{GS}} = V_{\mathrm{TH}}$ (long channel MOSFET is provided). However, real saturation voltage is greater than function expressed in (4) for higher voltage V_{GS}, $V_{\mathrm{DS_{sat}}} > V_{\mathrm{GS}} - V_{\mathrm{TH}}$, i.e. $A_{\mathrm{bulk}} < 1$, for $V_{\mathrm{GS}} \gg V_{\mathrm{TH}}$. Subsequently, the inequality (6) is always true.

The drain current direction is changed, and it is controlled by the constant gate-source voltage $V_1 - V_2$, while $V_2 < V_{\mathrm{in}} \leq V_{\mathrm{IL}}$. The gate-source voltage decreasing quickly in the interval $\langle V_{\mathrm{IL}}, V_{\mathrm{IH}} \rangle$, while a change of the drain-source voltage is negligible. Hence, the drain current achieves the maximal value at point V_{IL} and transistor is abruptly switched off after exceeding the switching point. Neglecting the transition part of the inverter transfer characteristic, drain current can be considered the constant in the interval $V_{\mathrm{in}} \in \langle V_{\mathrm{IL}}, V_{\mathrm{SP}} \rangle$. Total current I_{S} is given by the following formula:

$$I_{\mathrm{S}}(V_{\mathrm{in}}) \approx \begin{cases} I_{\mathrm{DS0_F}}, & V_{\mathrm{in}} \in \langle 0, V_2 \rangle, \\ I_{\mathrm{S_R}}, & V_{\mathrm{in}} \in (V_2, V_{\mathrm{SP}} \rangle, \\ 0, & V_{\mathrm{in}} \in (V_{\mathrm{SP}}, V_1 \rangle. \end{cases} \tag{7}$$

Current $I_{\mathrm{S_R}}$ is calculated on the basis of the two following cases:

- if $V_{\mathrm{IL}} > V_2 + V_{\mathrm{DSsat_{MSi}}}$, then

$$I_{\mathrm{S_R}}(V_{\mathrm{in}}) \approx \begin{cases} I_{\mathrm{DS0_R}}, & V_{\mathrm{in}} \in (V_2, V_2 + V_{\mathrm{DS_{sat}}} \rangle \\ I_{\mathrm{D_{sat0R}}}, & V_{\mathrm{in}} \in (V_2 + V_{\mathrm{DS_{sat}}}, V_{\mathrm{SP}} \rangle, \end{cases} \tag{8}$$

- if $V_{\mathrm{IL}} \leq V_2 + V_{\mathrm{DSsat_{MSi}}}$, then

$$I_{\mathrm{S_R}}(V_{\mathrm{in}}) \approx \begin{cases} I_{\mathrm{DS0_R}}, & V_{\mathrm{in}} \in (V_2, V_{\mathrm{IL}} \rangle \\ I_{\mathrm{DS0_R}}|_{V_{\mathrm{GS}} = V_1 - V_2, V_{\mathrm{DS}} = V_{\mathrm{IL}} - V_2}, & V_{\mathrm{in}} \in (V_{\mathrm{IL}}, V_{\mathrm{SP}} \rangle, \end{cases} \tag{9}$$

where I_{DS0} is the drain current in triode region and $I_{D_{sat0}}$ is the drain current in saturation region at $V_{DS} = V_{DS_{sat}}$. The reverse current waveform for the both cases is shown in Fig. 4. The source-bulk voltage is the parameter.

The drain current of the M_{Di} transistor is zero in the reverse configuration due to shorted gate and source electrodes,

$$I_D(V_{in}) = \begin{cases} I_{Dsat0}, & V_{in} \in \langle 0, V_2 - V_{TH_{MDi}}) \\ 0, & \text{otherwise.} \end{cases} \quad (10)$$

3. Time Response Characteristics

Step response is a typical characteristic situation in the switched-capacitor circuits. Step response characteristics of the circuits are shown in Fig. 6 and 8. The time-varying voltage on the main capacitor to the clock signal will be found for both the forward and reverse configuration to determining pumping losses. The extreme values of the bias voltage have been chosen for the following optimization process. The time domain method must be used for the calculation due to the nonlinearity behavior of this system. It is also necessary to define the next conditions for the analysis process:

- parasitic capacitances are negligibly small compared with the main pumping capacitors, $C_s \ll C_i$.
- rise time and fall time delay of the clock signal and propagation delays of the inverter are very short compared to the charge/discharge time of the main capacitors.
- leakage currents of all the components are neglected.
- settling time of the switches is zero.

The main capacitor is charged, when the gate of the switch transistor is connected to high output voltage level of the inverter V_{inv} = "H" = V_1, the drain is connected to the input stage voltage V_2 and the main capacitor is connected to ground. This situation is shown in Fig. 5.

When the switches S_1, S_2 and S_3 are ON at $t = 0$, the current flowing through the capacitors i_{c_F} is supplied both of the transistor until the capacitor voltage does not exceed the value V_{0_F} at time t_{0_F}, see Fig. 5. Total current i_{c_F} is given by

$$i_{c_F}(t) = \begin{cases} i_s(t) + i_d(t), & \text{for } 0 < t \le t_{0_F}, \\ i_s(t), & \text{for } t > t_{0_F}, \\ 0, & \text{otherwise.} \end{cases} \quad (11)$$

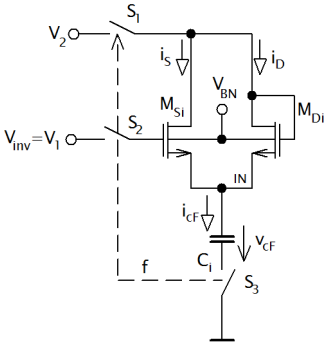

Fig. 5. Configuration for the charge of the main capacitor.

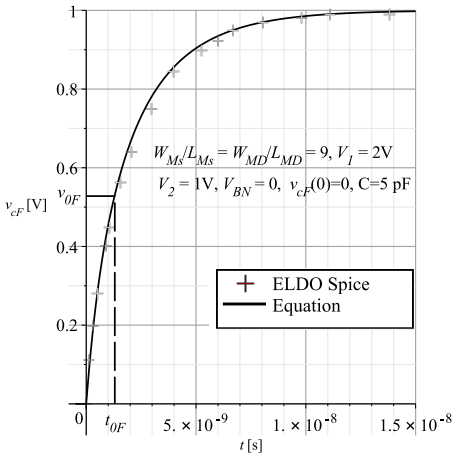

Fig. 6. Time response characteristics of the circuit from Fig. 5.

The voltage on the capacitor is equal to V_2 in steady state and the particular value of the voltage V_{0_F} can be derived from

$$V_{0_F} = V_2 - V_{TH_{MDi}}(v_{SB}) \quad (12)$$

where source-bias voltage is equal to v_{c_F} ($V_{BN} = 0$). Dependence of the threshold voltage on the V_{SB} voltage (body effect [10], [12], [13], [15]) is given by

$$V_{TH} = V_{TH0} + K_{1ox}\sqrt{\phi_s - V_{BS}} - K_1\sqrt{\phi_s} - K_{2ox}V_{BS} \quad (13)$$

where V_{TH0} is threshold voltage at zero bias voltages, ϕ_s is the surface potential and K_1, K_2 are body effect coefficients (model parameters). Combining (12) and (13), the instantaneous value of the voltage in which the transistor M_{Di} will be OFF, is calculated from

$$V_{0_F} = \frac{V_2 + K_1 - V_{TH0_{MDi}}}{K_{2ox} + 1} + \frac{1}{2}\frac{K_{1ox}\left(K_{1ox} - \sqrt{\gamma}\right)}{(K_{2ox} + 1)^2} \quad (14)$$

where

$$\gamma = 4\phi_s (K_{2ox} + 1)^2 + 4 (K_{2ox} + 1)\psi,$$
$$\psi = \left(K_1\sqrt{\phi_s} + V_2 - V_{TH0_{MDi}} + K_{1ox}^2\right).$$

Substituting the voltage v_{cF} in the static model for V_{in} and using equations for the drain current [10], [12], [13], [15], time response characteristic is found by the solving of following differential equation

$$\int \frac{C}{i_{c_F}} dv_c = t + IC \quad (15)$$

with the initial condition $v_c(t_0) = v_{c_0}$ for each of the intervals, as it is shown in (11). The drain current equation is the composite function (NF) in the form

$$i_c = f\left[v_{ds}(t), v_{gs}(t), v_{TH}(v_c(t)), A_{bulk}(v_c(t)), \mu_{eff}(v_c(t))\right],$$

consequently, the analytical solution would be unreasonably complicated for practical design. Thus, the estimation is done providing the constant nested functions v_{TH}, A_{bulk} and μ_{eff}

according this criteria: When $t \leq t_{0_F}$, the voltage v_{c_F} change in time is approximately same as at the beginning of the transient process. Contrariwise, when $t > t_{0_F}$ and $i_D = 0$ the characteristic curve is approximated by the nested function values which would acquire in the steady state.

The same principle is also used for the reverse configuration, as it is shown in Fig. 7. Bias voltages are listed in Tab. 2.

Condition		Index of NF.		$\mathbf{V_{in}}$[V]	
		M_{D_i}	M_{S_i}	M_{D_i}	M_{S_i}
$i_s > 0$	$t < t_{0_F}$	D0	S0	$v_{c_F}(0_+)$	$v_{c_F}(0_+)$
	$t \geq t_{0_F}$	X	S	X	V_2
$i_s < 0$	$t < t_{0_R}$	X	SR	X	$v_{c_R}(0_+)$
	$t \geq t_{0_R}$	X	S	X	V_2

Tab. 2. Bias voltages of the nested functions (NF) V_{TH}, A_{bulk} and u_{eff}.

Therefore, solving of (15) can be only found by integrating the voltage square $[v_{gs}(t) - V_{TH}]^2$, eventually $v_{ds}(t)$ and $v_{ds}^2(t)$ for triode region. The time-varying voltage v_{C_F} for the forward configuration is given by

$$v_{C_F}(t) = \begin{cases} V_{C_F}(0), & \text{for } t \leq 0 \\ \dfrac{\sqrt{C_1C_2}\cdot\tan\left[\frac{(t+\mathrm{IC_{F1}})\sqrt{C_1C_2}c_{oxe}}{2L\cdot C A_{bulk_{D0}}}\right]-C_4}{\mu_{eff_{D0}}W_{M_S}+C_1\left(A_{bulk_{S0}}-2\right)}, & \text{for } 0 < t < t_{0_F} \\ \dfrac{C_6 e^{\frac{t+\mathrm{IC_{F2}}}{C_7}}-V_2}{e^{\frac{t+\mathrm{IC_{F2}}}{C_7}}(A_{bulk_S}-2)-1}, & \text{for } t \geq t_{0_F}, \end{cases} \tag{16}$$

where L is channel length and c_{oxe} is electrical oxide capacitance. Integration constants, labeled IC_1 and IC_2, are generally calculated from the initial conditions that are substituted into (15) – Cauchy's equation:

$$\mathrm{IC}_1 = \frac{2LCA_{bulk_{D0}}}{\sqrt{C_1C_2}c_{oxe}}\arctan(\zeta), \tag{17}$$

$$\mathrm{IC}_2 = C\frac{V_{DSsat_{Ms}}}{I_{Dsat0_{Ms}}}|_{V_{in}=V_2}\ln(|\lambda|) - t_0, \tag{18}$$

where $\zeta = \frac{v_{c_0}\left[\mu_{eff_{D0}}W_{M_S}+C_1\left(A_{bulk_{S0}}-2\right)+C_4\right]}{\sqrt{C_1C_2}}$, $\lambda = \frac{A_{bulk_S}\left[V_2-v_{c_0}\right]-2\left[V_1-V_{TH_S}-v_{c_0}\right]}{V_2-v_{c_0}}$, $\mathrm{IC_{F1}} = \mathrm{IC}_1|_{v_{c_0}=V_{C_F}(0_+)}$, for $0 < t < t_0$ and $\mathrm{IC_{F2}} = \mathrm{IC}_2|_{t_0=t_{0F}, v_{c_0}=V_{C_F}(0_+)}$, for $t \geq t_0$.

Using the voltage V_{0_F} in (18), the initial time t_{0_F} is given by

$$t_{0_F} = \mathrm{IC_{F1}}|_{v_{c_0}=V_{0_F}} - \mathrm{IC_{F1}}|_{v_{c_0}=V_{C_F}(0_+)}, \quad V_{C_F}(0_+) < V_{0_F}. \tag{19}$$

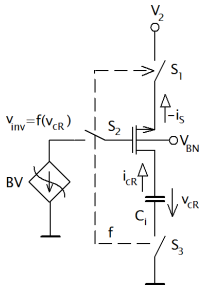

Fig. 7. Configuration for the discharge of the main capacitor

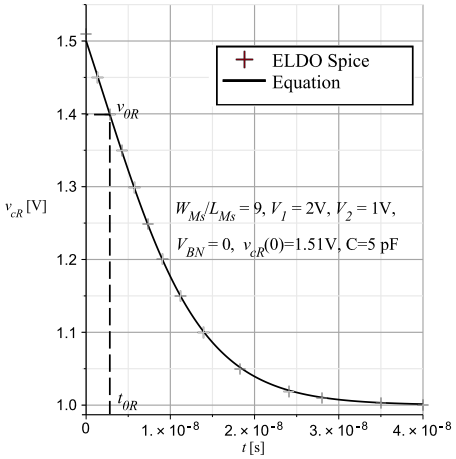

Fig. 8. Time response characteristics of the circuit from Fig. 7.

Coefficients C_1, C_2, C_3, C_4 and C_5 are calculated from:

$$\begin{aligned} C_1 &= -A_{bulk_{D0}}\mu_{eff_{S0}}W_{M_S}, \\ C_2 &= -C_1(V_1 - V_2 - V_{TH_{S0}})^2 - C_3, \\ C_3 &= \mu_{eff_{S0}}W_{M_D}(2V_1 - 2V_2 - A_{bulk_{S0}}V_{TH_{S0}}), \\ C_4 &= -C_1(A_{bulk_{S0}}V_2 - V_1 - V_2 + V_{TH_{S0}}) - C_5, \\ C_5 &= \mu_{eff_{D0}}W_{M_D}(V_2 - V_{TH_{D0}}), \\ C_6 &= A_{bulk_S}V_2 - 2(V_1 - V_{TH_S}), \\ C_7 &= -C\frac{V_{DSsat_{MS}}}{I_{Dsat0_{MS}}}|_{V_{in}=V_2}. \end{aligned}$$

Discharge of the main capacitor is shown in Fig. 7. The CMOS inverter is modeled by the voltage source BV controlled by the time-varying voltage v_{cR}. The switch transistor is ON after the switches S_1, S_2, S_3 are closed at $t = 0$ and the capacitor C_i was charged on the value in the interval of the voltages $v_{C_R}(0) \in (V_2, V_{SP})$.

The initial condition $v_{C_R}(0) \in (V_{IL}, V_{SP})$ will be considered to a complete description of time response characteristics. Then, the main capacitor is firstly discharged by the constant current I_S until the voltage of BV achieves V_1 at time $t = t_{0_R}$,

$$i_{C_R}(t) = \begin{cases} I_{S_R}, & \text{for } 0 < t \leq t_{0_R} \\ i_s(t), & \text{for } t \geq t_{0_R}. \end{cases} \tag{20}$$

Value of the constant current I_{S_R} for $V_{in} = v_{c_R}(0_+)$ follows from the static model, parameters for $i_s(t)$ are mentioned in Tab. 2 (index SR).

The default differential equation for each of the time interval is the same as in the previous case,

$$v_{C_R}(t) = \begin{cases} v_{C_R}(0), & \text{for } t \leq 0, \\ -\frac{I_{S_R}}{C}t + v_{C_R}(0), & \text{for } 0 < t \leq t_{0_R}, \\ \dfrac{V_2\left(A_{bulk_S} - e^{\frac{t+\mathrm{IC_R}}{C_5}}\right)+2\left(V_1-V_2-V_{TH_S}\right)}{A_{bulk_S} - e^{\frac{t+\mathrm{IC_R}}{C_5}}}, & \text{for } t > t_{0_R}. \end{cases} \tag{21}$$

Because the voltages are equal to V_2 in steady state for both the configurations, the coefficients in the exponential functions are also the same. The integration constant $\mathrm{IC_R}$ can be easily expressed as

$$\mathrm{IC_R} = \mathrm{IC_2}|_{v_{c_0}=V_{C_R}(0),t_0=t_{0_R}} \tag{22}$$

and the point t_{0_R} is given by

$$t_{0_R} = \begin{cases} \frac{C}{I_{S_R}}\left[v_{C_R}(0) - V_{IL}\right], & \text{for } V_{SP} \geq v_{C_R}(0) > V_{IL}. \\ 0, & \text{otherwise.} \end{cases} \tag{23}$$

4. Minimization of the Pumping Losses

The sizing of the switch transistor will be discussed in this part. The main criterion of the optimal pump design is based on the maximum voltage gain at the end of each phase of the clock signal, as it is shown in Fig. 9. Sizing of the switch transistor M_{Si} can be set, so that the voltage gain is greater than $2V_2$, better V_{max} at point $T/2$. The transistor length is determined from condition (2) and the width is determined based on the following condition:

$$\max\{V_{C_F}(W_{MS}) + V_{C_R}(W_{MS})\}|_{t=T/2,t>t_0}. \tag{24}$$

The optimal width $W_{MS_{opt}}$ will be searched while using the limit initial conditions to satisfy the worst case that can be taken into account in the real circuit. Using the condition (24) and (16), (21) then the following equality is true:

$$\frac{\mathrm{d}V_{C_F}}{\mathrm{d}W_{MS}}|_{t=T/2,t>t_{0_F}} = -\frac{\mathrm{d}V_{C_R}}{\mathrm{d}W_{MS}}|_{t=T/2,t>t_{0_R}},$$
$$v_{C_F}(0_+) = 0,\ v_{C_R}(0_+) = V_{SP}, \tag{25}$$

and it is giving desired value of the width at the known clock frequency. However, the optimal point can be estimated even in a simpler way. Both the time response characteristics $v_{C_F}(t)$ and $v_{C_R}(t)$ in the intervals $t > t_{0_F}$ and $t > t_{0_R}$ are compared to each other via its linearization in the initial time, as it is shown in Fig. 10.

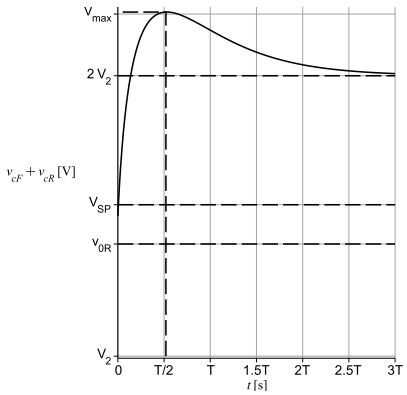

Fig. 9. Time response characteristic for the pumping losses minimization.

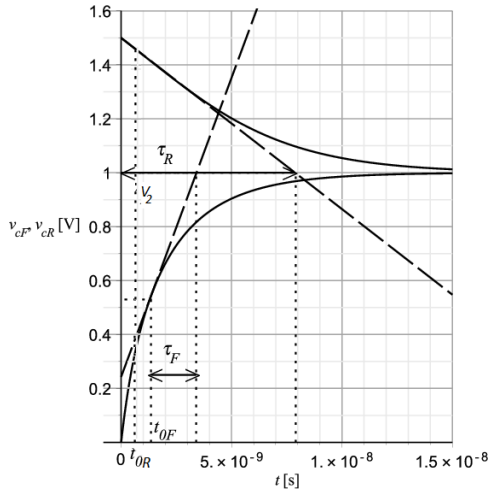

Fig. 10. Linearization of the time response characteristics.

Providing the linear change voltage as in the initial time, the transient process would be terminated at time τ. This parameter is equivalent to the time constant, but it is a function of the bias voltages (is not constant), unlike the first order linear systems. It is derived from the first order Taylor approximation,

$$\tau(v) = \frac{v_{C_\infty} - v_c|_{t=t_0}}{\dot{v}_c|_{t=t_0}}. \tag{26}$$

If the capacitor is charged from the initial value $v_c(t_0)$ to value in the steady state v_{c_∞}, then the voltage on the capacitor reaches the value $\Delta v_c = \alpha\,(v_{C_\infty} - v_{c_0})$ during time $t = k\tau$. Parameters $1 > \alpha > 0$ and $k \geq 0$ are multiple constants. The specific values of α and k parameters calculated for exponential function of $v_{C_R}(t)$, are shown in Tab. 3.

k	0.75	0.9	1	1.5	2	3	5
α	0.5	0.6	0.63	0.76	0.84	0.93	0.98

Tab. 3. Relationship between parameters k and α calculated from (16).

The increase of the pump stage voltage must not fall bellow the value $\Delta V_{max} \geq V_2$ during half of the period, as it is shown in Fig. 7. Discharge time through the parameter τ_R primarily determines the amount of the pumping losses and $\tau_R > \tau_F$, thus

$$\{\Delta v_{C_F} + \Delta v_{C_R} \approx V_2\}|_{t=k\cdot\tau_R+t_{0_F}=T/2}. \tag{27}$$

Thence the parameter α is given by

$$\alpha = \frac{V_2}{V_{SP}}. \tag{28}$$

Parameter τ_R can be calculated from (26), however it is approximately given by the reverse current I_{S_R},

$$\tau_R(W_{M_S}) \approx \frac{(V_{SP} - V_2)C}{I_{S_R}|_{V_{inv}=V_1,V_{in}=V_{IL}}}. \tag{29}$$

Using the condition (27) and respecting the time value t_{0_F} from (19), in which the M_{D_i} transistor is OFF, then the found width $W_{M_{S_{opt}}}$ is given by

$$W_{M_{S_{opt}}} = \frac{kC(V_{SP} - V_2)}{T\hat{I}_{S_R}} + \frac{\hat{I}_{S_R}(Tc_{t_0} + 2a_{t_0}) + \sqrt{D_{t_0}}}{2T\hat{I}_{S_R}b_{t_0}} \tag{30}$$

where

$$a_{t_0} = \frac{2C \cdot A_{\text{bulk}_{\text{D0}}} W_{\text{M}_\text{D}} L \mu_{\text{eff}_{\text{D0}}} V_{0_\text{F}}}{c_{\text{oxe}}},$$
$$b_{t_0} = -A_{\text{bulk}_{\text{D0}}} \mu_{\text{eff}_{\text{D0}}} \mu_{\text{eff}_{\text{SR}}} W_{\text{M}_\text{D}} \left(V_{t_a} + V_{t_b} V_{t_c}\right),$$
$$c_{t_0} = \left(\mu_{\text{eff}_{\text{D0}}} W_{\text{M}_\text{D}}\right)^2 \left(-V_2 + V_{\text{TH}_{\text{SR}}}\right) V_{0_\text{F}} + \\ + \left(\mu_{\text{eff}_{\text{D0}}} W_{\text{M}_\text{D}}\right)^2 \left(-V_2 + V_{\text{TH}_{\text{SR}}}\right)^2,$$
$$D_{t_0} = \left[2kC \cdot b_{t_0}(V_2 - V_{\text{SP}}) - \hat{I}_{\text{S}_\text{R}} \left(Tc_{t_0} + 2a_{t_0}\right)\right]^2 + \\ + 16kCa_{t_0} b_{t_0} \hat{I}_{\text{S}_\text{R}} (V_2 - V_{\text{SP}})$$

and

$$V_{t_a} = V_{\text{TH}_{\text{SR}}} \left(V_{\text{TH}_{\text{SR}}} A_{\text{bulk}_{\text{SR}}} - 2V_1 + 2V_2\right),$$
$$V_{t_b} = V_2 \left(A_{\text{bulk}_{\text{SR}}} - 1\right) - V_1 + V_{\text{TH}_{\text{SR}}},$$
$$V_{t_c} = V_{0_\text{F}} - 2\left(V_2 - V_{\text{TH}_{\text{SR}}}\right).$$

Parameter k is selected from Tab. 3 based on the parameter α from (28), $\hat{I}_{\text{S}_\text{R}}$ is the drain current calculated for the unity width $\left(\hat{I}_{\text{S}_\text{R}} = I_{\text{SR}}/W\right)$.

In case the multiple of the time constant satisfies the session $k\tau_\text{R} \gg t_{0_\text{F}}$, (30) now becomes to

$$W_{\text{M}_{\text{S}_{\text{opt}}}} \approx \frac{2kC(V_{\text{SP}} - V_2)}{T\hat{I}_{\text{S}_\text{R}}}. \tag{31}$$

5. Sizing of the "Diode" Transistor

Analysis results show that dynamic properties are not practically dependent on the sizing of the transistor M_{D_i} in the wide range of the ratio W/L. It only needs to be adequately dimensioned for the pump output load current i_L in steady state. After the clock signal $\bar{\phi}$ goes to H logic level (corresponds to V_{DD}), the output voltage starts from the initial value $V_{\text{out,av}} - V_\text{r}/2$ and can theoretically achieve the maximum value $V_{\text{out,max}}$ during $T/2$. $V_{\text{out,av}}$ is the required average value of the output voltage and V_r is the peak value of the ripple voltage. The situation is shown in Fig. 11. The transistor $M_{\text{D}_{N+1}}$ is on in the active interval of the clock signal.

Time response characteristics will be firstly determined. Providing the capacitive character of the load impedance, the state description of the voltage on the capacitor $v_{\text{out,av}}(t)$ is in an accordance to (15) ($R_\text{L} \to \infty$).

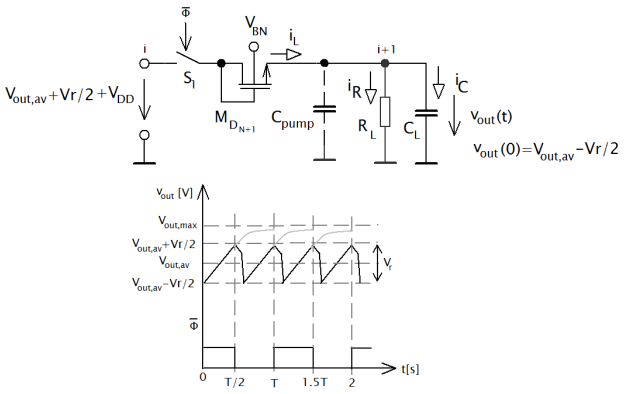

Fig. 11. The last stage of the charge pump and waveform of the output voltage in the steady state.

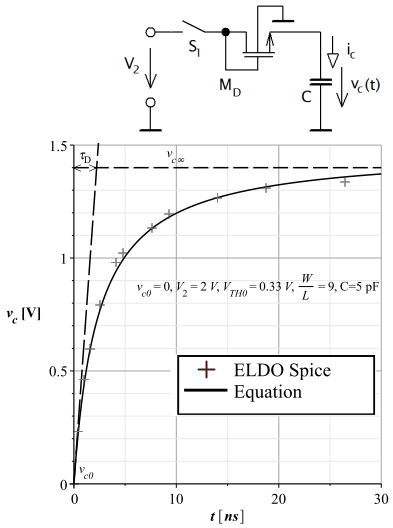

Fig. 12. Time response characteristics of the diode transistor.

The step response characteristics of the circuit in Fig. 12 after closed S at t=0, when the capacitor is charged from the initial value $v_\text{c}(0_+) = v_{\text{c}_0}$ to the steady state v_{c_∞}, is given by

$$v_\text{c}(t) = \begin{cases} v_{\text{c}_0}, & \text{for } t \le 0, \\ \dfrac{W_{\text{M}_\text{D}} \beta_\text{D} v_{\text{c}_\infty} t (v_{\text{c}_\infty} - v_{\text{c}_0}) + C v_{\text{c}_0}}{W_{\text{M}_\text{D}} \beta_\text{D} t \left(v_{\text{c}_\infty} - v_{\text{c}_0}\right) + C}, & \text{for } t > 0. \end{cases} \tag{32}$$

The maximal output voltage value v_{c_∞} is equal to $V_{0\text{F}}$ from (14) and β factor is calculated at the bias voltages in steady state,

$$\beta_\text{D} = \frac{1}{2L} \frac{\mu_\text{eff} c_\text{oxe}}{A_\text{bulk}} |_{V_\text{GS} \approx V_\text{DD}, V_\text{SB} = V_\text{max}}.$$

The increase of voltage α_D at time expressed as the multiples k of the τ_D parameter, $v_\text{c}|_{t=k\tau_\text{D}} = \alpha_\text{D}(v_{\text{c}_\infty} - v_{\text{c}_0})$, is listed in Tab. 4.

k	0.5	0.7	1	2	5	10	20	40	∞
α_D	0.32	0.39	0.48	0.63	0.77	0.85	0.91	0.97	1

Tab. 4. Relationship between parameters k and α_D calculated from (32).

The optimal width of the M_D transistor is determined from a condition, that the voltage v_out from Fig. 11 must achieve the maximal allowable ripple voltage V_r during T/2 at the desired average value of the output voltage. The maximal output voltage $V_{\text{out,max}}$ is calculated from (32), into which the concrete values are substituted for input voltage V_2,

$$v_{\text{c}_\infty} = V_{0_\text{F}}|_{V_2 = V_{\text{out,av}} + V_{r\text{max}}/2 + V_\text{DD}}. \tag{33}$$

Of course, the specified amplitude of the AC voltage value $v_\text{r}(t)$ depends on both the external load R_L, C_L and on the equivalent internal pump impedance including R_pump, C_pump. Consequently, the following inequality must be true:

$$\left\{V_\text{out}\left(W_{\text{M}_\text{D}}\right) \ge v_{\text{c}_0} + \alpha_\text{D}\left(v_{\text{c}_\infty} - v_{\text{c}_0}\right)\right\}|_{t=T/2}. \tag{34}$$

Therefore,

$$W_{\text{M}_\text{D}} \ge \frac{2\left(C_\text{L} + C_\text{pump}\right)}{T\beta_\text{D}\left(v_{\text{c}_\infty} - v_{\text{c}_0}\right)} \frac{\alpha_\text{D}}{1 - \alpha_\text{D}} \tag{35}$$

where pump capacitance may be neglected, provided $C_L \gg C_{pump}$ and $\alpha \geq \frac{V_{r\max}}{v_{c\infty} - v_{c0}}$ with the minimal value of the average voltage $V_{out,av}$. However, parameter α_D should be chosen, so that the load capacitor was charged by the large current all along of the active interval. Consequently, the transistor is fully switched on ($v_{gs} \gg v_{TH}$, strong inversion) and the load voltage is the approximately linear function of time. Results from Tab. 4 show that significant voltage change meets this assumption for α, which no exceeding the value about 0.7. Otherwise, the width quickly grows with $\alpha \to 1$ despite the improvement of dynamic properties. An example of the width calculation vs. α parameter is shown in Tab. 5.

Parameters
$L = 5\mu$m, $\beta_D = 135\,\mathrm{AV^{-2}m^{-1}}$,$V_{DD} = 1$ V,
$V_{out,av} = 3.3$ V, $V_{r_{max}} = 50$ mV, $C_L = 20$ pF, $T = 100$ ns

$\alpha[-]$	0.1	0.2	0.4	0.6	0.8	0.9	1
$W_{M_D}[\mu m]$	5	11	30	68	182	411	∞

Tab. 5. Width of the M_{D_i} transistor vs. α parameter.

6. Experimental Part

The real circuits properties were simulated in the professional environment ELDO Spice, Design Architect-IC v2008.2_16.4. All assertions from the previous parts were be verified in the three-stages charge pump including the real models of all the components.

Parameter		Value
Temperature	ϑ	24° C
Number of stages	N	3
Supply voltage	V_{DD}	1.5 V
Main capacitance	C	40 pF
Load ressistance	R_L	200 kΩ
Load capacitance	C_L	20 pF
Threshold voltage of the	V_{TH0_N}	0.35 V
hvt NMOS and PMOS at 0V	$\lvert V_{TH0_P}\rvert$	0.33 V
Channel length of N(P)MOS	L	5μm
W/L ratio of the M_{S_i}	W_s/L_s	2
M_{P_i}	W_p/L_p	3
M_{N_i}	W_n/L_n	1
M_{D_i}	W_d/L_d	10

Tab. 6. Simulation parameters.

The HVT MOS transistors BSIM 4.2.0 were used that are available in the library MGC Design Kit. The various types of MOSFETs, M_{Si}, M_{N_i}, M_{Pi} and M_{D_i} are the same sized in each the pump stage. Simulation parameters (unless noticed otherwise) are specified in Tab. 6.

Firstly, the equation validity expressing the optimal point W_s/L_s (Fig. 13) will be tested via the comparison of the calculated functional values $V_c = v_{C_F} + v_{C_R}|_{t=T/2}$ from (16), (21) and the pump output voltage value $V_{out,av}$ dependending on the ratio W_s/L_s. The optimal width calculated from simplified (31) is listed in the last line. Setting of the voltages V_1, V_2 and source-bulk bias voltage of the N/PMOS for the calculation must first be resolved.

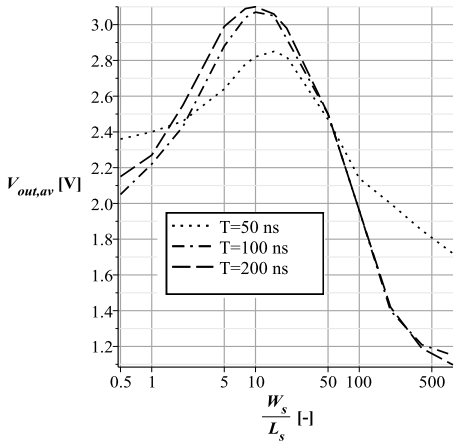

Fig. 13. Pump output voltage vs. the ratio W_s/L_s.

Starting from the fact, that the maximal output voltage value with a change of the circuit parameters (clock frequency, main capacitances, etc.) is achieved, just when the voltage gain of the first pump stage is maximal (it decreases with increasing the number of stages). In accordance to situation in Fig. 1, power supplies of the pump stage (Fig. 2) are $V_2 = V_{DD}$, $V_1 = 2V_{DD}$. The bulk of the NMOS is connected to ground ($V_{SB_N} = V_{DD}$) and bulk of the PMOS is selected so that the inverter switching point was the maximum (at the constant setting of the inverter transistors sizing). Using the definition V_{SP} [12], [15], then $V_{BS_P} = 0$ (in the last pump stage). As a consequence, the worst case of the V_{SP} voltage, labeled $V_{SP_{max}}$ in the N-stages pump is taken into account. Then, general formula of the $V_{SP_{max}}$ ($V_{B_P} = V_{B_N} = 0$) can be written as,

$$V_{SP_{max}} = V_{SP}|_{V_2=V_{DD}, V_1=2V_{DD}, V_{SB_N}=V_{DD}, V_{BS_P}=0}.$$

	$v_{c\infty} = 2V_2 = 3$ V, $V_c(0) = V_{SP_{max}} = 2.41$ V					
	$T = 50$ ns		$T = 100$ ns		$T = 200$ ns	
$\frac{W_s}{L_s}$ [−]	$V_c[V]$	$V_{out,av}[V]$	$V_c[V]$	$V_{out,av}[V]$	$V_c[V]$	$V_{out,av}[V]$
0.5	2.39	2.36	2.42	2.05	2.49	2.15
1	2.42	2.4	2.48	2.22	2.59	2.27
2	2.49	2.46	2.60	2.43	2.75	2.55
5	2.64	2.64	2.81	2.88	2.99	2.99
8	2.76	2.78	2.94	3.04	3.06	3.09
10	2.81	2.82	2.99	3.07	**3.07**	**3.1**
15	2.92	2.85	3.05	3.05	**3.05**	**3.06**
20	**2.98**	**2.82**	**3.07**	**2.92**	3.04	2.98
50	**3.06**	**2.47**	**3.02**	**2.5**	3.01	2.5
100	3.02	2.14	3.01	1.96	3.01	1.96
200	3.01	2.0	3.0	1.4	3.0	1.42
400	3.0	1.85	3.0	1.21	3.0	1.19
800	3.0	1.72	3.0	1.15	3.0	1.097
$W_{MS_{opt}}[\mu m]$	43.8		21.9		10.9	

Tab. 7. Simulation results.

Example calculation of the switch transistor width for practical design will be shown in the following part. The charge pump parameters from Tab. 6 will be considered and: $T = 100$ ns, $V_{Bn} = 0$, $V_{Bp} = 0$. Channel length is same for all the transistors.

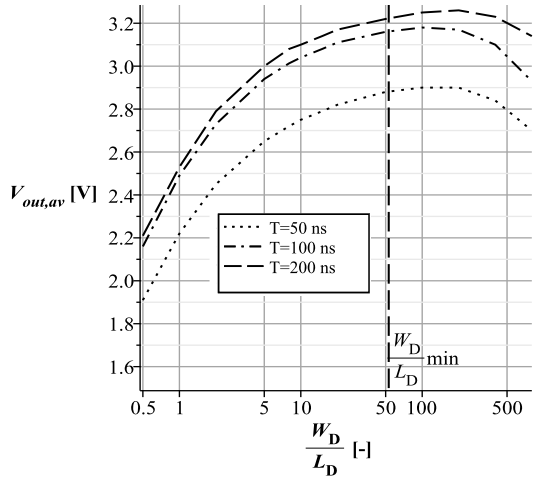

Fig. 14. Pump output voltage vs. the ratio W_D/L_D.

- the maximal inverter switching point [5] at appropriate bias voltage values $V_2 = V_{DD} =$ $= V_{SB_N} = 1.5\,V$, $V_1 = 2V_{DD} = 3\,V$ and $V_{BS_P} = 0$ is $V_{SP_{max}} = 2.41\,V$
- α factor is written as $\alpha = \frac{V_2}{V_{SP_{max}}} = \frac{1.5\,V}{2.41\,V} = 0.62\,[-]$,
- corresponding coefficient alpha deteremined based on the data from Tab. 3 is $k \approx 1\,[-]$,
- The drain current value in the specicific technology process and for unity width is $\hat{I}_{S_R} = \hat{I}_{Dsat0}|_{V_{GS}=V_1-V_2=1.5\,V, V_{SB}=V_2=1.5\,V} \approx 34$ A/m, for $V_{IL} > V_2 + V_{DSsat_{Ms}}$,
- finally, the switch transistors width calculated from (31) is equal to

$$W_{M_S} \approx \frac{2kC(V_{SP} - V_2)}{T\hat{I}_{S_R}} = \\ = \frac{2 \cdot 1 \cdot 40\,pF \cdot (2.41 - 1.5)\,V}{100\,ns \cdot 34\,A/m} \approx 21.9\,\mu m.$$

The results correspond with data from Tab. 6. They show that the pump output voltage is maximal (bold) if the time response characteristic of the pump stage at time $T/2$ does not exceed the value V_{max}, as it is shown in Fig. 9. The optimal width W_{M_s} must be less than the calculated value from (30), (31), otherwise, the pumping losses cause the discontinuous decrease of the output voltage due to the opening the feedback of the system (the condition 1 is not satisfied). It is a critical parameter from the view of the design process.

Conversely, the voltage gain is not changed in a wide ratio range W_D/L_D of the diode transistor, as it is shown in Fig. 14.

7. Conclusion

Guidelines on the design of the switch and "diode" transistors for the cross-coupled charge pump architecture without using long-time iteration process was presented in this paper. The symbolic description was used for calculation. The equivalent channel MOSFETs resistance was designed, so that the voltage gain and power efficiency were maximal. Analytical formulas are including the extreme values of circuit bias voltages to achieve satisfactory results in N-stage architecture, in which these types of the transistors have same dimensions in each of the stages. All the results were verified by the professional simulation software ELDO.

The switch and diode MOSFETs channel length was determined based on the critical electrical field in structure (breakdown voltage and maximal Drain-source voltage), see (2). The width of the switch and "diode" transistor were determined based on the analytical expression of the time response characteristics of the pump stage as an analog block. Switch transistors width, see (30), (31), was found using the criteria of the maximal difference between forward/charge and reverse/discharge current during the period of the clock signal. The ratio W_s/L_s, in which the sum of the time characteristics (reverse+forward) of the pump stage achieve the maximum value was compared with results fort three-stage pump, see Tab. 7. Compliance between both of the values is obvious. Simulation results show that switch resistance cannot be very small because increasing the ratio W/L, the reverse switch current decreases pump efficiency. This ratio can be less than one at the extreme values of input parameters (power supply, clock frequency). Exceeding the critical value of the reverse current, the pump output voltage is discontinuously decreased (see Fig. 13) because the basic condition (1) is not valid. This is an important practical result.

An estimation of the minimal width of the diode transistors W_D, see (35), is possible to determine from the requirements on the output load current and the output ripple voltage. Static and dynamic properties of the pump are quite stable over a wide range of the ratio W_D/L_D, see Fig. 14. Reverse current through the diode transistor is practically zero.

Acknowledgments

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