

FPGA-based Low Latency Inverse QRD Architecture for Adaptive Beamforming in Phased Array Radars

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Abstract. *The main objective of this paper is to facilitate the adaptive beamforming which is one of the most challenging tasks in phased array radars receivers. Recursive least square (RLS) is considered as the most well suited adaptive algorithm for the applications where beamforming is mandatory, because of its good numerical properties, high convergence rate and low misadjustment. In this paper, some RLS variants are discussed and the most numerically suitable algorithm Inverse QR decomposition (IQRD) is selected for efficient adaptive beamforming. A novel architecture for IQRD RLS is also presented, which offers low latency and low area occupation for Field Programmable Gate Array (FPGA) implementation. This approach reduces the computations by utilizing the standard pipelining methodology. Hence, efficient adder and multipliers and Look Up Table (LUT) based solution for square root and division, has highly enhanced the performance of the algorithm. The proposed IQRD RLS architecture has coded in Verilog and analyzed its performance in terms of throughput, hardware resources and efficiency.*

Keywords

Adaptive filters, beamforming, phased-array radars, Recursive Least Square (RLS), Inverse QR Decomposition (IQRD), Field Programmable Gate Array (FPGA)

1. Introduction

Radar signal processing is one of the active area of research due to its vast applications in radar systems like target tracking, navigation. Most of the radar systems are composed of multiple transmitting and receiving phased array antennas, known as phased array radars. These phased array antennas are designed to transmit and receive the spatially propagating signals and to focus on the arriving direction of desired signals as well as suppressed the interfering signals [1], [2]. Beamforming is an important signal processing technique in phased array radars for

directional signal transmission or reception [2]. Figure 1 shows a generalized block diagram of four-channel adaptive beamformer receiver having a uniform linear array structure (ULA) and an adaptive weight calculation (AWC) unit. In ULA, phased array radars, all the antenna elements are arranged along a line with uniform spacing s , to attenuate interferences coming from different directions along with desired signal [3]. AWC unit is based on an over determined system of equations in many cases and various algorithms has been developed to solve these equations. Such a system is also known as adaptive antenna system. AWC usually based on gradient based adaptive algorithms like Least Mean Square (LMS), Normalized Least Mean Square (NLMS), Recursive Least Square (RLS), Kalman filter, assuming all the input signals to ULA system are uncorrelated with each other [3], [4]. But, RLS is considered as the most commonly used algorithm as it has the fast convergence rate to find an appropriate solution and good numerical properties, but it has complex mathematical operations like matrix inversion. Hence, it limits its application in real time systems [5]. In numerical methods, a well-known method known as QR decomposition (QRD) is used to decompose any matrix \mathbf{X} into orthogonal matrix \mathbf{Q} ($\mathbf{Q}\mathbf{Q}^T = \mathbf{I}$), and upper triangular matrix \mathbf{R} ($\mathbf{X} = \mathbf{Q}\mathbf{R}$). So, to overcome the computational complexity, various QR decomposition based RLS variants (QRD, Inverse QRD, Fast QRD) were developed, which are widely used in variety of applications, which leads to more efficient architectures, stability and accuracy [5], [6]. In the paper, the comparisons of few RLS variants are performed and select IQRD RLS as the least computationally expensive algorithm for hardware application.

The primary goal of this paper is to propose and develop a high-throughput architecture of the selected RLS variant, by minimizing its latency and device area occupation for adaptive beamforming application. The speed of the beamformer is limited due to recursive operation based AWC unit, therefore, minimizing latency is a critical issue [4], [7]. In this paper, a novel architecture is proposed for IQRD RLS to reduce the computational complexity by using the standard pipelining methodology and mapped into Virtex5 FPGA because it provides the powerful com-

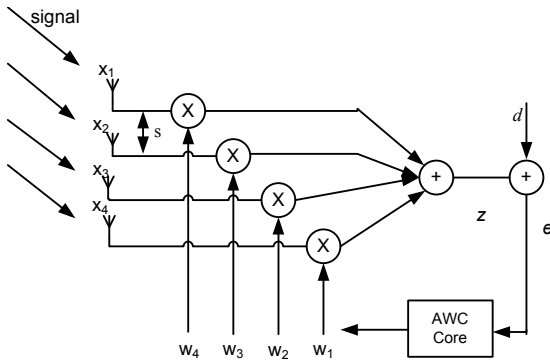


Fig. 1. Adaptive beamformer receiver with ULA structure.

computational architecture features for floating point arithmetic.

The paper is organized as follows: first of all, a brief introduction of adaptive beamforming is presented in Sec. 2. Further, in Sec. 3, a thorough study is performed to select IQRD as the most suitable RLS variant. Section 4 describes the conventional systolic array architecture and the proposed new architecture based on low latency modules. Finally, in Sec. 5, AWC unit implementation in Virtex 5 FPGA is discussed to confirm the advantages of the new structure.

2. Adaptive Beamforming

The core of adaptive beamformer receiver is to detect and estimate the target signal at the input of adaptive antenna array. Such systems are usually consisted of an antenna array along with adaptive processor (AWC) to adjust its weights in real time, such that the main lobe of the radar is focused on the arriving direction of target signal and suppresses undesired signals [3], [6].

The output of beamformer in Fig. 1 is given as:

$$e(k) = d(k) - z(k) \tag{1}$$

where z be the vector array of estimated signal given as

$$Xw = z \tag{2}$$

where w ($m \times 1$) be weights vector, X ($m \times N, m > N$) is the input data matrix, d ($N \times 1$) is the desired training signal and e ($N \times 1$) is the additive noise error vector. The primary goal of the adaptive beamformer is to minimize the mean square error, such that $z(k) \approx d(k)$ and find out the optimized values of unknown weight vector w .

$$\xi(k) = \sum_{i=0}^k \lambda^{k-i} [d(i) - w^T(i)x(k)]^2 = \|e(k)\|^2 \tag{3}$$

where λ is a forgetting factor in conventional RLS [4].

3. RLS Variants for Adaptive Beamforming

In this section, a detail study of RLS variants is performed to select the most efficient one for the AWC unit in

adaptive beamformer. But, first of all a brief introduction of QR decomposition based on Givens Rotation (GR) method is given. A GR rotation matrix $G = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$ is

used to premultiply a two-row matrix and transformed it into upper triangular matrix. Let two-row matrix be given as:

$$A = \begin{bmatrix} \sqrt{\lambda}r_1 & \sqrt{\lambda}r_2 & \dots & \sqrt{\lambda}r_m \\ x_1 & x_2 & \dots & x_m \end{bmatrix} \tag{4}$$

Premultiplying matrix A with G we get

$$\begin{bmatrix} c & s \\ -s & c \end{bmatrix} \begin{bmatrix} \sqrt{\lambda}r_1 & \sqrt{\lambda}r_2 & \dots & \sqrt{\lambda}r_m \\ x_1 & x_2 & \dots & x_m \end{bmatrix} = \begin{bmatrix} r'_1 & r'_2 & \dots & r'_m \\ 0 & x'_2 & \dots & x'_m \end{bmatrix} \tag{5}$$

where

$$r'_1 = \sqrt{\lambda r_1^2 + x_1^2} \tag{6}$$

$$c = \frac{\sqrt{\lambda}r_1}{\sqrt{\lambda r_1^2 + x_1^2}} \tag{7}$$

$$s = \frac{x_1}{\sqrt{\lambda r_1^2 + x_1^2}} \tag{8}$$

In [7], a numerically stable RLS variant QRD RLS, is described which avoids the complex matrix inversion operations. Moreover, it has the possibility of implementation in systolic array architecture (pipelined architecture). Hence, many researchers considered QRD RLS as the most suitable adaptive algorithm for hardware implementation [8–10]. The QRD decomposes input data matrix X through an orthogonal triangularization approach like Givens rotation (GR), Householder transformation or Gram Schmidt orthogonalization [11]

$$X = QR \tag{9}$$

In most of the cases GR is considered as the most numerically well-conditioned method. Q be the unitary matrix ($QQ^T = I$) generated as the sequence of Givens rotation matrices in [11], and R is the upper triangle matrix which is also the Cholesky factor of autocorrelation matrix $R = X^T X$ [11]. So, equation (9) can be written as:

$$QX = R \tag{10}$$

Premultiplying (1) with Q we get

$$Qe = Qd - QXw \tag{11}$$

Let $e' = Qe$ and $d' = Qd$, so equation (11) can be written as

$$e' = d' - R w \tag{12}$$

From (12) the weight update equation can be written as

$$w = R^{-1}d', \quad e' \approx 0 \tag{13}$$

The above equation is the solution of least square problem which is obtained by back substitution process. Hence, the QRD RLS algorithm is composed of two steps: first the QR

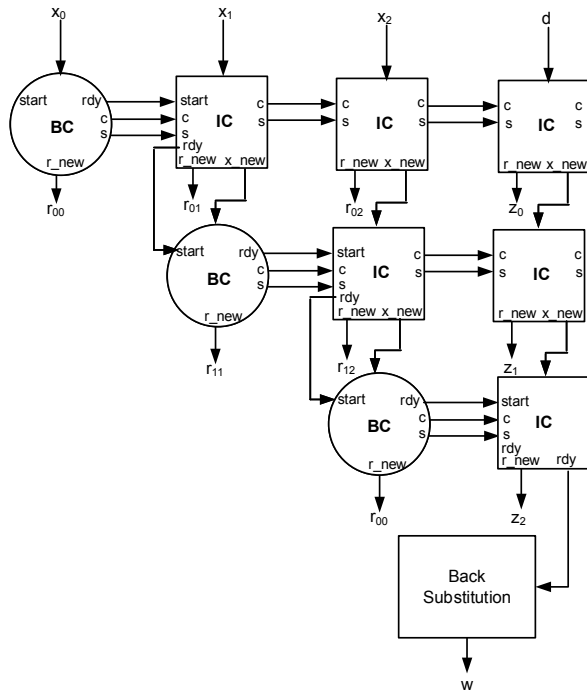


Fig. 2. QRD RLS systolic array.

decomposition of data matrix X (9) is performed and has systolic realization. In step 2, back substitution process begins for weight calculation (13), as shown in Fig. 2.

IQRD RLS is another important variant of RLS proposed by Alexander and Ghirnikar [12], to avoid the numerically tedious back substitution process for weight calculation. The core idea is to update the inverse matrix R (13) in each iteration of systolic array. So, the weights of filter are computed within systolic array. In [11], a new weight update equation is derived which is given as:

$$w(k) = w(k-1) + e(k)R^{-1}(k)R^{-T}(k)x(k) \quad (14)$$

where the term $R^{-1}(k)R^{-T}(k)x(k)$ is known as the Kalman gain. The systolic realization of IQRD RLS will be discussed in Sec. 3. Hence, IQRD RLS is less computationally expensive as compared to QRD RLS.

In Fast QRD (FQRD) RLS, matrix update equation is replaced by vector update equations. In [11] detail derivations of these equations are given, which further reduces the numerical complexity as compared to QRD RLS and IQRD RLS algorithms. Although, FQRD RLS is numerically less complex, but it has no weight update procedure, so it is limited to applications which try to estimate the output error vector [13].

In this section, three important RLS variants and their properties are discussed and summarized in Tab. I. It is worth mentioning that QRD and IQRD are computationally more complex than FQRD, but FQRD has no weight update procedure. So, we cannot consider it for adaptive beamforming application. On the other hand, QRD involves more computations (two step procedure) so it is also not preferable. Due to above reasons, IQRD RLS is the well-suited algorithm for hardware implementation.

Algorithm	Computational Complexity	Weight Update Procedure
QRD RLS	$O(N^2)$	Back Substitution
IQRD RLS	$O(N^2)$	Within Systolic array
FQRD RLS	$O(N)$	No Procedure

Tab. 1. Properties of RLS variants.

3.1 Performance Analysis of Adaptive Beamforming in Terms of Radiation Pattern

The performance analysis of adaptive beamforming, using RLS adaptive algorithm is done by varying different beamformer parameters. Researchers have performed the analysis of adaptive beamformers for smart antennas based on adaptive algorithms Least Mean Squares (LMS), Sample Matrix Inversion (SMI), Recursive Least Squares (RLS) and Conjugate Gradient Method (CGM). The analysis is done by varying the inter element spacing and the number of antenna elements for each algorithm and studying the radiation patterns, amplitude response, mean square error and absolute weights for adaptive beamforming algorithms [14], [15]. We assume a ULA beamformer with an operating frequency of 1 GHz. It receives an echo signal from the single target at azimuth of 30° and an interference signal at -45° . Simulations show that the RLS adaptive algorithm rejects the interference at -45° and enhanced the target signal at 30° . The following procedures are adopted for further analysis of RLS based adaptive beamformer:

- Change the number of antenna elements.
- Change the antenna elements inter space.

Figure 3 depicts the performance of beamformer with different number of antenna elements. The selected numbers of antennas are 10, 15 and 20. It is clear from the radiation pattern that when the number of antenna increases the main lobe of the beamformer is shrunk and pointed accurately towards the target angle and the side lobes are much suppressed. On the other hand, the perfor-

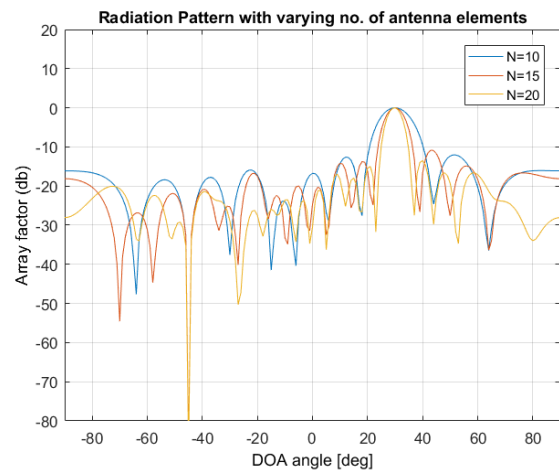


Fig. 3. Radiation pattern with different number of antennas N .

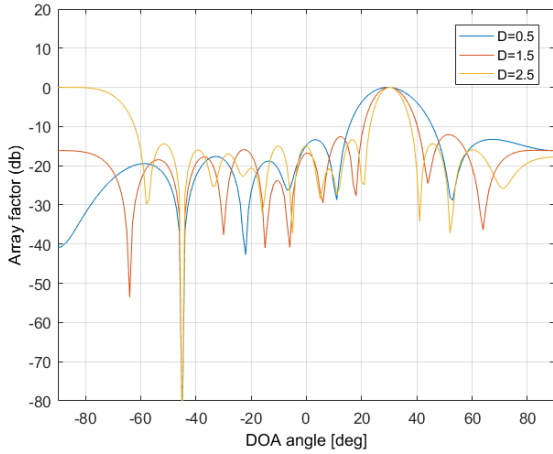


Fig. 4. Radiation pattern with different inter antenna element space D .

mance is also judged in terms of changing antenna elements inter space. The selected inter spaces are 0.5, 1.5 and 2.5 mm. Figure 4 is the resulting radiation pattern in which the performance of the adaptive beamformer is improved as the distances between the antenna elements are increased. The side lobes are also suppressed in a much better way.

Hence, the RLS based adaptive beamformer has a good performance and accuracy as the numbers of antenna elements are increased as well as the distance between each antenna elements is also increased.

4. IQRD Systolic Array Architecture

Systolic arrays are the well-known concept for matrix triangularization and inversion [16], [17] and the same idea is adopted for IQRD-RLS algorithm. Figure 5 shows the conventional systolic realization of the IQRD-RLS algorithm. The IQRD systolic triangular array consists of four types of processing cells; Boundary Cell (BC), Internal Cell (IC), Inverse Internal Cell (IIC) and Final Cell (FC).

A Boundary Cell determines the rotation parameters $\cos \alpha$ and $\sin \alpha$ to perform the rotations on input complex data rows \mathbf{x} , from data matrix \mathbf{X} and update the corresponding row values of \mathbf{R} matrix which is an upper triangular matrix. It also sends the rotation parameters to the right neighboring Internal Cells [16], [18]. The corresponding equations (6), (7) and (8) are modified as:

$$\cos \alpha = c = \frac{\sqrt{\lambda} \ r}{\sqrt{\lambda r^2 + |\mathbf{x}|^2}}, \tag{15}$$

$$\sin \alpha = s = \frac{x}{\sqrt{\lambda r^2 + |\mathbf{x}|^2}}. \tag{16}$$

BC is more complex than IC, IIC and FC because it performs square-root and inverse operations. All the other cells perform only multiplication and inverse operations.

Researchers have performed a lot of work to find a square-root and division free BC unit for systolic arrays. In [19], the following data transformations are applied to seek the square-root and division free expressions for transformed data.

$$r_j = \frac{1}{\sqrt{\alpha_1}} a_j, \quad x_j = \frac{1}{\sqrt{\beta_1}} b_j, \quad r'_j = \frac{1}{\sqrt{\alpha_2}} a'_j, \quad j = 1, 2, \dots, m, \tag{17}$$

$$x'_j = \frac{1}{\sqrt{\beta_2}} b'_j, \quad j = 2, 3, \dots, m. \tag{18}$$

However, the number of multiplications is increased due to these transformations, but it is a good approach to improve the system latency and reduce number of computations. In [8], another single cycle look-up table (LUT) based approach is used to replace the square root and inverse operations and to optimize the QRD RLS latency. This approach gives much improvement in overall performance of QRD RLS algorithm.

An Internal Cell (IC) received the rotation parameters $\cos \alpha$ and $\sin \alpha$ from the Boundary Cell (BC) in each row, and performed the rotations on the input values of data matrix \mathbf{X} and updated the x and r values. The corresponding update equations are given as follows [16], [17]:

$$r_n = \sqrt{\lambda} c \cdot r + s \cdot x, \tag{19}$$

$$x_n = c \cdot x + \sqrt{\lambda} s \cdot r. \tag{20}$$

Inverse Internal Cells receive the sine and cosine value of the rotation angle from the internal cell in the same row. Some part of the inverse internal cell operation is similar to the internal cell; i.e. it rotates the input data by multiplying it with input rotation angles. Along with this operation, Inverse internal nodes of IQRD-RLS use $\lambda^{(-1/2)}$ in (12) and (13). In this paper, we consider the case when $\lambda = 1$, so that IIC is equivalent to IC units.

Final Cell (FC) performs two functions: it received the rotation parameters $\cos \alpha$ and $\sin \alpha$ to rotate the input data and generate the updated filter weights using the following relation [10]

$$w = (-1) \cdot \gamma \cdot \sqrt{\lambda r^2 + |\mathbf{x}|^2} \tag{21}$$

where γ is computed using the following relation

$$\gamma(k) = \prod_{i=0}^N \cos \alpha_i(k). \tag{22}$$

A design methodology has been proposed to optimize the throughput and latency of the IQRD-RLS architecture. In Fig. 6, a block diagram of the proposed architecture is presented, which utilizes the standard pipelining methodologies and has 50% reduction in number of BC, IC and IIC units (Tab. 2). We have further optimized the IQRS RLS architecture, by omitting the square-root and division operations in BC, in terms of single cycle single cycle look up table (LUT) as shown in Fig. 7. Generally, a look up table

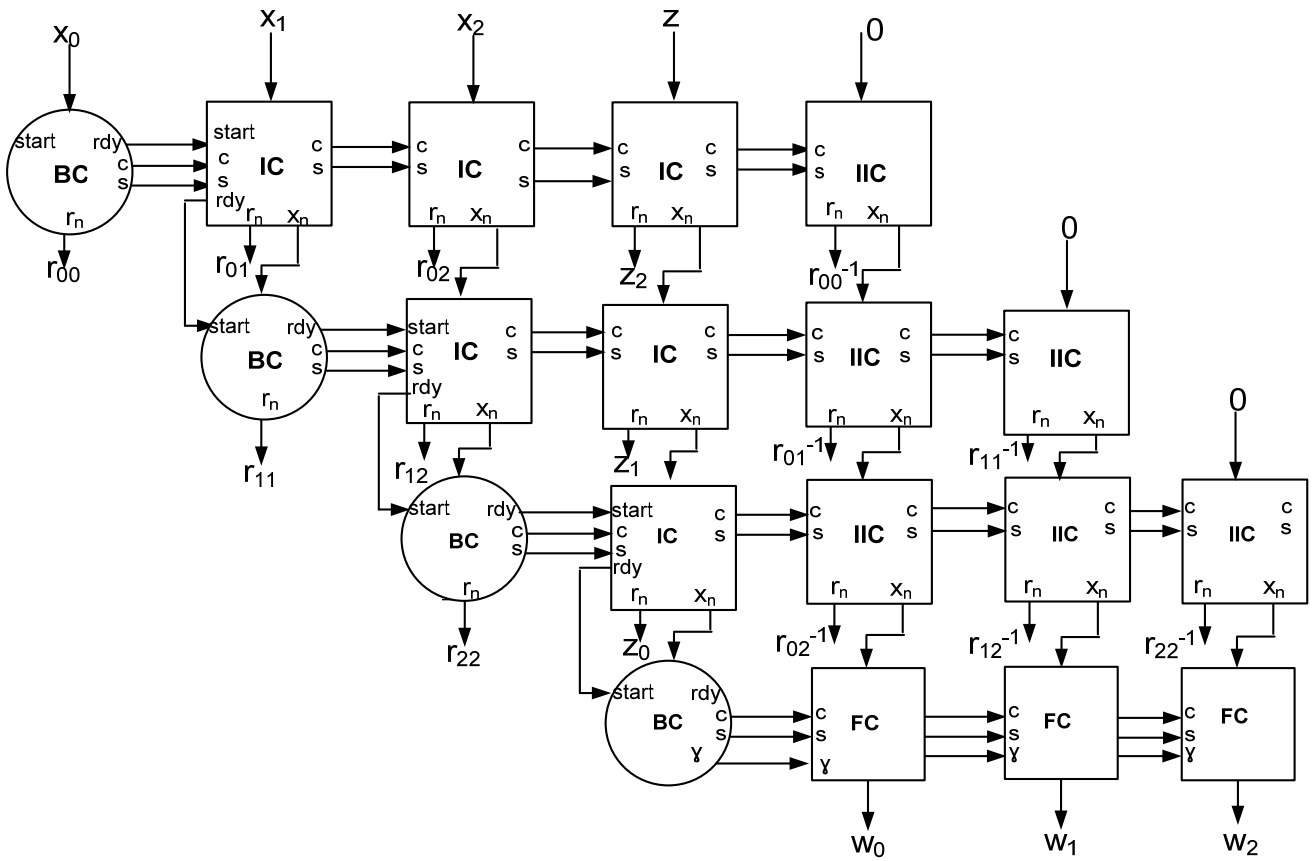


Fig. 5. Conventional IQRD systolic array.

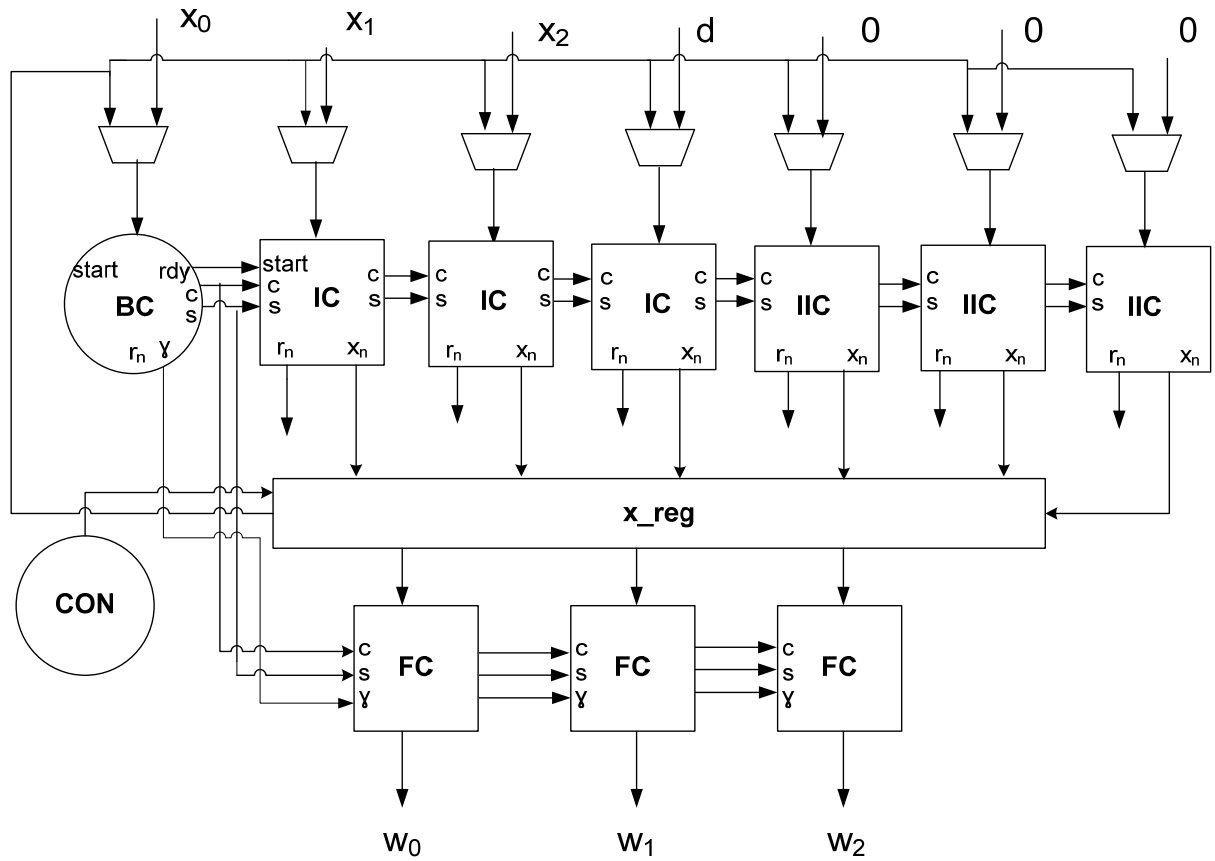


Fig. 6. The proposed IQRD architecture.

(LUT) is a table that determines what the output is for any given input. In FPGA truth tables are used to implement any digital logic. In [8], the same methodology is adopted for QRD RLS algorithm. This scheme avoids the complex hardware implementation with considerable decrease in latency and improves the speed of overall system. In some previous work the conventional implementation of BC is based on CORDIC algorithm, for non-recursive applications [20], [21]. But, digital beamforming is a recursive procedure, so, the conventional approach would not pay off because it leads to considerable latency. In the proposed architecture, the pipelined registers (R_reg, x_reg, Rinv_reg) are introduced which not only holds the updated values, but also feedback them to BC, IC and IIC cells. The controller CON handles the control signals as well as feedback timings. Hence equations (15) and (16) can be modified as:

$$A_s = \lambda r^2 + |\mathbf{x}|^2 = \lambda r^2 + x_i^2 + x_r^2, \tag{23}$$

$$A_{ss} = \sqrt{\lambda r^2 + |\mathbf{x}|^2}, \quad A_i = \frac{1}{A_{ss}}, \tag{24}$$

$$c = \sqrt{\lambda} r \times A_i, \tag{25}$$

$$s_i = x_i \times A_i, \quad s_r = x_r \times A_i. \tag{26}$$

The IC unit received the c , s_i and s_r values from neighboring BC to compute (19) and (20) and update the values of x_{ni} , x_{nr} and r_n . These computations required only adder and multiplier units as shown in Fig. 8. The updated values x_{ni} , x_{nr} are stored in pipelined register x_reg and also feedback to IC module, and updated r_n is stored in internal memory of IC. The c , s_i and s_r are also sent to the neighboring IC (Fig. 8).

One of the major differences between the LUT implemented in [8] and in this paper, is the floating-point representation format. In [8], the latency optimization of LUT is discussed with a defined N bits fixed point number format, including 1 sign bit, i integer bits ($i > 1$) and f frac-

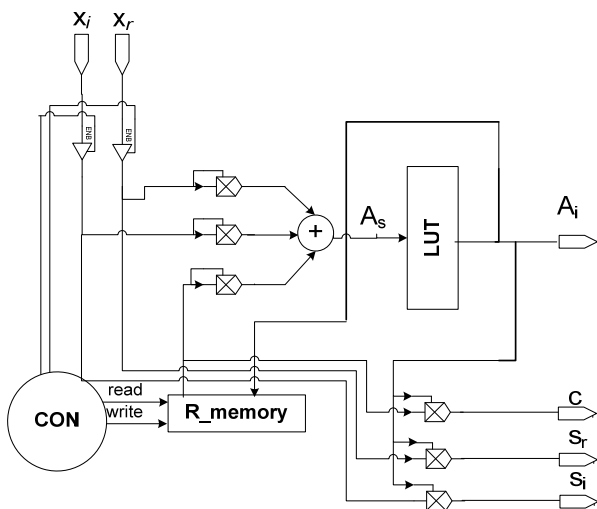


Fig. 7. Boundary Cell (BC) architecture.

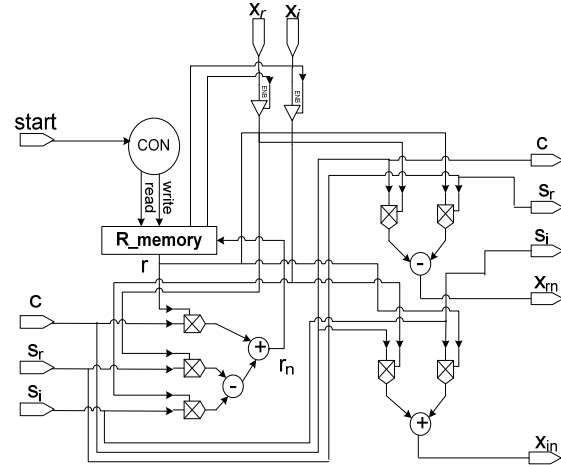


Fig. 8. Internal cell (IC) architecture.

Data matrix X [size]	No. of BC		No of IC		No of IIC	
	Conventional Architecture	Proposed Architecture	Conventional Architecture	Proposed Architecture	Conventional Architecture	Proposed Architecture
3×3	4	1	6	3	6	3
4×4	5	1	10	4	10	4
5×5	6	1	15	5	15	5

Tab. 2. Comparison between the proposed and conventional IQRD architecture.

tion bits ($f > 1$). But, the floating-point multiplier and adder are not discussed with the new defined number format.

In this paper, we have utilized the same LUT approach for IQRD RLS architecture with single precision IEEE 754 format due to its wider range over fixed point. The single-precision numbers are stored in 32 bits: 1 for the sign, 8 for the exponent, and 23 for the fraction [22]. In the proposed architecture, the computation of A_i and A_{ss} are handled in single LUT, whereas A_s is the 32-bit input address field to the LUT as shown in Fig. 7. Simulation results show that 97% of the A_s values are greater than 1 as

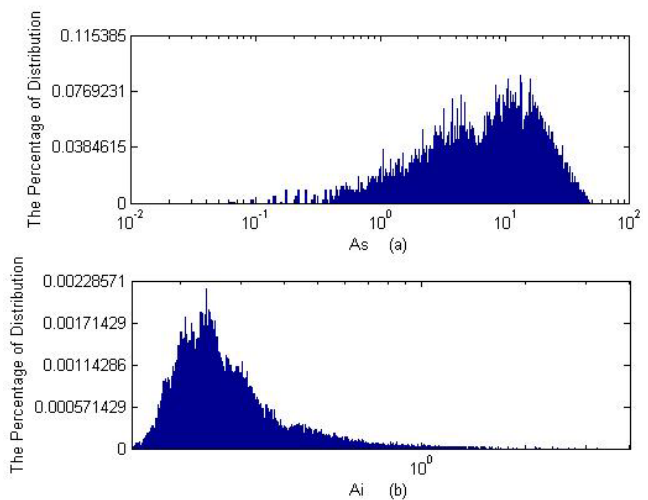


Fig. 9. (a) Histogram of A_s . (b) Histogram of A_i .

shown in Fig. 9a, when the all input variables in (23) have a typical uniform distribution within the range of $[-4, 4]$, and their corresponding output values (A_i) are very small (Fig. 9b). Hence, probability of occurring a value less than 1 is very low thus reduces the range of input values A_s for LUT. The output of the LUT A_i has 32-bit bandwidth, which is used to compute the c , s_i and s_r values, for the IC units.

5. Implementation and Results

In this paper, we have optimized the BC module of systolic array in terms of complex mathematical operations. Many researchers also performed a lot of work in single precision floating point multiplier which is also a complex mathematical operation in hardware [23–25], but we keep our focus in divider and square-root operations and use the multiplier core of the FPGA. Xilinx Virtex 5 FPGA is the selected platform for hardware implementation.

As we have already discussed, adaptive algorithm is a basic part of the beamforming system and we select the IQRD-RLS algorithm as the most suitable algorithm. Three types of architectural modules are designed to judge the performance of algorithm in terms of latency, throughput (1sample/clock Time \times clock cycles), error and efficiency (throughput/number of slices). The details are:

1. MD₀ (module 0), a *conventional* systolic array architecture with single precision floating point multipliers, dividers and a square root module (generated with Coregen software).
2. MD₁ (module 1), a *proposed* systolic array architecture with single precision floating point multipliers, dividers and a square root module (generated with Coregen software).
3. MD₂ (module 2), a *proposed* systolic array architecture with LUT based BC for divider and square root operation.

where MD stands for module. A radar target detection scenario is simulated in MATLAB to generate the data points for the testing of MD₀, MD₁ and MD₂. First, a radar received signal is modelled having one target at azimuth angle 30°, and two interferences at azimuth 15° and 45°, respectively. Assume that both targets and radar lie at the same; i.e. elevation angle is equal to zero. Figure 10 shows the radiation pattern. The received signal is impinged on 3 element ULA beamformer based phased array radar to generate almost 10⁴ data points.

In adaptive beamforming application, latency is an important performance metric which affects the overall system throughput. To judge the LUT effects on algorithm performance we compare the latencies and throughput of the architectural modules. Table 3 details the latency of each unit in system individually, and throughput of adaptive filter (3-tap) for IQRD-RLS algorithm with three dif-

ferent architectural modules; i.e. MD₀, MD₁, MD₂. These modules are modelled using Verilog and their behavior description is placed and routed on Virtex5 device by ISE14.1i tool. It is clear from Tab. 3, the proposed architecture based module MD₂ module has offered 9 times reduction in latency as compared to MD₀ and MD₁ modules because of its optimized single cycle LUT based architecture. On the other hand, MD₂ module of IQRD-RLS has a higher throughput as compared to QRD-RLS M2 module. It is again important to notify that in [8], QRD-RLS is implemented using a new floating point format, whereas we implement the IQRD-RLS with standard IEEE-754 single precision floating point representation. Hence, it is again proved that IQRD-RLS is the most suitable algorithm for adaptive beamforming application.

Algorithm accuracy of the proposed architecture and in presence of LUT is found out by measuring the difference between the weight coefficients of the ideal method and the proposed method in MD₂ with 10⁴ simulated samples. This is also known as weight error. Results show that the weight error is less than 0.00216 for 96% samples. Figure 11 illustrates the filter weights of the ideal and proposed methods for 3 tap beamformer (For clarity of the image we plot only 200 iterations).

The device utilization details or hardware summary are given in Tab. 4. It is noteworthy that MD₂ outperforms in terms of area efficiency and throughput. The conventional architecture MD₀ has the highest area efficiency, while MD₁ occupies much lesser area as compared to MD₀. The hardware efficiency and throughput are found out to draw a reasonable comparison between the architectures. To the best of our knowledge, this is the first implementation of IQRD RLS algorithm in FPGA, so, the performance of MD₂ is also measured, after it is synthesized for different target FPGAs as shown in Tab. 5. The throughput of the IQRD proposed architecture in all FPGAs is better than the QRD [8]. Hence, simulation results have clearly indicated that the IQRD RLS is the most suitable algorithm for adaptive beamforming due to its better throughput, hardware efficiency and latency.

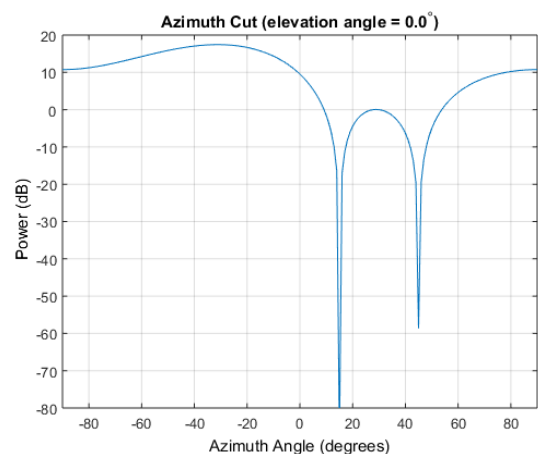


Fig. 10. Radiation pattern.

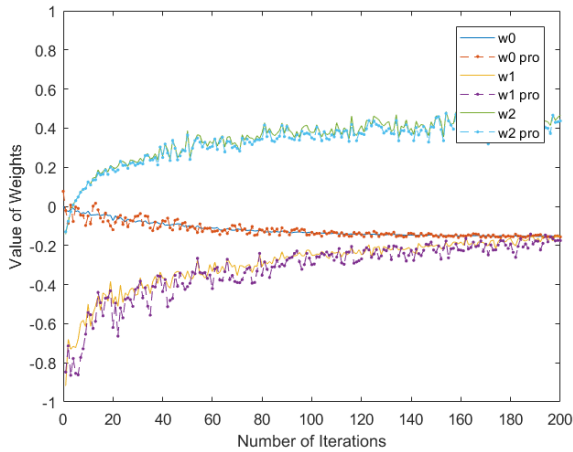


Fig. 11. Weight error.

Algorithm	IQRD RLS			QRD RLS [8]	
	MD ₀	MD ₁	MD ₂	Modules	M ₂
BC	46	46	3	BC	5
IC	5	5	5	IC	3
FC	5	5	5	---	---
Total	455	455	52	Total	76
Throughput [MSamples/sec]	0.44	0.44	3.92	Throughput [MSamples/sec]	2.45

Tab. 3. Comparison between IQRD and QRD [8] latency and throughput.

Hardware Resources	MD ₀	MD ₁	MD ₂
Slices	61%	28%	3%
4-input LUT	18%	14.4%	5%
DSP48	55%	41%	5%
ROM	0%	0%	52%
Avg. Area	38.2%	21.6%	13.92%
Area Efficiency	0.011518	0.02037	0.22923

Tab. 4. Hardware resources.

No.	System	Slices.	Throughput
1.	Spartan-3 (exc3s500)	5891	3.01
2.	Virtex-4 (vsx55)	5603	3.24
3.	Virtex-5 (vtx150)	5001	3.92

Tab. 5. Comparison between FPGAs.

6. Conclusion

A low latency architecture is presented that implements the IQRD algorithm for beamforming application using system level hardware tools. The proposed architecture improves the divider and square root operations via LUT approach. Moreover, it is mapped in Virtex5 FPGA by Xilinx and achieved the minimum errors between the real and ideal weight values. Hence, the proposed architecture is outperforming in terms of area efficiency, throughput, and latency, and the most suitable algorithm for adaptive beamforming. In future work, the multiplier and adder units can be implemented via LUT, for further improvement in latency and throughput.

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