Ultra-Low Voltage Analog IC Design: Challenges, Methods and Examples

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Abstract. *The paper brings an overview of main challenges and design techniques effectively applicable for ultra-low voltage analog integrated circuits in nanoscale technologies. New design challenges linked with a low value of the supply voltage and the process fluctuation in nanotechnologies, such as device models, robustness to process variation, device mismatch and others are discussed firstly. Then, design techniques and approaches to analog integrated circuits towards (ultra) low-voltage systems and applications are described. Finally, examples of basic building blocks of ultra-low voltage analog ICs designed in standard CMOS technology using such design techniques are presented. Finally, the developed circuits are compared to the state-of-the-art solutions in terms of the main parameters and features.*

Keywords

Ultra-low supply voltage, analog design, integrated circuits, ultra-low voltage design techniques, bulk-driven

1. Introduction and Motivation

Recent enormous advance of semiconductor fabrication technology has allowed steep trends in the shrinkage rate of integrated circuits (IC) die area. According to [1], in 2017, there was fabricated a chip in 10 nm CMOS process node with the density of 100 millions of transistors per 1 mm^2. Such an integration density brings great enhancement of computational power per area. However, this trend brings also crucial drawback, as downscaled process nodes suffer from the random fluctuation of process parameters, voltage and temperature sensitivity (PVT) along different samples on wafer.

Design of low-volatge (LV)/ultra-low voltage (ULV) and low-power (LP) analog and mixed-signal ICs in modern nanotechnologies represents a real challenge for circuit designers and researches, since it introduces several limitations in numerous aspects. Firstly, since advanced nanoscale technologies offer a possibility to design analog, digital, and radio-frequency (RF) circuits as well as micro-electromechanical systems (MEMS) on a single chip, there is usually issue of a common value of the supply voltage. With the technology development, the value of the supply voltage is scaled down significantly. However, the threshold voltage (V_{TH}) of MOS devices is not lowered with the same pace. This fact reduced the voltage headroom for conventional circuit topologies (e.g. cascode structures) to operate correctly. Moreover, low value of the supply voltage influences the main parameters of analog ICs, such as dynamic range (DR), power supply rejection (PSR), noise immunity, etc. Another limiting factor lies in the significant fluctuation of process parameters in nanoscale technologies, which brings a new requirement to IC design - circuits have to be robust enough against process, temperature and voltage variations.

Advanced nanoscale fabrication processes bring several limitations to ULV analog IC design. Firstly, it severely constrains the level of inversion the MOS transistors operate in. Resulting in higher mismatch between transistors, higher temperature sensitivity, lower transition frequency, much higher area requirements and many more [2]. The second issue lies in limited possible number of stacked transistors in order to ensure an operation in saturation region. According to [3], theoretical lower limit for saturation voltage of MOS transistor is defined as $V_{DSsat(min)} \approx 4kT/q$, which at room temperature equals about 105 mV. Hence, the novel circuit topologies are heavily modified and their mode of operation is usually far from conventional approach. The third restriction is the dynamic voltage range, which affects the signal-to-noise ratio. This is usually compensated by rail-to-rail operation or differential signal representation for the price of circuit complexity.

In order to overcome these limitations, new ULV design techniques based on unconventional approaches have to be employed. Additionally, brand new topologies of basic building blocks for analog ICs, which offer reliable operation at ultra-low supply voltage conditions have to be developed. Towards improving the main parameters of ULV analog ICs, the fully differential signal processing is usually needed.

The rest of the paper is organized as follows. In Sec. 2, new challenges in ULV analog IC desing in nanotechnologies are addressed. Section 3 brings an overview of design techniques and approaches to analog IC design that can be used to overcome serious limitations linked with a low value of the power supply and process fluctuations. Examples of ULV analog building blocks and their comparison to the state-of-the-art achievements are presented within Sec. 4. Finally, some conclusions are given in Sec. 5.

2. Challenges in ULV Design

As mentioned above, there are several different negative outcomes that are traded for low-power consumption or low-voltage operation in age of battery-powered devices. In the following sections, the main challenges and issues of ULV analog IC design in nanotechnologies will be addressed in more details.

2.1 Inversion Modes of a MOS Device

MOS transistor can operate in different modes, depending on the level of inversion in the channel [4]. In strong inversion, the channel is fully formed, which is not the case in weak inversion. The transition between these two regions of operation is progressive, through a range called moderate inversion. The transistor behavior is rather different in the strong and weak inversion regions, which can be observed in the change from the square–law transfer characteristic in the former, to the exponential one in the latter. According to [5], the mode of MOS operation can be described using the inversion coefficient ic, calculated using (3), where I_f and I_r are the forward and reverse components of the drain current I_D respectively, as defined in (1). The specific current I_spec is described in (2), where n is the slope factor, μ is the mobility of current carriers, C_ox is the oxide capacitance per area, W is the channel width, L is the channel length and U_T is the thermal voltage. The transistor operates in strong inversion for $ic \gg 1$, in weak inversion for $ic \ll 1$, and in moderate inversion for $ic \cong 1$.

$$I_\mathrm{D} = I_\mathrm{f} - I_\mathrm{r}, \tag{1}$$

$$I_\mathrm{spec} = 2n\mu C_\mathrm{ox}\frac{W}{L}U_\mathrm{T}^2, \tag{2}$$

$$ic = \max\left(i_f = I_\mathrm{f}/I_\mathrm{spec}, i_r = I_\mathrm{r}/I_\mathrm{spec}\right). \tag{3}$$

In conventional analog IC, transistors operate in strong inversion [6]. However, in modern CMOS nanoscale technologies, the supply voltage has been significantly decreased to avoid high electric fields within the ever smaller devices and the related unwanted effects [5]. However, the threshold voltage was not scaled proportionally, as this would have resulted in increased leakage currents [7] and thus, larger power consumption [8]. In Fig. 1, the trend of the supply voltage V_DD and the threshold voltageV_TH reduction for shorter transistor channel lengths can be observed. It shows that while

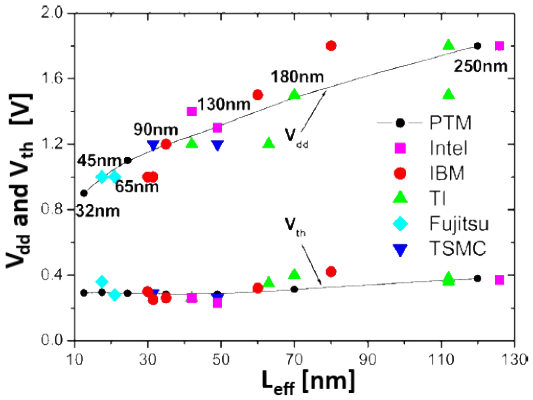

Fig. 1. Trend of supply (V_dd) and threshold (V_th) voltage scaling vs the effective transistor channel length (L_eff) [8].

V_DD has changed drastically, V_TH has remained almost constant. This leads to the reduction of the voltage headroom, which consequently limits the available overdrive voltage. This is especially important in circuits utilizing stacked transistors, such as various cascode structures commonly used in basic analog building blocks. The use of stacked transistors increases the minimum supply voltage required to achieve strong inversion in the circuits to many times more than V_TH. As shown in Fig. 1, this condition can not be fulfilled in modern technologies. To utilize known topologies in these conditions, the operating point of the transistors is moved from strong to moderate or weak inversion.

An advantage of using transistors operating in weak inversion is the significantly reduced power consumption in comparison to those working in strong inversion. However, this decreases the bandwidth and increases the size of the transistors, as will be described later. Therefore, the use of transistors in weak inversion is favourable mainly for low-frequency and low-power applications.

2.2 Device Models

Advanced nanoscale CMOS technologies brought a need for new design approaches and new simulation models of MOS devices that would be more accurate in the whole range of inversion regions. Therefore, to design circuits operating in these conditions, a new type of MOS transistor models is needed. A good example is the charge-based EKV model that accurately predicts the behaviour of MOS transistors in all inversion types [5], [9]. EKV model uses the smallest number of core parameters needed for a proper and accurate behavioural modelling. EKV model uses one equation for all inversion regions (including weak, moderate, and strong inversions). This model was successfully applied to low-voltage and low-power IC design with good accuracy. Moreover, it is very useful for analog circuit designer because significantly simplifies hand-made calculations. The basis of this model is parameter g_m/I_D, which expresses the transconductance efficiency of a MOS transistor and describes how effectively the current (power) is transformed to the device transconductance.

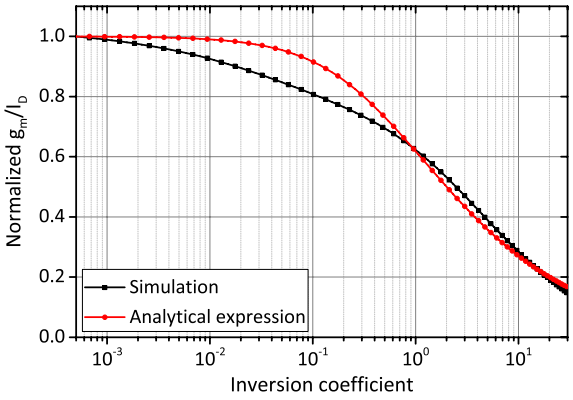

Fig. 2. Normalized g_m/I_D vs inversion coefficient ic.

There are several equations describing the relationship between the g_m/I_D parameter and the inversion coefficient ic that defines the particular inversion region. These equations differ in interpolation accuracy of the transition region between the individual inversion regions. The simplest expression of g_m/I_D is given in [3]

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \frac{1}{0.5 + \sqrt{0.25 + ic}} \tag{4}$$

where n is the MOS transistor slope factor and U_T is the thermal voltage. Parameter g_m/I_D is not technology-related, which predicts its wide usability over different CMOS technologies. Nevertheless, simulation analysis of this characteristic using the widely used BSIM transistor models shows an inaccuracy in the weak inversion and moderate inversion regions. More details about ic will be given in Sec. 3.4. Comparison of the characteristics obtained by analytical method and simulation shows significant error in these regions in a standard 130 nm CMOS technology, as can be observed in Fig. 2.

2.3 Robustness to PVT Fluctuations

With downscaling the process technology, it is rather difficult to ensure the designed geometric dimensions, doping profile or dielectric layer thickness of fabricated chips. These physical variations obviously reflect themselves on electrical parameters of ICs. The MOS transistor threshold voltage V_{TH} is one of the most essential electrical parameters of ICs, which is in this way degraded. The standard deviation of V_{TH} in 45 nm CMOS process node reaches approximately 16 % of the mean value [10]. Other affected electrical parameters include parasitics of the chip interconnects, namely parasitic impedance and parasitic capacitance [11]. The characteristics of semiconductor structure alter with time, so electrical parameters of ICs are also affected by ageing. This creates a long-term drift, causing a systematic error. Such an effect is further described by the phenomenon of negative-bias temperature instability (NBTI) [12].

Recent ICs needs to meet industrial requirements, hence the circuit topologies need to be robust against temperature variation in a wide range, at least from −20 °C to 85 °C. Such

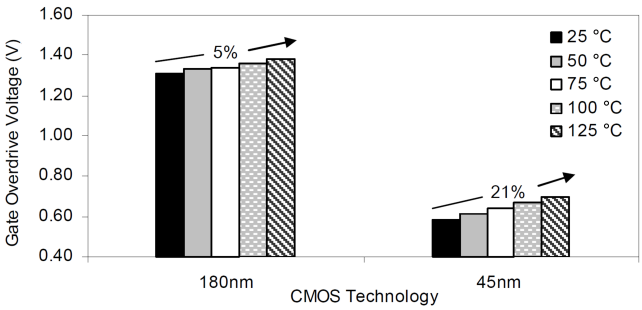

Fig. 3. The variation of the transistor overdrive voltage with temperature for two technology nodes [13].

variations cause substantial shift of the semiconductor structures electric characteristics. Thus, it obviously results in another deviation and systematic error in IC electric parameters.

Advanced integrated systems impose challenging demands on IC power consumption. Since the threshold voltage does not scale consistently with the supply voltage, the V_{DD}/V_{TH} ratio has decreased from approximately 3 for 800 nm technology node to level of 2 for 45 nm technology node [13]. Moreover, the voltage headroom problem get worse with temperature. As can be observed from Fig. 3, the temperature sensitivity of the transistor overdrive voltage in 45 nm technology is higher than the one in 180 nm node [13].

Additionally, similar tendency has been presented in terms of the MOS transistor drain current (I_D) in [14]. It was shown that the I_D temperature sensitivity increases in the inverse proportion with V_{DD}. Also, the I_D sensitivity to V_{DD} increases dramatically below the supply voltage value of approx. 500 mV. However, this change is less significant with technology downscale as the temperature sensitivity.

2.4 Supply Voltage Scaling

Contemporary trends in CMOS technologies include the device downscaling and shrinking the gate-oxide thickness down to the order of few nanometers. This leads to low breakdown voltages, and therefore, the supply voltage has to be reduced to ensure the circuit correct operation and the reliability. Reducing the device size and technology resolution also leads to increased density of components on chip. Since the substrate can dissipate only certain amount of heat per area, the power consumption has to be reduced too. On the other hand, the decrease of the MOS transistor threshold voltage is less significant in comparison to the supply voltage scaling over the years, which results in worse on/off characteristics and lower voltage swing.

The minimum V_{DD} of a CMOS circuit is limited by the value given by a sum of transistor turn-on voltage V_{GS} and the required voltage swing. For an NMOS device in a standard 130 nm CMOS process, $V_{TH} \approx 300$ mV is quite typical value to achieve saturation in the strong inversion region. Subsequently, when two or more NMOS transistors are stacked into cascode, there is low or no headroom left if using low supply voltages ($V_{DD} \leq 1$ V).

Multi-threshold process or BiCMOS technology can be used to achieve better performance but at the cost of higher fabrication expenses. However, advanced techniques for IC design in a standard CMOS process have been developed to compete these technologies. Nevertheless, IC design becomes rather difficult when it comes to low-voltage and low-power operation. On the other side, to achieve comparable gain of simple stages in comparison to cascode structures, it is possible to connect multiple simple stages in series (into cascade). However, multi-gain stage topologies may represent a stability problem due to the location of their dominant poles. Subsequently, clever compensation techniques has to be used to ensure stability of circuits.

Another problem in ULV IC design is degradation of the dynamic range. Dynamic range is ratio between the maximum voltage swing (or supply voltage) and noise floor. Since noise is relatively constant, lowering the power supply voltage leads to the dynamic range degradation.

2.5 Mismatching

The operation of high performance ICs strongly depends on the circuit element layout matching and differential paths matching. Therefore, any random or systematic deviations invoked by effects described above actually cause mismatch, which consequently decreases the production yield or/and the IC reliability. As an example of undesired circuit parameters caused by mismatching, the input offset voltage of an operational amplifier can be given. This parameter is of the significant concern in the amplifier design, as it is tightly related to degradation of other AC or DC amplifier specifications. The situation get even worse for low-voltage conditions. Other important parameters that are degraded due to both the mismatch in nanotechnologies and low-power restrictions, include common-mode rejection ratio and power supply rejection ratio. For this reason, appropriate layout techniques have to be employed in order to reduce the mismatch of all devices working with a low power supply value.

3. ULV Design Techniques

Generally, very common and useful approach in ULV IC design is using the differential or balanced structures thanks to their high values of PSRR and CMRR, higher voltage swing and lower distortion.

There have been several design techniques developed for ULV and low-power analog ICs. The most used ones include:

- Floating-gate MOS transistors
- Self-cascode topologies
- Level shifters
- MOS transistors operating in sub-threshold region
- Bulk-driven MOS transistors
- Dynamic-threshold MOS transistors

3.1 Floating-gate MOS Transistor

Floating-gate MOS (FGMOS) transistor is similar to the conventional MOS transistor. The difference is in the isolated floating-gate (FG) with no resistive connections. Secondary gates (inputs) are then deposited above, which are connected to FG only through capacitive coupling, since the FG is completely surrounding with high resistive material (usually SiO_2) [15].

Floating-gate voltage V_{FG} is not controlled directly but through the input gates with capacitive coupling. V_{FG} can be expressed as

$$V_{\mathrm{FG}} = \frac{Q_{\mathrm{FG}} + C_{\mathrm{FG,D}}V_D + C_{\mathrm{FG,S}}V_S + C_{\mathrm{FG,B}}V_{\mathrm{B}}}{C_\Sigma} + \frac{\sum_{i=1}^{n} C_{\mathrm{Gi}}V_{\mathrm{Gi}}}{C_\Sigma} \quad (5)$$

where Q_{FG} is the static charge on the floating-gate and C_Σ represents the total capacitance seen at the floating-gate, which is given by 6

$$C_\Sigma = C_{\mathrm{FG,D}} + C_{\mathrm{FG,S}} + C_{\mathrm{FG,B}} + \sum_{i=1}^{n} C_{\mathrm{Gi}}. \quad (6)$$

All these capacitances can be observed in the equivalent circuit shown in Fig. 4.

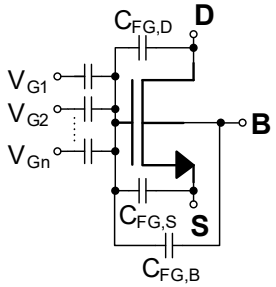

Fig. 4. Input and parasitic capacities of a FGMOS transistor.

Since the electrical isolation between the input gates and floating-gate is almost ideal, the static charge Q_{FG} can remain on the FG for years with negligible variation from the original value. The equivalent threshold voltage of a FGMOS transistor can be controlled by several ways [15]: 1) Ultra-violet light, which can cause the temporary conductivity of the isolation layer, 2) Injection of hot electrons (it requires rather big programming currents), 3) Fowler-Nordheim tunnelling (it requires relatively high programming voltages).

3.2 Self-cascode Structures

In ULV conditions, regular cascode structures are avoided as their use decreases the output signal swing. The self-cascode (Fig. 5) is a two-transistor structure, which can be treated as a single transistor. Gates of both transistors are driven by a common input signal [16]. The self-cascode technique offers higher output impedance and reduces the effect of Miller capacitance on the transistor gates. Moreover, this structure creates higher voltage headroom for signal processing.

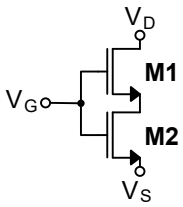

Fig. 5. The self-cascode structure.

The lower (upper) transistor M2 (M1) operates out of saturation (in saturation). If both transistors have similar aspect ratio (W/L), M2 will operate in the linear region and M1 will operate in saturation. In such a case, the self-cascode works like a common-source stage with higher voltage gain. On the other hand, for $(W/L)_1 >> (W/L)_2$, such a circuit behaves like a single MOS transistor operating in the saturation region with rather high gain and significantly lower influence of the channel length modulation. The output resistance r_{out} of this topology is approximately proportional to $(W/L)_1/(W/L)_2$ ratio, and the saturation voltage $V_{DS(sat)} = V_{GS} - V_{TH}$ is roughly comparable to the conventional MOS transistor. The basic principle of this technique is in different threshold voltages of the transistors (i.e. $V_{TH1} \neq V_{TH2}$), which is not available in a standard low-cost CMOS process [16].

3.3 Voltage Level Shifters

Dynamic level shifters represent also a potential solution for circuits with low-voltage input signals. This technique usually uses resistors for shifting the input common-mode voltage to the operation region of input differential transistor pair. Thus, the input transistor pair keeps sufficient transconductance g_m in comparison to the other low-voltage design techniques [17]. Other approach uses a single-supply level shifters for LP applications. Such shifters do not suffer from delay variation (due to different current driving capabilities of transistors), high power consumption and failures at low supply voltage V_{DDL}, compared to the conventional dual-supply equivalents. Single-supply level shifters have advantages over the dual-supply ones in terms of pin count, congestion in routing and the overall cost of the system. Another benefit of the single-supply lever shifters is flexible placement and routing in physical design [18].

3.4 MOS Transistors in Sub-threshold Region

Operating region of the MOS transistor becomes one of the most important aspects for ULV analog IC design [19]. The inversion region of the MOS device is defined by the inversion coefficient ic expressed by

$$ic = \frac{I_D}{I_0(W/L)} = \frac{I_D}{2\mu C_{ox} U_T^2 (W/L)} \tag{7}$$

where I_D is the transistor drain current, I_0 is the technological current, μ is the charge-carrier mobility, C_{ox} is capacitance of the gate-oxide and U_T is the thermal voltage.

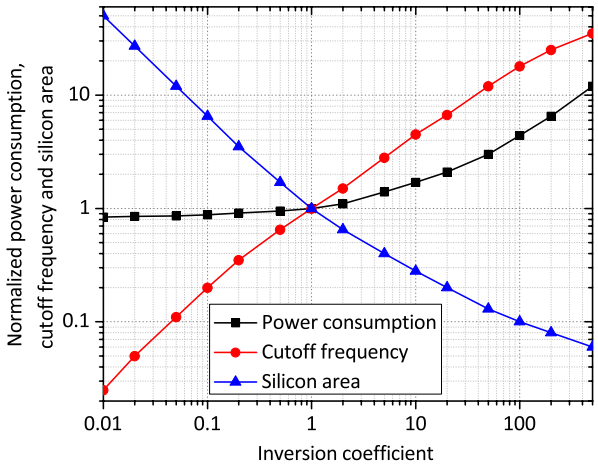

Fig. 6. Normalized power consumption, cut-off frequency and area vs. the inversion coefficient [20].

MOS transistor operating in strong (weak) inversion region has good (bad) frequency response, small (large) chip area and high (low) power consumption. Extreme cases of the strong or weak inversion regions do not provide good trade-off between these variables. The solution could be to use the moderate inversion region. MOS transistor operates in strong (weak) inversion for $ic > 10$ ($ic < 0.1$). Everything in between belongs to the moderate inversion with center in $ic = 1$ (when $I_D = I_0$), in logarithmic scale. Figure 6 shows the relation between the normalized speed, the power consumption and chip area [20].

g_m/I_D approach – A conventional MOS transistor simulation models use different equations for the weak and strong inversion regions. The transition moderate inversion is often described using difficult equation, and it is impossible to avoid significant inaccuracies and discontinuities. Therefore, a new design approach using parameter g_m/I_D is increasingly used [21]. The advantage of this approach is that MOS transistor sizing rules for IC design are defined easily. Such approach can be used for any inversion region thanks to the "one-equation" transistor model. Relation between g_m/I_D and the inversion coefficient ic (Fig. 4) became fundamental for analog IC design in submicron and nanoscale technologies. Parameter g_m/I_D suggests the operation region of a MOS transistor and, more importantly, g_m/I_D does not change across different technologies.

3.5 Bulk-driven MOS Transistors

Drain current I_D of a conventionally connected MOS transistor is usually controlled by the gate-source voltage V_{GS}. In the bulk-driven (BD) design technique, the bulk electrode of the MOS transistor is used as a signal input to modulate drain current (Fig. 7) [22].

Using bulk-source voltage V_{BS} instead of V_{GS} may introduce unwanted body transconductance g_{mb} [23], which is 3–4 times lower than the gate transconductance g_m. The body transconductance g_{mb} is a small-signal parameter of the MOS transistor and it can be expressed as

Technique	GBW	Supply voltage	Power consumption	Technology
FGMOS	Medium	$< VTN + \|VTP\|$	High	2x Polysilicon
Self-cascode	Medium	$< VTN + \|VTP\|$	Medium	Multi-threshold
Bulk-driven	Low	$< VTN + \|VTP\|$	Low	Standard (triple-well) [
Dynamic-threshold	Medium	$< VTN + \|VTP\|$	Low	Standard (triple-well)
Sub-threshold	Low	$< VTN + \|VTP\|$	Low	Standard
Level shifters	High	$< VTN + \|VTP\|$	Medium	Standard

Tab. 1. Comparison of LV design techniques in terms of main parameters.

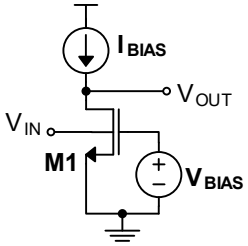

Fig. 7. Schematic of a bulk-driven MOS transistor.

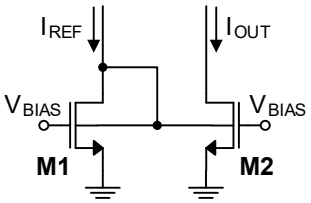

Fig. 8. Simple bulk-driven current mirror.

$$g_{mb} = \frac{\partial i_{\mathrm{d}}}{\partial v_{\mathrm{BS}}} = \frac{\gamma g_m}{2\sqrt{-2\phi_{\mathrm{F}} - V_{\mathrm{BS}}}} \tag{8}$$

where ϕ_{F} is the Fermi potential and γ is the substrate coefficient. Using g_{mb} instead of g_m also leads to lower gain band-width and worse frequency response. Bulk-driven approach increases the input capacitance and input noise. There is also susceptibility to turning on an unwanted latch-up effect in this approach. Nevertheless, clever physical layout by following the specific layout rules can prevent the circuit against latch-up.

On the other side, the BD technique leads to a significantly reduced need to overcome the threshold voltage at the MOS transistor input. This increases the voltage headroom and makes the technique very useful for ULV analog IC design. Moreover, the main advantage of this technique is the compatibility with a standard CMOS process, hence there is no need to change the structure of the conventional MOS transistor [20]. BD design technique can be easily applied to different analog IC building blocks, such as current mirrors [24] or differential pairs [25]. For example, a simple current mirror designed using BD approach is shown in Fig. 8, where bulks of transistors M1 and M2 in both branches are tight together and gates are connected to the bias voltage V_{BIAS}. The input current brought into the input branch creates the voltage V_{BS} between bulks and sources of both transistors.

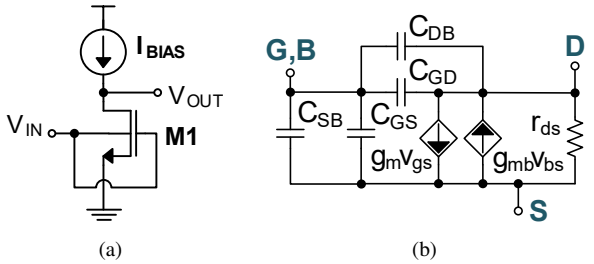

Fig. 9. DTMOS transistor: (a) schematics; (b) equivalent circuit.

3.6 Dynamic-threshold MOS Transistors

Dynamic-threshold (DT) MOS transistors are derived from the BD technique with only a simple difference in the gate biasing conditions. DT transistor has gate and bulk electrodes tight together and biasing is realized dynamically with the input signal swing, which leads to a dynamically reduced value of the threshold voltage V_{TH}. Thanks to the dynamic biasing conditions, the potential of the conductive channel is controlled by both the gate and bulk at the same time, which results in a high overall transconductance $g_m + g_{mb}$ and faster current transfer. Schematic and small-signal equivalent circuit of the DT MOS transistor is depicted in Fig. 9(a) and Fig. 9(b), respectively [26].

Similarly to the BD technique, by applying the DT design technique to basic analog IC building blocks and widely used topologies, DT equivalents can be obtained.

3.7 Summary of ULV Design Techniques

Generally, the LV (ULV) design techniques described above have certain performance limitations such as gain bandwidth (GBW) degradation, increased input noise, increased input impedance or decreased overall transconductance. Main characteristics of the analyzed design techniques are summarized and compared in Tab. 1 [27].

Taking into account the feasibility of particular LV design techniques in different technologies, it is advantageous to use techniques employing MOS transistors operating in the sub-threshold region, such as BD MOS transistors and DT MOS transistors, because there is no need for modification of a standard CMOS process. Additionally, with those two LV techniques, also low power consumption of designed circuits can be achieved.

3.8 Calibration Techniques

In order to overcome nanotechnology drawbacks and compensate the effects of PVT fluctuations on ULV circuits, calibration techniques are employed in analog IC design. Calibration methods are still developing, as new issues appear along with upcoming technology advances. Such methods can be differentiated as static and dynamic ones. Static calibration methods are represented mainly by trimming, where laser or current blown fuses are used [28]. Dynamic calibration methods include, for example, the chopper stabilization [29], auto-zeroing [30] or digital calibration [31]. The latter method will be more deeply described in Session 4.3.1, where digital calibration of a variable gain amplifier was implemented, with a focus on the input offset voltage compensation.

4. Examples of ULV Circuits

4.1 Current Mirrors

Current mirrors (CM) represent one of the most used basic building blocks of analog ICs. Therefore, in our analysis of low-voltage circuit examples, three basic topologies of current mirrors designed using the BD technique are compared to their standard gate-driven equivalents in terms of the output characteristics. Dimensions of transistors were $L = 2\,\mu\text{m}$ and $W = 6\,\mu\text{m}$ for a simple CM (Fig. 8), and $W = 14\,\mu\text{m}$ for the improved Wilson and cascode current mirrors (Fig. 10). Gates of all BD transistors are biased by voltage $V_{\text{BIAS}} = 300\,\text{mV}$. The designed CMs were manufactured in a standard 130 nm CMOS technology and then, the measured parameters were compared to simulation results.

Since the minimum output voltage $V_{\text{MIN}} = V_{\text{DSsat}}$ of the simple CM does not depend on the threshold voltage V_{TH} nor the transconductance, the output resistance $r_{\text{out}} = r_{\text{ds}}$ of both GD and BD simple current mirrors are similar. In other words, a convential gate-driven simple CM is suitable also for use in low-voltage ICS but its main drawback is rather low output resistance (in order of hundreds kΩ). Moreover, even lower output resistance (for similar value of V_{MIN}) was reported for measured results if compared to the simulation results Fig. 11.

The improved Wilson CM can enhance the output resistance of the mirror by adding a negative serial feedback to the circuit. From Fig. 12, one can observe that the BD technique reduces the V_{MIN} voltage from 300 mV to approximately 120 mV, which is similar to the simple CM but with much higher output resistance (in order of MΩ).

In the case of cascode CM (Fig. 13), the minimum output voltage is again significantly reduced to the value about 150 mV for the BD design topology. Measurements of both topologies proved simulated results with only slight inaccuracy observed. Thus, DC biasing conditions had to be slightly modified from 300 mV to 320 mV to achieve the required accuracy of the cascode mirror. More details on the LV current mirror analysis can be found in [32].

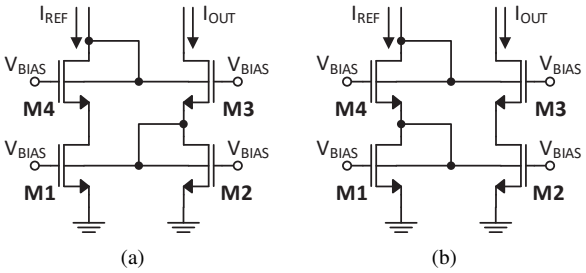

Fig. 10. Schematics of the bulk-driven CMs: (a) improved Wilson; (b) cascode.

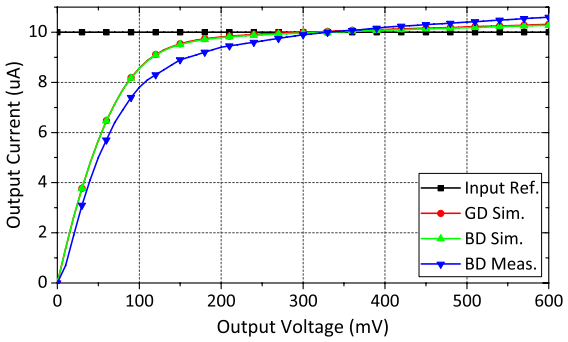

Fig. 11. Output characteristics of a simple CM (using GD and BD design styles).

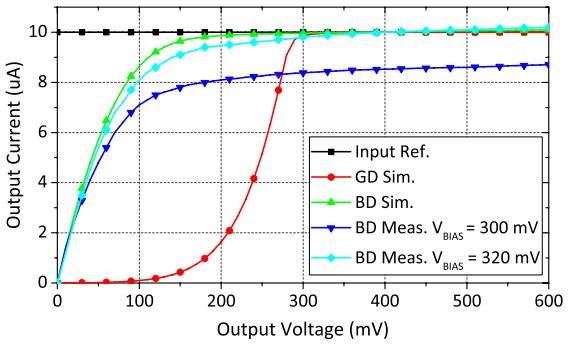

Fig. 12. Comparison of the improved Wilson CMs results.

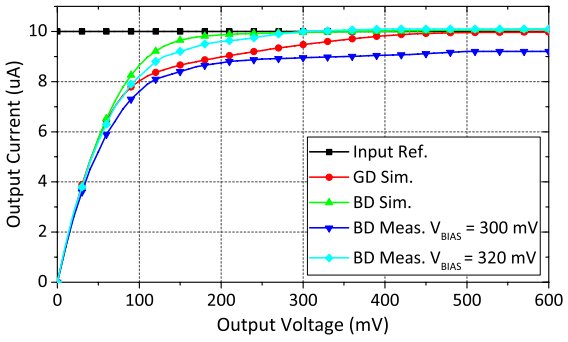

Fig. 13. Output characteristics of the cascode CM.

Presented experimental results have proven that the BD design approach can increase the signal swing by reducing the MOS transistor dependence on the threshold voltage. This can be the key towards LV current mirror design, especially when the cascode CM topologies are used (due to their simplicity and favourable characteristics).

Parameter	[39]	[33]	[34]	[35]	[36]	[37]	[38]
Process	130 nm	65 nm	90 nm	180 nm	500 nm	180 nm	130 nm
V_{DD}	0.4 V	1 – 1.2 V	1 V	1.8 V	1.8 – 5 V	0.3 V	0.2 V
Design style	BD	GD	GD	GD current inp.	GD	BD	GD
Total power	94 nW	60 fJ/decision	40 µW	1.01 mW	40 nA	100 pW	3 fF/decision
Frequency	500 kHz	1 MHz	1 GHz	500 MHz	10 kHz	62.5 kHz	250 kHz
Load	25 pF	-	-	200 fF	-	-	10 fF
Silicon area	410 µm^2	100 µm^2	543.75 µm^2	-	-	-	-
Sim./Meas.	Meas. (25 °C)	Meas. (25 °C)	Meas. (25 °C)	Sim. corners	Meas. (25 °C)	Sim. (25 °C)	Sim. (25 °C)

Tab. 2. Comparison of state-of-the-art ULV comparators.

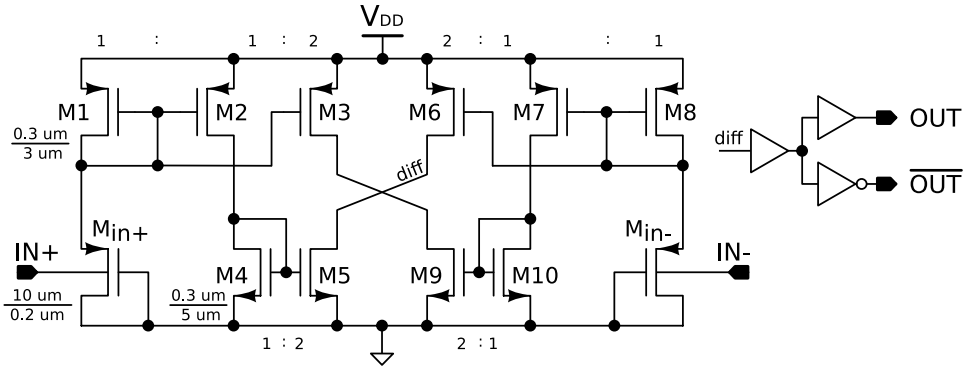

Fig. 14. A non-latched LV rail-to-rail bulk-driven voltage comparator in 130 nm CMOS technology [39].

4.2 Low-voltage Comparators

Several low-voltage comparator designs with the low power consumption have been developed mainly in deep submicron CMOS technologies thanks to fair trade-off between the cost, fabrication process properties, and component parameters. The research and the comparison of state-of-the-art (ultra) low-voltage and low-power comparator designs was carried out. The results of the investigation are summarized in Tab. 2.

A novel low-voltage comparator design that we have proposed in [39] is depicted in Fig.14 (along with the device dimensions). Standard 130 nm CMOS process was selected and the power supply voltage of 400 mV was used. The input stage is comprised of bulk-driven PMOS transistors, which introduces the rail-to-rail input voltage range ability. Again, the real limitation of true rail-to-rail range is the offset voltage. The input voltage modulates the current flowing through the input circuit branch. This current is afterwards mirrored by transistors M1–M5. Set mirroring ratios improve the consumed quiescent current and layout matching of respective devices. The differential voltage is generated in the node called *diff*. Since the analog part is symmetrical, the other half of the circuit works in the identical way. The differential voltage is shaped by serial system of buffers and inverters. The driving capability was set to $f = 500$ kHz at capacitive load of 25 pF. The expected performance and other parameters are discussed in more details in [39].

The measurements performed on the fabricated prototype chip of the comparator (Fig. 14) confirmed correct operation and ability to work with even lower supply voltage value. Measured DC transfer characteristics at room temperature for various reference voltages is depicted in Fig. 15. The experimental measurement data are also compared to simulation results.

One can observe an excellent agreement between both sets of data. The calculated average input offset voltage equals $V_{OS} = 2.29$ mV while the average power consumption

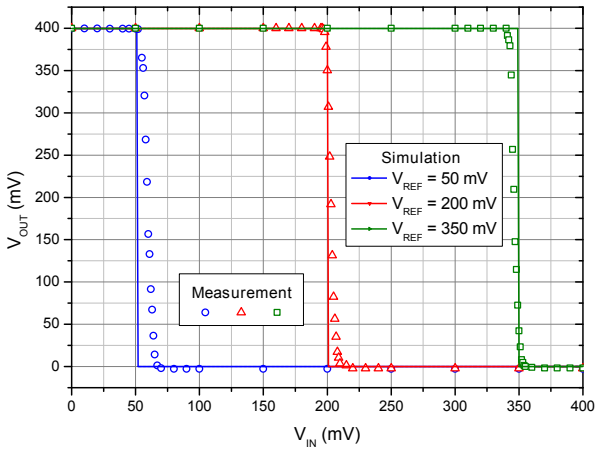

Fig. 15. Comparison of measured and simulated transfer characteristics of the LV comparator proposed in [39].

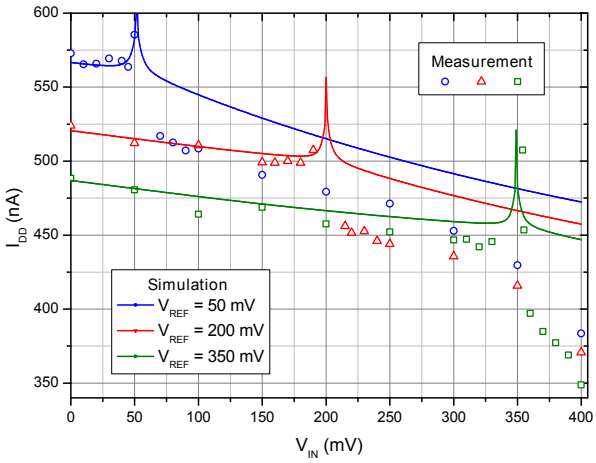

Fig. 16. Comparison of measured and simulated current consumption of the LV comparator proposed in [39].

was calculated at $P = 94\,\text{nW}$. Figure 16 depicts measured current consumption of the proposed comparator along with the simulation results as well. There is an ongoing performance analysis of the proposed rail-to-rail bulk-driven comparator which should be published soon.

4.3 Variable-gain Amplifier

Variable-gain amplifier (VGA) represents a basic building block of many mixed-signal integrated systems. Novel ultra-low voltage VGA circuits, based on the BD approach, were presented in [25], [40], [41]. The general block diagram of the VGA presented in [25], [40] is depicted in Fig. 17. The two-stage VGA circuit is based on a BD differential difference amplifier (DDA). The second stage is composed of a standard common-source amplifier (CSA). Additionally, two common-mode feedback (CMFB) circuits were proposed and used in order to ensure a stable operational point of the first stage as well as the second stage. The developed VGA can reliably work at the supply voltage of 0.6 V. The achieved tuning range is from 20 dB to 47 dB, and the power consumption of about 11 µW was reported. The developed VGA was successfully employed in an automatic gain control (AGC) loop.

Another experimental VGA circuit, designed to work with the supply voltage of 0.4 V with the power consumption of 3.4 µW, was presented in [41], and its block diagram is shown in Fig. 18. This VGA design is based on a pseudo differential difference amplifier (PDDA), which was designed using the BD technique.

In this ULV amplifier design, a common-mode feedforward (CMFF) circuits was used in order to ensure the bias voltage for the input BD transistors [41]. Besides, a CMFB circuit for the stabilization of the operational point was employed here as well. Since in the PDDA topology, the tail current source is missing, the CMFF circuit is used to improve the common-ode rejection ratio (CMRR) of the VGA. The tuning range of the amplifier presented in [41] is from 0 dB to 18 dB for the control voltage value from 0 V to 0.33 V, respectively.

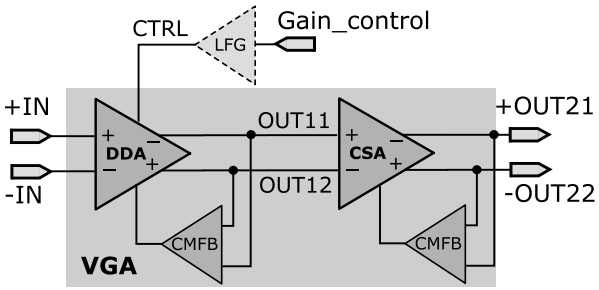

Fig. 17. General block diagram of the VGA presented in [40], [25].

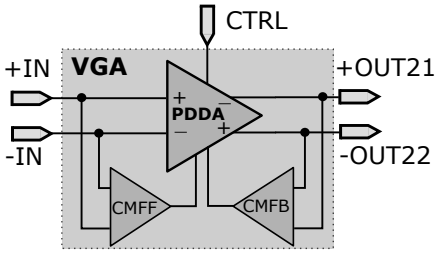

Fig. 18. Block diagram of the VGA presented in [41].

The main parameters of the ultra-low voltage VGAs designed using the BD technique are summarized and compared in Tab. 3.

Parameter	**[42]**	**[25, 40]**	**[41]**
Process	180 nm	130 nm	130 nm
Design style	BD	BD	BD
Total power	0.2 mW	0.12 µW	3.45 µW
V_{DD}	0.8 V	0.6 V	0.4 V
Tuning range [dB]	17 (L-in-dB)	14 (L-in-dB)	8 (L-in-dB)
Gain [dB]	−10.5 ÷ 6.5	20 ÷ 47	0 ÷ 18
BW [MHz]	42 ÷ 195	0.28 ÷ 0.29	0.73
Distortion	THD: 0.32% @ in : −16.2 dBV, out : −25 dBV	THD < −30 dB@1 mV	N/A
Sim./Meas.	Sim. (typ)	Sim. (PV)	Sim. (PV)

Tab. 3. Main parameters of the presented VGA designs.

4.3.1 Digital Calibration of the VGA

A digital calibration technique, targeting the compensation of the VGA input voltage offset ($V_{\text{IN-OFF}}$), was employed and implemented within an experimental chip. The block diagram of the calibration system is depicted in Fig. 19. The whole system can be divided in three main functional parts: the calibrated device, compensation circuitry and the control logic. The VGA circuit was used as the calibrated device.

As already mentioned above, the VGA is a low-voltage fully differential difference amplifier. Its gain can be varied up to 47 dB and the GBW of 15.5 MHz is reached. Thus, it is crucial to optimally adjust compensation circuitry for a specific range of $V_{\text{IN-OFF}}$ range. The residual offset of the proposed calibration method is directly proportional to the maximum offset value which this method is able to compensate. Specifically, this is represented by the DAC (digital-to-

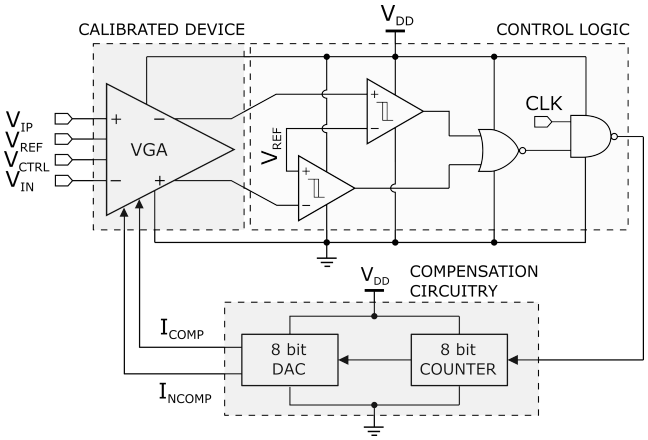

Fig. 19. The block diagram of the calibration system for VGA.

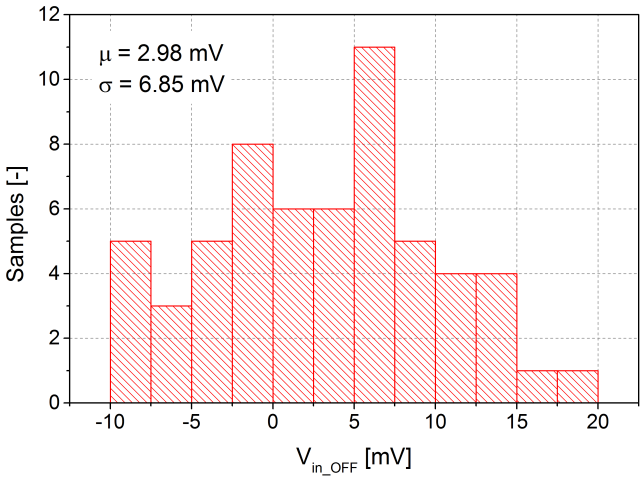

Fig. 20. The statistical distribution of $V_{\text{IN-OFF}}$ measurement over 60 samples.

analog converter) specifications, analog response to a lowest significant bit (a_{LSB}), and the full scale. Therefore, it was essential to determine the statistical distribution of $V_{\text{IN-OFF}}$ over significant number of samples. Fig. 20 presents variation of $V_{\text{IN-OFF}}$ measurement results obtained from measurement of naked prototyped chips. The statistical distribution consisting of 60 samples reaches the mean value of 2.98 mV and the standard deviation of 6.85 mV. The DAC full scale was adjusted to the $V_{\text{IN-OFF}}$ results in Fig. 20. Considering the 3σ range of distribution, the calibration circuit was optimized to compensate the $V_{\text{IN-OFF}}$ of ± 20 mV.

The main part of compensation circuitry is a 8-bit DAC with the differential output, which is connected to the VGA so that it can modify the current-voltage conditions in both branches of the amplifier. The DACs input code is set by an 8-bit counter. Initially, the input code is 0 and corresponding differential outputs of the DAC are 0 (the minimum output current) and the full scale (the maximum output current). The output offset voltage of the VGA ($V_{\text{OUT-OFF}}$) is, in this case, near the supply voltage level, as the amplifier is imbalanced. Then, the counter increases the input code for DAC. The VGA current-voltage conditions are adjusted accordingly to the DAC outputs, which are gradually changing in the opposite direction (until they swap their initial states - 0 and the full scale). This process is continuously monitored by the control logic block, which terminates it immediately after $V_{\text{OUT-OFF}}$ reaches the lowest possible value. After that, the DAC continually supplies the last set analog outputs, and the calibrated VGA can emerge its normal operation.

The control logic is composed of two comparators with hysteresis. The VGA outputs are connected to one of the comparators inputs. The second input of both comparators is fed with the reference voltage V_{REF}, which represents the ideal VGA output common mode. As explained previously, the DACs outputs starts to change as the counter begins to increase its output code. One of them is stepping down from the full scale and the other is stepping up from 0. Initially, both comparators are in low state at the output. The following NOR gate output is kept in high state. In this way, one of the subsequent NAND gate inputs is at high logic level, allowing the gate to be transparent for the other input. This is formed by the clock signal (CLK), which is then fed to the counter. In this manner, the DAC conversion proceeds and $V_{\text{IN-OFF}}$ is reduced.

After one of VGA outputs exceeds the V_{REF} value, the corresponding comparator flips its output to high level, and the NOR gate flips its output to low level. In this way, the CLK signal for compensation circuitry is stopped and the counter and DAC maintain their actual output values. If the calibration is terminated, control logic continues to sense the VGA output and it starts the whole cycle again when $V_{\text{IN-OFF}}$ exceed the given value. Therefore, this method is able to eliminate also the temperature and ageing drifts of the offset.

4.4 LV Charge Pump for Self-powered Systems

As reviewed and summarized exhaustively in rather recent publication [43], ULV CMOS based charged pumps (CP) are widely used within energy-autonomous or also called self-powered electronic systems. The most dominant advantage of CPs – fully on-chip integration capability – can be very challenging in terms of finding compromise between performance and acceptable area consumption, especially in ULV applications. Thus, this subsection presents the design of a dynamic threshold charge pump using a novel driver developed for ULV applications.

Our research was focused on pushing the minimum start–up voltage to its lower possible limit by improving the driving capability of the inverter-based driver and designing a boosting circuit for the CP cell itself as the future step. In start-up process, the driver is usually fed by the output voltage drawn from an energy harvester. Therefore, its driving capability strongly depends on it due to higher switch–on *RC* constant. Also lowering *RC* time constant results in higher switching frequency opportunity in ultra–low supply voltage conditions. Consequently, the enhancement of V_{GS} enables the use of much smaller transistors, then strongly reduces transistor capacitances and also switching losses.

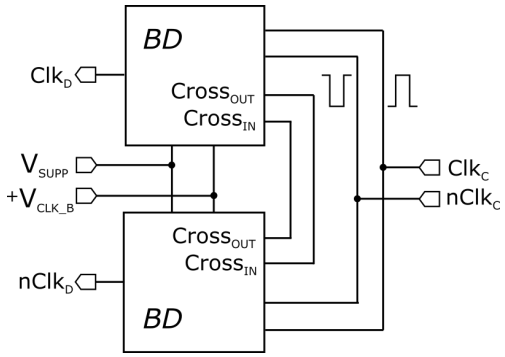

Fig. 21. Block diagram of the cross-connected driver [45].

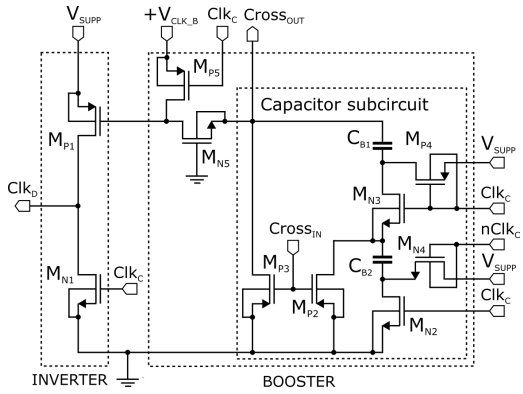

Fig. 22. Transistor level schematic of the proposed driver [45].

To improve the reliable start–up and operation conditions of the charge pump, the novel boosted driver for pull–up (PMOS) transistor has been proposed (Fig.21 and 22). The initial goal was to ensure the reliable function of the CP from the minimum possible value of the supply voltage. The boosting technique extends the range of driving voltage of M_{P1} transistor to $\approx -2V_{\mathrm{SUPP}} \div V_{\mathrm{SUPP}}$ and reduces its ON resistance. The driver generates a non-overlapping outputs under the condition of non-overlapping control signals (Clk_{c} and $nClk_{\mathrm{c}}$). Design utilizes only two capacitors and charging is accomplished directly by the supply voltage, compared to three capacitors (two capacitors version is also available) with lower driving range of $\approx -V_{\mathrm{SUPP}} \div V_{\mathrm{SUPP}}$ and charging supported by the clock signal presented in [46]. More details together with the propagation delay measurement of the proposed driver can be found in [45] and [47] respectively.

To verify the performance of the proposed driver in ULV systems, the driver has been implemented as part of a CP-based energy harvesting control loop, as shown in Fig.23. Conventional On/Off regulation scheme has been chosen to maximize the charge pump efficiency. This scheme is based on a low-power BD rail-to-rail comparator [39] that blocks or passes clock signal to the driver. The switching frequency f_{CLK} and size of the bootstrap capacitors and switching transistors have been designed as a trade–off between the reliable function of the driver from 200 mV supply voltage in all corners and the temperatures range from −20°C to 85 °C. Taking this into account, the bootstrap capacitors of $\approx 4 \times 15$ pF have been chosen with the expected charging capability up to 1 MHz.

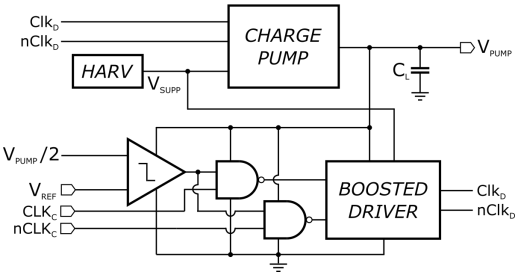

Fig. 23. The block diagram of the proposed charge pump system [45].

The charge pump consist of a three-stage dynamic threshold cross-coupled CP structure, where the number of stages was limited by available chip area, which limits the voltage conversion to $2-3\times$ [44]. This restriction can be however, avoided by cascading a multiple chip due to identical topology of the individual CP cells. The cross-copupled CP belongs to popular, dual-branch linear types of CPs, having several advantages: *a*) good compromise between the power consumption and voltage conversion efficiency, *b*) compensated dual-branch topology reduces the output ripples and improves the pumping efficiency due to a flying capacitor size reduction resulting in faster charge transferring, *c*) reduction of loss between the last stage and the output capacitor since one of the two branches always provides current to keep the output voltage stable, *d*) lower reverse charge sharing, *e*) two phase non-overlapping clock can ensure sufficient timing of the switching process, *f*) the channel charge injection is eliminated due to complementary switching of adjacent NMOS/PMOS transistors. In spite of the above mentioned advantages, the application of the original cross-coupled topology is not suitable for ULV systems due to missing bootstrap techniques, and dynamic threshold method itself seems to be insufficient (see comparison to the other solutions in Tab. 4). In addition, the cross-coupled CP suffers from the reduced V_{GS} in the last stage, which is even more pronounced in regulated systems.

The proposed CP system was fabricated in a triple–well UMC 130 nm CMOS technology, where the CP core, control logic and the driver occupy area of $\approx$ 0.122 mm^2 (Fig. 24). Early characterization process of the fabricated chip was primary aimed at investigating the reliable start and achieved parameters has been compared to other works [47]. The measurements proven that the control unit and the driver can work in the case of hot–start from the minimum supply voltage of 126 mV at 160 kHz. Regulated voltage of 379 mV was achieved where a regulatory deviation was caused by comparable impedances of electrostatic discharge (ESD) diodes with resistor based voltage divider. For more details of measurement setup please refers the [47]. The further measurements will be dedicated to characterization of the proposed CP systems in terms of others important parameters such as the maximum load capabilities, voltage conversion and power efficiency, etc. Table 4 summarizes the achieved parameters and compares the developed CP to other works.

	[45], [47]	[48]	[49]	[46]	[50]	[51]	[52]	[53]
CMOS process [nm]	130	130	180	55	130	65	65	180
Sim/Meas	*sim & meas*	*meas*	*meas*	*meas*	*meas*	*meas*	*meas*	*meas*
Year	2017	2015	2014	2017	2011	2012	2010	2016
Number of Stage	3	3	2	12	3	5 + 10	3	2 + 2
Reg/Unreg	*by voltage reference*	*unreg*	*by MPPT*	*unreg*	*by voltage reference*	*unreg*	*unreg*	*by MPPT*
$V_{IN,MIN}$ / $V_{START,MIN}$ [mV]	V_{IN} = 200/ V_{OUT} = 126 *(meas, hot-start)*	150 *(cold-start)*	210 *(cold-start)*	200 *(cold-start)*	270 *(unreg,cold-start)*, 400 *(reg,cold-start)*	120 *(cold-start)*	180 *(cold-start)*	350 *(cold-start)*
V_{OUT} [mV]	407 (sim), 379 ($meas$) @ V_{IN} = 0.2 V, R_L = 27 kΩ	619 @ V_{IN} = 0.18 V, $R_L \rightarrow \infty$	600 – 1800 @ NA	1900 @ V_{IN} = 0.22 V, P_{OUT} = 10.45 µW	1400 @ V_{IN} = 0.45 V	1300 @ V_{IN} = 0.16 V, P_{OUT} = 2 µW	600 @ V_{IN} = 0.18 V, I_{OUT} = 2.5 µA	860 – 1800, 2500 – 5200 @ $R_L \rightarrow \infty$
P_{OUT} [µW]	6.5 (sim) @ V_{IN} = 0.2 V, V_{OUT} = 0.407 V	10.5 @ V_{IN} = 0.18 V, V_{OUT} = 0.5 V	1000 *(power throughput)* @ NA	10.45 @ V_{IN} = 0.22 V, V_{OUT} = 1.9 V	11 @ V_{IN} = 0.45 V	10 @ V_{IN} = 0.16 V, V_{OUT} = 0.9 V	4.5 @ V_{IN} = 0.18 V, V_{OUT} = 0.5 V	396 @ V_{OUT} = 1.41 V
I_{OUT} [µA]	16 (sim) @ V_{IN} = 0.2 V, V_{OUT} = 0.407 V	21 @ V_{IN} = 0.18 V, V_{OUT} = 0.5 V	NA	6 @ V_{IN} = 0.22 V, V_{OUT} = 1.9 V	5 @ V_{IN} = 0.45 V	11 @ V_{IN} = 0.16 V, V_{OUT} = 0.9 V	9 @ V_{IN} = 0.18 V, V_{OUT} = 0.5 V	NA
(Power:) η_{CONV}/ $\eta_{E\text{-}E}$ [%]	29 (sim)/NA, @ V_{IN} = 0.2 V, V_{OUT} = 0.407 V	34/NA,@ V_{IN} = 0.18 V, V_{OUT} = 0.5 V	NA/73.6 @ V_{OUT} = 1.46 V, P_{OUT} = 348 µW	37.4/NA @, V_{IN} = 0.22 V, V_{OUT} = 1.9 V	58/NA @ V_{IN} = 0.45 V, P_{OUT} = 11 µW	38.8/NA @, V_{IN} = 0.120 V, V_{OUT} = 0.77 V	NA	NA/75.8 @ V_{OUT} = 1.41 V, P_{OUT} = 396 µW
f_{CLK} [MHz]	1 (sim), 0.160 ($meas$)	0.250	*set by MPPT*	2.15	0.8	1($start-up$), 20($operation$)	10	*set by MPPT*
Start-up Technique	*mechanical switch (hot-start)*	*none*	*free-run*	*none*	*none*	*free-run*	*none*	*free-run*
Area [mm^2]	0.122	0.066	0.94	0.74	0.42	0.783	0.3	1.75
Integration	*partial*	*partial*	*fully*	*fully*	*fully*	*fully*	*fully*	*fully*
MPPT	*no*	*no*	*yes*	*no*	*no*	*no*	*no*	*yes*

Tab. 4. Comparison of capacitive charge pumps (step-up converters) suitable for low-voltage energy harvesters.

4.5 Experimental Chip

Figure 24 shows a microphotography of the developed experimental chip where the presented ULV analog circuit examples are implemented. The experimental chip was designed and implemented in a standard 130 nm CMOS technology and occupies area with dimensions of 1.2 mm × 1.2 mm (1.44 mm^2). The charge pump together with the low-voltage driver together and the comparator are used as self-powered system. We have to note that chip do not contains the integrated clock generator yet and clock signals with desired frequency as well as the reference voltage for the comparator were generated externally. Both variable-gain amplifiers are placed on the bottom of the chip. The BD current mirrors are located in the middle of the chip. The proper layout principle and techniques were employed in order to achieve good matching of all bulk-driven transistors used in the proposed analog circuits.

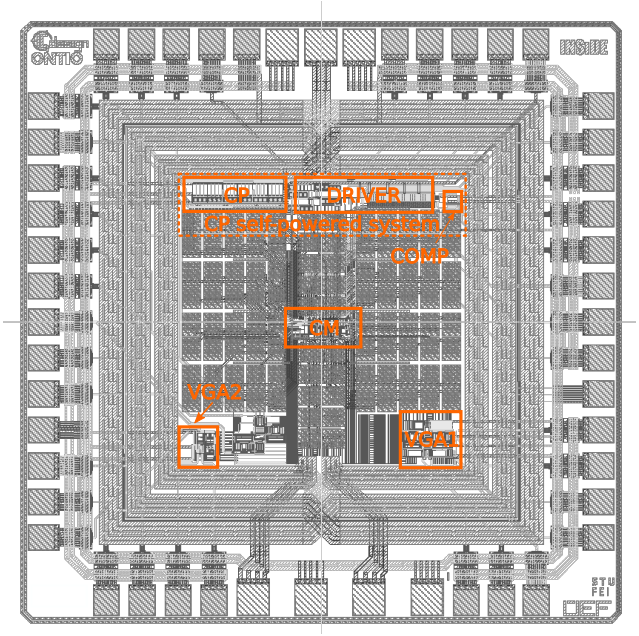

Fig. 24. Microphotography of the fabricated experimental chip.

5. Conclusion

Challenges and problems that have to be solved within the design of ultra low-voltage analog ICs are addressed in this paper. Since the use of standard circuit topologies as well as conventional design techniques is rather limited under the ultra low-voltage conditions, design engineers have to look for new topologies that are robust to PVT variations. As shown in this paper, the bulk-driven design technique can be an effective alternative for ULV analog ICs. Using this technique, the power consumption of analog circuits can be significantly reduced. However, the bulk driven approach can be used properly only for low-frequency applications. Therefore, the development of dedicated design techniques and analog topologies for ULV applications are still needed.

Acknowledgements

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