Binary Weighted DAC with 2-ξ Resistor Ratio

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Abstract. *In this paper we present a new digital analog converter (DAC) design, based on the binary weighted resistor network. The proposed design ensures high conversion accuracy using low precision resistors with ±1%, ±2%, ±5%, ±10% and ±20% resistor tolerance. High accuracy is achieved due to better coverage of the analog domain of the transfer characteristic. In binary weighted converters the imprecision of resistors introduces positive and negative differential nonlinearities (DNL). Positive DNL causes gap in the analog domain of the transfer characteristic and negative DNL causes non-monotonicity. In the proposed solution we change the resistor ratio of the two consecutive DAC branches from 2 to 2-ξ, where ξ is a small positive number. With this change, we intentionally introduce an additional negative DNL in order to entirely avoid the positive gap. Simulation results confirm that even with resistors tolerance of up to ±10%, we can achieve a converter with maximal gap in the transfer characteristic less than or around one LSB.*

Keywords

Binary weighted DAC, conversion accuracy, differential nonlinearity, gap in transfer characteristic, lookup table

1. Introduction

The main challenge with all digital-analog converters (DAC) is to achieve high conversion accuracy, high speed and high resolution. Resistor based DAC architectures, like binary weighted DAC, R/2R DAC, string DAC, etc., are commonly used due to their simple structure, short settling time, and low power consumption and are a good choice for many applications [1].

However, conversion accuracy of the resistor based DAC extremely depends on the precision of the used resistors as well as on the voltage reference stability. From the other side conversion speed mainly depends on the switching delay time [2]. With the laser trimming technology it is possible to improve the converter accuracy [3], but aging and environmental factors decrease linearity and overall accuracy of a converter, and reduce its applicability.

Deviations of the resistor values around the nominal ones cause deviations of the LSB output step. This output deviation is known as differential nonlinearity (DNL). The effects of the DNLs on the transfer characteristic are shown in Fig. 1 and Fig. 2.

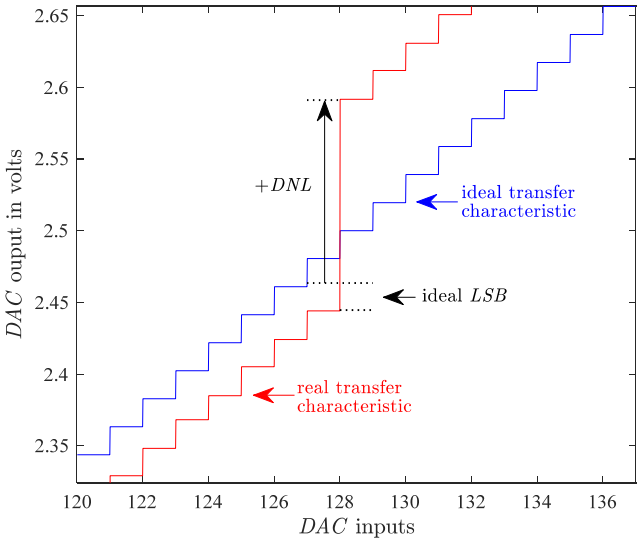

Fig. 1. Positive DNL in the DAC transfer characteristics.

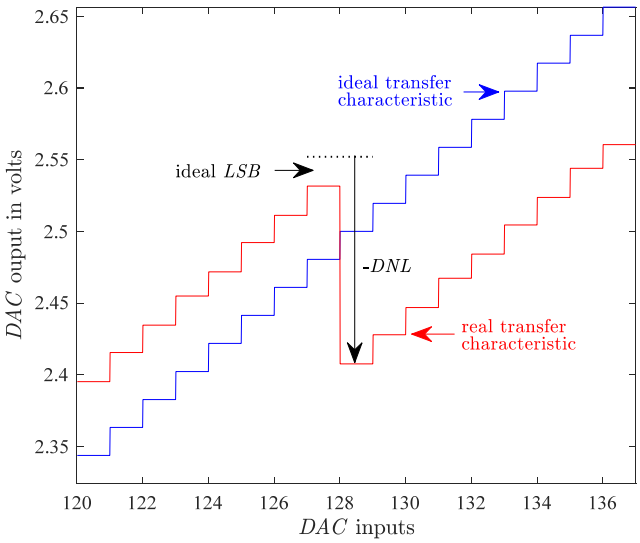

Fig. 2. Negative DNL in the DAC transfer characteristics.

Generally, the most significant bit introduces the largest DNL, while the DNL caused by least significant bits may often be neglected [4], [5].

From Fig. 1 and 2 it can be seen that two types of deviation are possible in the transfer characteristic, positive and negative DNL. Positive DNL can cause gap in the analog domain of transfer characteristic. There is no digital word at the DAC input that can produce a desired analog voltage levels from the gap. Negative DNL, on the other side, makes the transfer characteristics non-monotonic.

The DACs also suffer from many other imperfections such as the integral nonlinearity (INL), gain error, offset error, settling time, and noise. The integral nonlinearity, known as the global nonlinearity, measures the overall or cumulative nonlinearity and represents maximal deviation of the output from the ideal transfer curve. The gain error indicates how well the slope of the DAC transfer function matches the slope of the ideal one. Offset error, often called 'zero-scale' error, indicates how well the DAC transfer function matches the ideal one at a single (start) point. Settling time is one of the most important dynamic DAC imperfections. It is defined by the interval between a command to update DACs output value and the instant when it reaches stationary level (within a specified percentage) [5].

Linearity of the DAC static characteristic is usually described by the differential and integral nonlinearity, gain and offset error. Noise is in general limited to the thermal noise, mainly generated by passive components such as resistors. The gain and offset errors can easily be removed by calibration. The INL and the negative DNL can be alleviated by appropriate calibration procedure as well.

The positive DNL (gaps in the DAC transfer characteristic) becomes an essential parameter in achieving the desired coverage of the analog range. The positive DNLs cannot be subsequently corrected, what mean that the analog values from the gaps remain unreachable. The main goal of this paper is to propose a method for reducing the positive DNLs in the DAC transfer characteristic.

One of the primus DAC architectures is the binary weighed DAC (Fig. 3). Binary-weighted DACs utilize one switch per bit and they first appeared in the 1920s. Since then, this architecture remains popular and forms the backbone for modern precision and high-speed DACs [6].

The main advantages of the binary weighted DAC are based on a small number of resistors and switches, and consequently simple construction, as well as on the short settling time. However, it suffers from poor accuracy because of the large difference in the resistor values. Furthermore, the transfer characteristic of the binary weighted DAC is not inherently monotonic. It may have high positive and negative DNLs. Opposite to it, R/2R DAC conversion network consists of only two different resistors values, with ratio 2:1. The resistors ratio does not depend on the number of bits in the network. However, as compared to the binary weighted DAC it needs twice more resistors and it has longer settling time. Further, the string DAC has

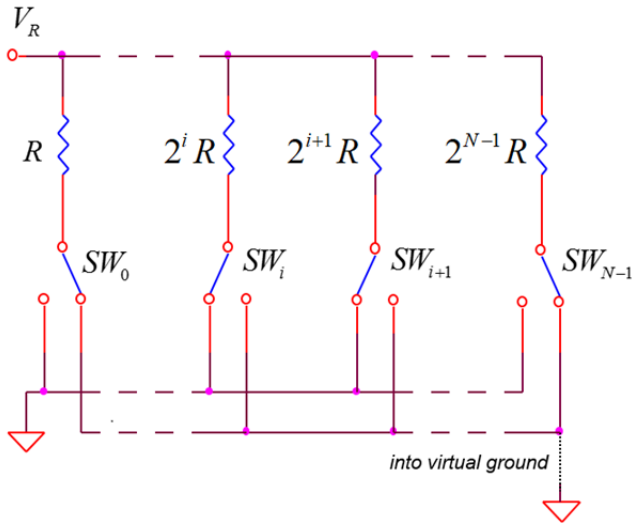

Fig. 3. Topology of a binary weighted DAC.

DAC type	Number of resistors	Number of switches	Settling time	Monotonic
Binary weighted	8	8	Shortest	Not guaranteed
R/2R	16	16	Medium	Not guaranteed
String	256	256	Longer	Not guaranteed
Sigma-delta	2	2	Very long	Yes

Tab. 1. The comparative review of the basic characteristics of the most frequently used 8-bit DAC realization.

an inherently monotonic characteristic, but it suffers from a large number of resistors and switches and much longer settling time [6].

The widely used sigma-delta DAC has a good monotonic characteristic and lower DNL. However, it is very slow [7].

Table 1 shows comparative review of some basic characteristics for the most frequently used 8-bit DAC realizations.

In this paper we present a method that could be used to reduce the positive DNL and such that improve transfer characteristics of the binary weighted DAC. We have already applied a similar method on the R/2R DAC [8, 9, 10]. The interest in this approach and its applicability is confirmed meanwhile by [11–21]. We found that the same benefits can be obtained from the presented approach applied to the binary weighted DAC.

2. Description of the Method

In this method, we propose a modification of the initial resistor values in the binary weighted resistor network from

$$2^k R, \quad k = 0,1,...,N-1 \tag{1}$$

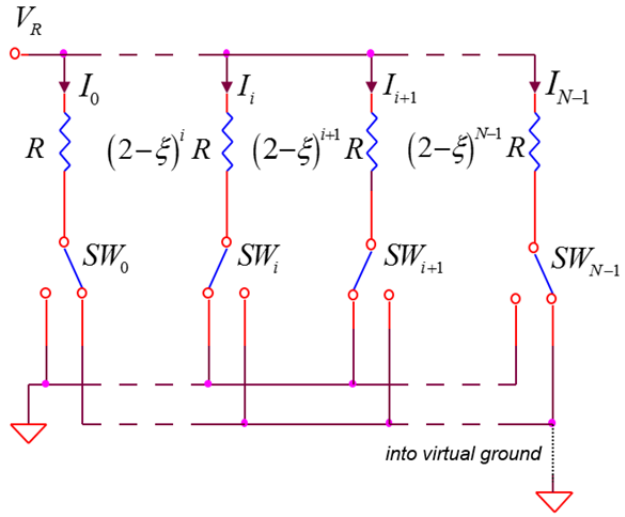

Fig. 4. Topology of a binary weighted DAC with the introduced ξ decrease in the resistors values.

to $$\left(2-\xi\right)^k R, \quad k=0,1,...,N-1, \quad \xi>0 \tag{2}$$

where ξ represents an intentionally introduced decrease in the resistors values and N represents the number of DAC bits (Fig. 4).

Due to the intentionally introduced ξ decrease, the resistance ratio of the two consecutive branches, $i+1$ and i, becomes:

$$\frac{R_{i+1}}{R_i} = 2-\xi < 2 \,. \tag{3}$$

The current ratio is also changed. It is now:

$$\frac{I_i}{I_{i+1}} = 2-\xi < 2 \,. \tag{4}$$

In this way it is possible to ensure that I_i remains lower than $2I_{i+1}$, even in the presence of the resistor value deviations and other imperfections inherent to a real circuit. The purpose of this modification is to avoid positive DNL*s* that induce gaps in DAC analog output and to obtain better coverage of the analog range, with the smallest possible gaps (Fig. 5). This modification increases the negative DNL, i.e. non-monotonicity (Fig. 6). However, an afterward lookup table correction can be used to repair this kind of nonlinearity (Fig. 7).

The lookup table contributes in achieving the best linearity of the DAC output. In this way the precision requirements for the DAC resistors are lowered and there is no need for a laser trimming of the circuit resistors.

The lookup table ensures that for each particular digital input word it is possible to select any of the available analog output values. If all analog output values are sorted, the characteristic as in Fig. 8 is obtained.

From Fig. 8 we can observe that thanks to small positive DNL a better coverage of the analog domain is achieved. However, the lookup table is not a simple sorting. Some values can be repeated twice and/or some others

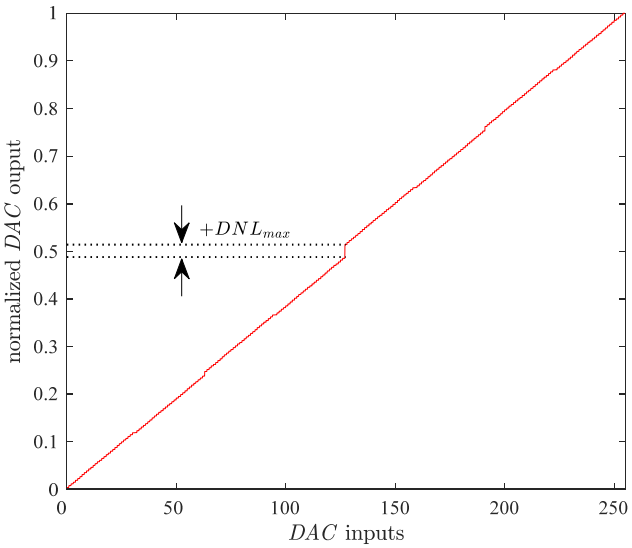

Fig. 5. Gap in the transfer characteristic of a binary weighted circuit without ξ decrease ($\xi = 0$).

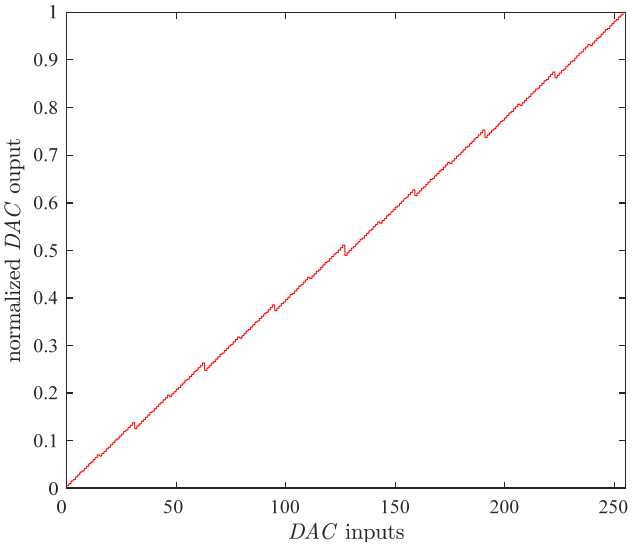

Fig. 6. Negative DNLs in the transfer characteristic of a binary weighted circuit with $\xi = 0.015$.

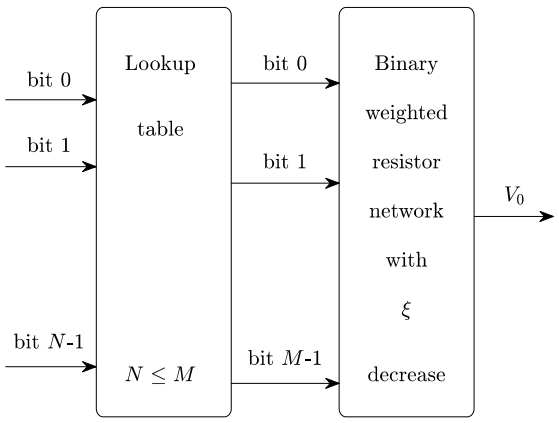

Fig. 7. Lookup table between DAC inputs and resistor networks.

may not appear in the lookup table. The main goal is to achieve a transfer characteristic as close as possible to the ideal one.

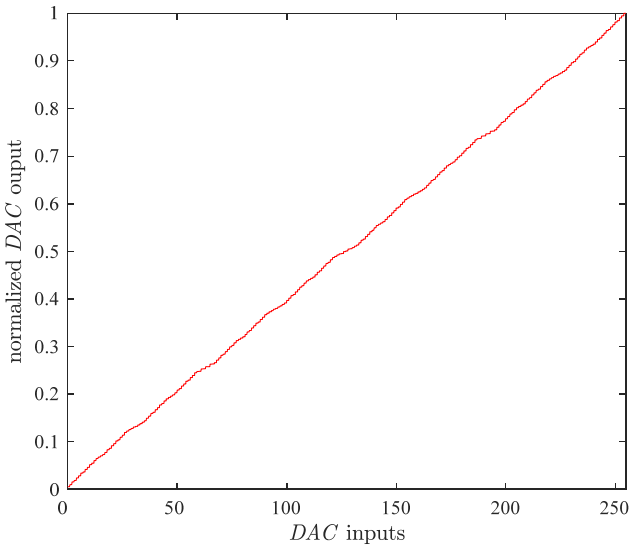

Fig. 8. Sorted values of the graph from Fig. 7.

The maximal positive DNL (MPD) on sorted values shows expected (possible) deviation from the ideal characteristic. Therefore, the target is to get a DAC network with the smallest possible MPD on the sorted values.

Linearity of the DAC transfer characteristic can be further improved if we ensure that the lookup table output has an extra bit relative to the input (Fig. 7). Using this extra bit ($M = N + 1$) we will have twice more values than we intend to implement in the lookup table. This allows a closer approach to the ideal transfer characteristic. In populating of the lookup table it is possible to use the algorithms presented in [8], [10].

In most applications of the proposed DAC, the lookup table will be realized in software instead hardware form. For example, one of such applications is the arbitrary function generations. In this application the first step is the waveform data preparation. This step includes the lookup table transformation. It can be done easily in the software domain because it is not time critical. The second step is the run time waveform generation. It is a simple data transfer to DAC. Removing the lookup table from the DAC hardware significantly simplifies it and shortens its settling time.

The focus of this paper is to describe a method for achieving better coverage of the analog domain of binary weighted DAC, i.e. for reducing maximal positive DNLs (MPD). The method is presented on a binary weighted DAC with the resistor network. However, the same method can be applied in the cases of different hardware implementations, such as the current steering DAC that ensures a short settling time (even under 15 ns) and that is very suitable for an integrated circuits design [22], [23].

3. The Optimal ξ Values

The optimal ξ decrease is the ξ value that ensures the smallest MPD in the transfer characteristic of binary weighted DACs.

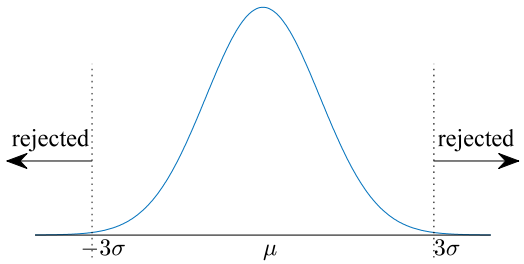

Fig. 9. Statistical security of approximately 99.7%.

An analytical determination of the MPD for a given resistors tolerance and a given ξ, is very complex because of many involved variables. For example, resistors in a binary weighted DAC exhibit random variation from their nominal values, thus affecting the maximal circuit DNL in an unknown, nonlinear manner. From the other side, it is very difficult to describe the nonlinearity, introduced by the sorting function, in an analytic way. For these reasons we used the statistical method for the MPD determination. This method is simple, but in order to produce accurate results, it implies a large number of the DAC circuit samples. For efficient calculation and simulation of such large number of circuits we used MATLAB.

We assumed that dispersion of the resistor values around their nominal ones obey the normal (Gauss) distribution with a standard deviation σ satisfying:

$$3\sigma = tol\ . \tag{5}$$

The range of -3σ to $+3\sigma$ provides statistical confidence of approximately 99.7%. In other words, the rejection ratio in the resistor production, caused by the missed tolerance threshold, will be less than 0.3% (Fig. 9) [24]. With such resistor values constraints in the DAC resistor networks we have calculated the MPD.

Statistical method for finding the MPD was performed for resistor tolerances of 1%, 2%, 5% and 10% in the 8-bit, 9-bit and 10-bit resistor networks. For each resistor tolerance (*tol*) various ξ are implemented, starting from 0 (the case without any decrease), followed by 0.001, 0.0012, 0.0015, 0.0018, 0.0022, 0.0027, 0.0033, 0.0039, etc., until 1, in accordance with E12 series of preferred numbers (international standard IEC 60063) [25]. For each particular combination of resistor tolerance, ξ value, and the number of bits in a resistor network, 100000 realizations of the binary weighted digital-analog circuits are considered. At the end, we used the worst case, with the maximal obtained MPD value.

Statistical results of the performed analyses are presented graphically in the figures that follow.

Figures 10, 11, 12, 13 and 14 present the MPD in LSB as a function of ξ for resistor tolerances ±1%, ±2%, ±5%, ±10% and ±20% respectively, in the 8-bit resistor networks. In these figures, the abscissa contains logarithmic scale of ξ decrease values and the ordinate shows the MPD that correspond to them.

The red dots in the figures denote the MPD for the resistor circuits with $\xi = 0$. These figures show that an in-

crease in ξ value significantly reduces the MPD. For example, from Fig. 12 (results for circuits with resistors tolerance of 5%), it can been seen that the MPD is reduced from the value of 10.36 LSB (for the $\xi = 0$ circuits) to 0.471 LSB (for the $\xi = 0.082$ circuits).

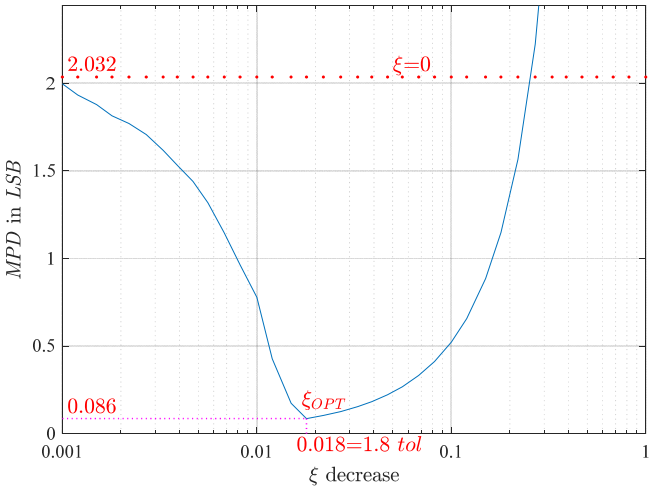

Fig. 10. The MPD as a function of ξ, for resistor tolerances ±1%.

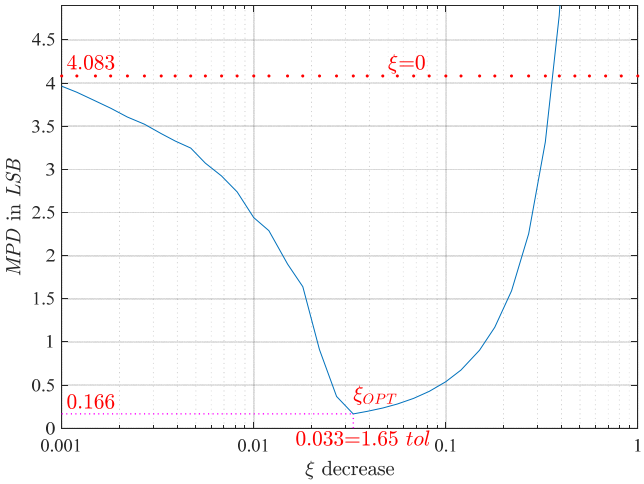

Fig. 11. The maximal +DNL as a function of ξ decrease, for resistor tolerances ±2%.

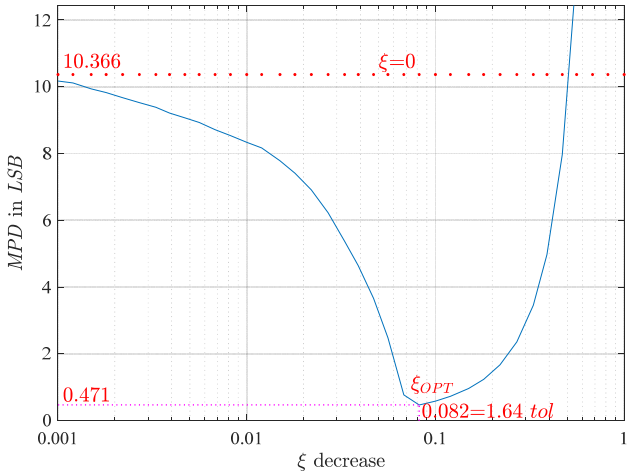

Fig. 12. The maximal +DNL as a function of ξ decrease, for resistor tolerances ±5%.

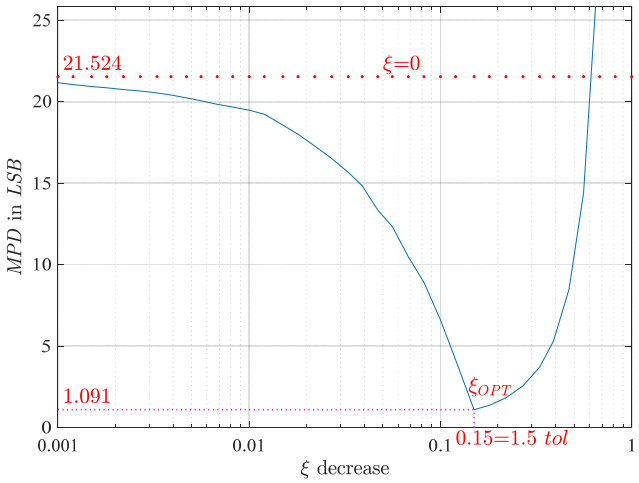

Fig. 13. The maximal +DNL as a function of ξ decrease, for resistor tolerances ±10%.

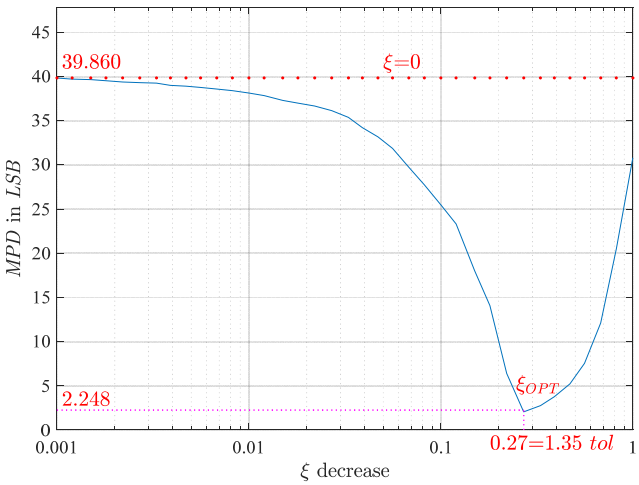

Fig. 14. The maximal +DNL as a function of ξ decrease, for resistor tolerances ±20%.

The MPD is reduced for about 22 times. The shrinking factor (*SF*) is equal to:

$$SF = \frac{+DNL_{\mathrm{MAX}}(\xi = 0)}{+DNL_{\mathrm{MAX}}(\xi_{\mathrm{OPT}} = 0.082)} = 22.008 \cdot \qquad (6)$$

Further increase of the ξ value causes increase in the MPD. Thus, for $\xi = 0.1$, we obtained maximal MPD = 0.52 LSB and for $\xi = 0.12$ MPD = 1.64 LSB. These results are worse than in the case of $\xi = 0.082$ (MPD = 0.471 LSB). It means that a further decrease in the resistor ratio is undesirable.

Similar results, like the ones presented in Figs. 10 to 14, are obtained for the resistor networks with 9 and 10 bits. The MPD as a function of ξ, for resistor tolerances 5%, in the 9-bit and 10-bit resistor networks are shown in Fig. 15 and 16, respectively.

It is obvious that within a prescribed tolerance, the optimal ξ value (ξ_{OPT}) is the one that causes the smallest MPD. Table 2 presents ξ_{OPT} for different resistor tolerances (*tol*), in the 8-bit, 9-bit and 10-bit resistor networks. From the results shown in Tab. 2, we concluded that the optimal ξ decrease value is slightly different for different resistor

tolerances and does not depend on the number of bits in resistor networks

The SF values for the ξ_{OPT} in the 8-bit, 9-bit and 10-bit resistor networks, for different resistor tolerances are presented in Tab. 3. The results from this table show that the SF significantly increases with an increase of the number of bits in the DAC resistor networks. On the other side, the MPD for ξ_{OPT} increases much slower (Tab. 4).

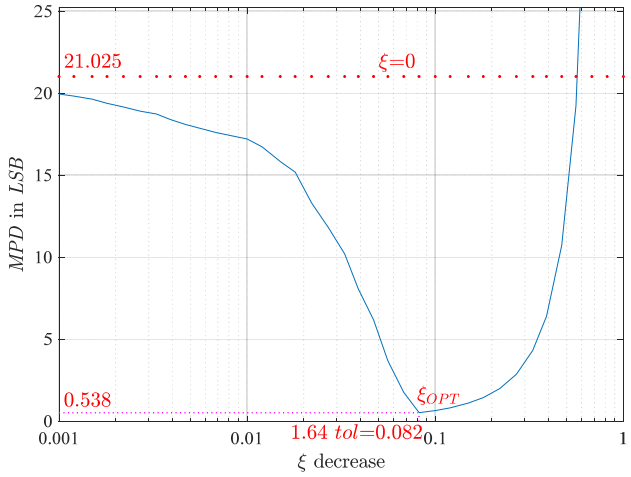

Fig. 15. The maximal +DNL as a function of ξ decrease, for resistor tolerances 5%, in a 9-bit resistor networks.

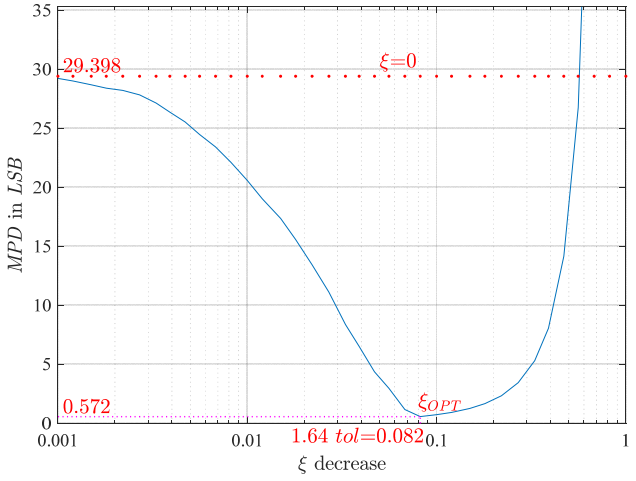

Fig. 16. The maximal +DNL as a function of ξ decrease, for resistor tolerances 5%, in a 10-bit resistor networks.

ξ_{OPT}	±1% *tol*	±2% *tol*	±5% *tol*	±10% *tol*	±20% *tol*
8-bit netw.	1.8 × *tol*	1.65 × *tol*	1.64 × *tol*	1.5 × *tol*	1.35 × *tol*
9-bit netw.	1.8 × *tol*	1.65 × *tol*	1.64 × *tol*	1.5 × *tol*	1.35 × *tol*
10-bit netw.	1.8 × *tol*	1.65 × *tol*	1.64 × *tol*	1.5 × *tol*	1.35 × *tol*

Tab. 2. Optimal ξ decrease values for different resistor tolerance and different number of bits in the resistor networks.

SF(ξ_{OPT})	±1% *tol*	±2% *tol*	±5% *tol*	±10% *tol*	±20% *tol*
8-bit netw.	23.627	24.569	22.008	19.726	17.727
9-bit netw.	44.740	44.248	39.076	33.190	29.766
10-bit netw.	55.558	55.446	51.392	46.557	43.258

Tab. 3. SF values in case of optimal ξ values for different resistor tolerance and different number of bits in resistor networks.

MPD(ξ_{OPT})	±1% *tol*	±2% *tol*	±5% *tol*	±10% *tol*	±20% *tol*
8-bit netw.	8.6%	16.6%	47%	109%	224.8%
9-bit netw.	8.9%	18.6%	53.8%	128.4%	269.4%
10-bit netw.	9.3%	20.1%	57.2%	137.3%	325.3%

Tab. 4. MPD values as percent of *LSB* in case of optimal ξ values for different resistor tolerance and different number of bits in resistor networks.

n	*tol*	$\xi = \xi(tol)$	ξ	ξ_n/ξ_{n-1}	$\xi_n = f(\xi_{n-1})$
1	1%	1.78 × *tol*	0.0178		$\xi_n \approx 0.935 \frac{tol_n}{tol_{n-1}} \xi_{n-1}$
2	2%	1.66 × *tol*	0.0332	1.86	
3	5%	1.57 × *tol*	0.0785	1.88 × 5/4	
4	10%	1.47 × *tol*	0.147	1.87	
5	20%	1.37 × *tol*	0.274	1.86	

Tab. 5. The results of simulation.

The values of ξ_{OPT}, shown in Tab. 2, are selected from the E12 series of preferred numbers. In order to determine more precise ξ_{OPT}, additional simulations are performed examining nearby values of ξ. The results of this simulation are shown in Tab. 5. Thanks to that, a simple relation between tolerances and ξ_{OPT} values is established.

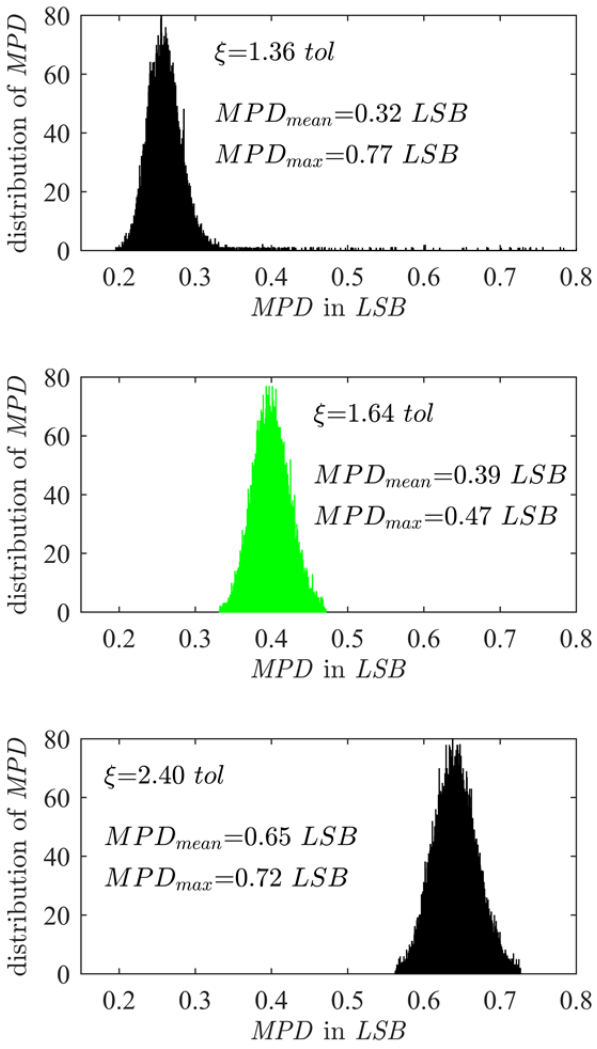

Fig. 17. Distribution of the MPD around their mean values (8-bit binary network, resistor tolerance 5%) for $\xi = \xi_{OPT} = 1.64tol$ and around it.

Distributions of MPD values, obtained in the 8-bit binary network circuit, with a resistor tolerance of 5% for $\xi = \xi_{OPT}$ and two consecutive values are shown in Fig. 17. The distribution is approximately Gaussian. The first histogram corresponds to $\xi < \xi_{OPT}$ value. In this case the MPD distribution is less concentrated around its mean value and the MPD may assume considerably higher values. The third histogram shows that for $\xi > \xi_{OPT}$ the mean and maximal value of the MPD distribution are greater. It the middle histogram (for $\xi = \xi_{OPT}$) the results are optimal. In this case the MPD mean value is equal to 0.399 *LSB*. The standard deviation σ(MPD) is 0.0224 ΔV_{LSB}. The maximal MPD deviation from the mean value is 0.0722 LSB, what is equal to 3.22 σ.

Statistical method is applied on 100000 samples of digital-analog circuits for each ξ value and resistor tolerance in the 8-bit, 9-bit and 10-bit resistor networks. Such a statistical sample is large enough for deriving reliable conclusions. For example, we have obtained in the 8-bit binary network circuit with a resistor tolerance of 5%, that all the values of the MPD are smaller or equal to 0.471 LSB, and that their distribution around the mean value is approximately of Gaussian type (Fig. 17). Thus, the probability that the MPD occurs outside of this range is significantly smaller than 0.00001 (1/100000). This probability is sufficient to justify the practical application of these circuits and the results obtained by statistical analysis.

4. Discussion

For the best circuit performance, especially speed, the DACs are dominantly produced in integrated circuit technology. In that case resistor values are not limited to E12 or any other series. The resistor values are determined in general by non-discrete resistor geometry. On the other side, the main problem is the precision due technology limitations [26]. There are methods which can help to match resistors pretty close to the optimal ratio [27], [28]. All mentioned is perfectly suitable for our DAC that accepts high tolerances of resistors. The precision demand decline from the MSB to the LSB, so only the first few resistors in the network preferably have to be matched as precise as possible.

However, this paper is not dealing with the IC design. Our method is presented on the simplest DAC with resistor network, but it is applicable also to other DACs realizations more suitable for the IC design like the current steering DAC [22].

The next consideration is about imperfection of transistor switches, mainly about their ON state resistance R_{ON}, and its influence on the DAC transfer characteristic and MPD. R_{ON} is added to each DAC resistor and hence its influence can be decreased by reducing resistances in DAC network for nominal value of R_{ON}. Thanks to that, impact on DAC characteristics will come only from R_{ON} deviation. By looking at the characteristics of various commercial switch circuits it can be seen that R_{ON} deviation is approximately 10% of its nominal values. Therefore R_{ON} influence is 10 times less. At the end, R_{ON} impact can be considered as extension (less than 1%) of the DAC resistors tolerance. Taking that tolerance, the proposed method is equally applicable.

DAC integrated circuit	MPD in LSB	Settling time (µs)
DAC3484 (current steering)	2	0.01
DAC38J82 (current steering)	4	0.01
MAX512 (R/2R)	1	0.07
DAC8229 (R/2R)	1	0.2
MAX548B (R/2R)	1	0.25
AD7224 (R/2R)	1	>5
MCP4901 (string DAC)	0.5	4.5
DAC8541 (string DAC)	0.5	10
LTC1450 (string DAC)	0.5	14

Tab. 6. MPD and settling time in some DAC integrated circuits available on the market.

Finally, we tried to estimate potential speed of the proposed DAC. For that purpose we collect some data of market available DACs and present it in Tab. 6. Our proposed method is best suited for the current steering DAC which is the fastest one.

5. Conclusion

The paper presents an approach to build a precise binary weighted DAC using "imprecise" resistors. It is shown that an appropriate change of the standard binary weighted resistor values may provide better analog range coverage, with low positive DNL. From the presented statistical method, with various resistor ratios in the circuit and various resistor tolerances, we have concluded that the optimal change in resistor value slightly depends on resistor tolerances. Based on the simulations with the 8, 9, and 10-bit resistor networks, we have concluded that optimal ratio practically does not depend on the number of DAC bits.

The other important DAC static parameters like gain and offset errors can easily be removed by calibration. The INL and the negative DNL can be alleviated by an appropriate calibration procedure as well. Detailed analysis of the possible calibration procedures is extensive. It is a topic of our ongoing research.

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