An Efficient MRTD Model for the Analysis of Crosstalk in CMOS-Driven Coupled Cu Interconnects

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Abstract. *This paper presents an efficient wavelet based numerical method for analyzing functional and dynamic crosstalk of CMOS driven coupled copper (Cu) interconnects known as Multi-Resolution Time Domain (MRTD), wherein, the CMOS drivers are modeled using n^{th}-power law model. The performance of the proposed MRTD method is evaluated through recursive simulations in HSPICE environment and compared with the conventional Finite Difference Time Domain (FDTD) method at 32-nm technology node for global interconnects of length 1mm, where the computations of the proposed model and conventional FDTD are carried out using MATLAB. For different number of test cases, the proposed MRTD method gives an average error of 0.14 % and 1.9 % for peak crosstalk noise and peak noise timing, respectively, with respect to HSPICE results. Also, the dynamic crosstalk noise on victim line of the proposed MRTD method are in close agreement with those of HSPICE. The results show the dominance of the proposed MRTD method over the conventional FDTD method regarding accuracy. The proposed MRTD method is also extended for three-mutually-coupled interconnect lines for crosstalk analysis, with an average error less than 1 % when compared to that of more than 3 % using the conventional FDTD method. Moreover, for the transient analysis, the MRTD method is more time efficient than HSPICE.*

Keywords

CMOS driver, Cu interconnects, peak crosstalk noise, delay, MRTD, FDTD, HSPICE

1. Introduction

With the evolution of deep sub-micron CMOS technology, the circuits in chips (SOCs) allow Giga-scale integration. In such circuits, the analysis of interconnects have become extremely important to determine the performance of a circuit such as power consumption and time delay. In addition to the delay, with the high operating frequencies, crosstalk is a pitfall in the design of interconnect structures for circuitry. As on-chip circuitry is gradually miniaturized, the adjacent interconnects are brought into closer proximity. Accordingly, the undesired signal coupling between the interconnects gets elevated [1].So, the precise prediction of peak crosstalk noise and peak noise timing in a driver-interconnect-load (DIL) system has become a critical design view for a long period [1].

For the analysis of the crosstalk noise, most of the earlier models have considered non-linear CMOS driver as a simple linear resistor [2], [3], which leads to a discrepancy in the results. Because, during the transient, MOSFET operates in saturation region about 50 % of its operating time and rest of time in linear (or) cutoff regions [4].

To model a DIL system, several methods have been reported in the recent state of the art works , where different analytical solutions, the Finite Difference Time Domain (FDTD) method and SPICE solutions are explored [5], [6]. The alpha-power law model used for modeling non-linear CMOS driver and an interconnect line is modeled using the Analytical approach for the analysis of functional crosstalk effects [5] and dynamic crosstalk effects [7]. The models outlined in [5] and [7] is limited to only two coupled interconnect lines resulting in dependance on even-odd modes. To analyze the dynamic crosstalk of multiple mutually coupled on-chip interconnect lines, Vobulapuram et al. in [8] used FDTD method for modeling of interconnect lines where CMOS driver is represented using alpha-power law model. The alpha-power law model becomes imprecise with the technology scaling, as it ignores the finite drain conductance (λ) parameter. Later, in [9], Vobulapuram et al. employed n^{th} power law model [10], which includes the finite drain conductance (λ) parameter to represent CMOS driver with FDTD [11] for modeling mutually coupled interconnect lines.

The conventional FDTD method is a substantial numerical technique for solving partial differential equations and Electromagnetic problems. But the conventional FDTD method is numerically dispersive [12]. The Multiresolution Time-Domain (MRTD) method proposed by Krumpholz et al. in [13] presents significant advantages in numerical dispersion properties [14]–[17]. In Multiresolution analysis using the Haar scaling function as the basis function, the MRTD algorithm is equally accurate with the conventional FDTD [15]. The Daubechies' scaling function based MRTD method with three and four vanishing moments shows higher

accuracy than conventional FDTD [16]. The MRTD method using the Daubechies' scaling function as the basis function for the transient analysis of transmission lines shows a better dispersion property than the FDTD method [18]. However, the MRTD method has not been used to calculate the crosstalk noise and delay of CMOS driven coupled on-chip interconnects in the present state of the art works.

This paper adopted the MRTD [18] method for the analysis of crosstalk noise of VLSI interconnects. To drive the interconnect lines a non-linear CMOS driver is considered, which is modeled using nth power law model [10].

The rest of the paper is organized as follows: Section 2 discusses the formulation of the MRTD method for coupled Cu interconnect lines. Section 3 describes the simulation setup and the validation of the results for two and three coupled interconnects, followed by conclusion in Sec. 4.

2. Formulation of the MRTD Method

The proposed MRTD method is developed using Daubechies' scaling function as the basis function having four vanishing moments for coupled VLSI interconnects. In a more practical approach, CMOS drivers are considered for analyzing the performance more precisely. Capacitive loads are considered for the termination of interconnect lines. The schematic of the CMOS-driven coupled interconnect lines are shown in Fig. 1. C_{d} and C_{m} are the parasitic capacitance of CMOS, where C_{d} represents drain diffusion capacitance and C_{m} represents gate-to-drain coupling capacitance.

Where R_x is the line resistance per unit length (p.u.l.), L_x is line inductance p.u.l. C_x is line capacitance p.u.l. The subscript x represents aggressor line at $x = 1$ and victim line at $x = 2$. C_{L} is the load capacitance. The interconnect lines are coupled inductively M_{C} and capacitively C_{C}.

2.1 Modeling of Coupled VLSI Interconnects

The coupled on-chip interconnects considered as distributed RLC transmission lines are described by telegrapher's equation [11].

$$\frac{\partial \mathbf{V}(z,t)}{\partial z} + \mathbf{R}\mathbf{I}(z,t) + \mathbf{L}\frac{\partial \mathbf{I}(z,t)}{\partial t} = 0, \tag{1a}$$

$$\frac{\partial \mathbf{I}(z,t)}{\partial z} + \mathbf{C}\frac{\partial \mathbf{V}(z,t)}{\partial t} = 0 \tag{1b}$$

where the voltages ($\mathbf{V}$) and currents ($\mathbf{I}$) are expressed in 2×1 column vector form $\begin{bmatrix} \mathrm{V}_1 & \mathrm{V}_2 \end{bmatrix}^{\mathrm{T}}$, $\begin{bmatrix} \mathrm{I}_1 & \mathrm{I}_2 \end{bmatrix}^{\mathrm{T}}$ and line parasitics are expressed in 2×2 matrices per unit length as shown below.

$$\mathbf{R} = \begin{bmatrix} \mathrm{R}_1 & 0 \\ 0 & \mathrm{R}_2 \end{bmatrix}, \mathbf{L} = \begin{bmatrix} \mathrm{L}_1 & \mathrm{M}_{\mathrm{C}} \\ \mathrm{M}_{\mathrm{C}} & \mathrm{L}_2 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} \mathrm{C}_1 + \mathrm{C}_{\mathrm{C}} & -\mathrm{C}_{\mathrm{C}} \\ -\mathrm{C}_{\mathrm{C}} & \mathrm{C}_2 + \mathrm{C}_{\mathrm{C}} \end{bmatrix}.$$

The accuracy and stability of the MRTD method for solving telegrapher's equations is achieved by considering the voltages and currents which are separated by $\frac{\Delta z}{2}$ in space and $\frac{\Delta t}{2}$ in time as shown in Fig. 2, where Δz is the space discretization interval and Δt is the time discretization interval.

A CMOS driver drives the interconnect line of length l at $z = 0$ and capacitive load terminates it at $z = l$. The line is divided uniformly into Nz segments of length $\Delta z = \frac{l}{Nz}$, representing the discretized voltage and current nodes which are unknown coefficients as shown in Fig. 3., where I_0 represents the source current.

To solve (1a) and (1b), the voltage and current terms can be expanded using the known functions ($\phi_k(z)$ and $h_n(t)$) and the unknown coefficients are considered from the method outlined in [13] as:

$$V(z,t) = \sum_{k,n=-\infty}^{+\infty} V_k^n \phi_k(z)\, h_n(t), \tag{2a}$$

$$I(z,t) = \sum_{k,n=-\infty}^{+\infty} I_{k+\frac{1}{2}}^{n+\frac{1}{2}} \phi_{k+\frac{1}{2}}(z)\, h_{n+\frac{1}{2}}(t) \tag{2b}$$

where V_k^n is the coefficient of the voltage expansion and $I_{k+\frac{1}{2}}^{n+\frac{1}{2}}$ is the coefficient of the current expansion in terms of scaling functions. The indices k and n are the discrete spatial and temporal indices related to space and time coordinates via $z = k\Delta z$ and $t = n\Delta t$.

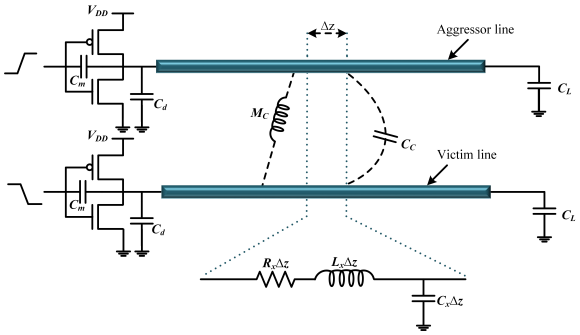


Fig. 1. DIL system for CMOS driven coupled Cu interconnects.

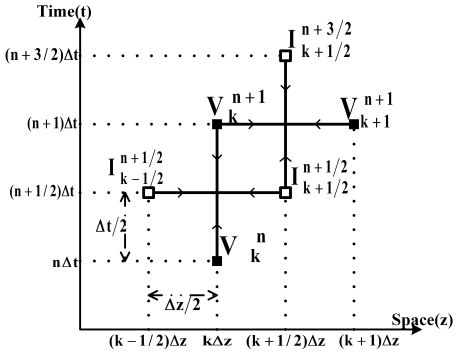


Fig. 2. Space and time discretization relation for acquiring second order accuracy.

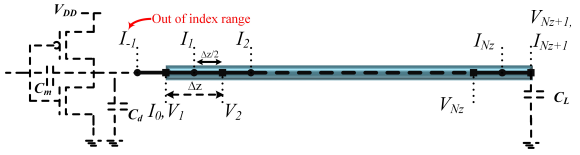


Fig. 3. Spatial discretization of MRTD technique for DIL system.

The function $h_n(t)$ and $\phi_k(z)$ is defined as:

$$h_n(t) = h\left(\frac{t}{\Delta t} - n\right), \tag{3}$$

$$\phi_k(z) = \phi\left(\frac{z}{\Delta z} - k\right) \tag{4}$$

where $h(t)$ represents a Haar scaling function and $\phi(z)$ represents a Daubechies' scaling function.

To derive the MRTD method for equation (1a) and (1b), the following integrals [19] are considered:

$$\langle h_n(t), h_{n'}(t)\rangle = \delta_{n,n'}\Delta t, \tag{5a}$$

$$\langle \phi_k(z), \phi_{k'}(z)\rangle = \delta_{k,k'}\Delta z, \tag{5b}$$

$$\left\langle h_n(t), \frac{\partial h_{n'+\frac{1}{2}}(t)}{\partial t}\right\rangle = \delta_{n,n'} - \delta_{n,n'+1}, \tag{6a}$$

$$\left\langle \phi_k(z), \frac{\partial \phi_{k'+\frac{1}{2}}(z)}{\partial z}\right\rangle = \sum_{i=-S_b}^{S_b-1} a(i)\,\delta_{k+i,k'} \tag{6b}$$

where $\delta_{k,k'}$ and $\delta_{n,n'}$ represents the Kronecker symbol. In equation (6b) S_b denotes the effective support size of the basis functions. The coefficients $a(i)$ are called connection coefficients. By considering Daubechies' scaling function having four vanishing moments (D_4) as the basis functions, Tab. 1 shows $a(i)$ for $1 \le i \le S_b$, whereas $a(i)$ for $i > S_b$ are zero and for $i < 1$ it can be obtained by the symmetry relation $a(-1-i) = -a(i)$.

Applying the Galerkin technique [13] to equations (1a) and (1b) using the test functions $\phi_{k+\frac{1}{2}} h_n(t)$ and $\phi_k h_{n+\frac{1}{2}}(t)$, the following iterative equations for the currents and voltages are obtained:

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \sum_{i=1}^{S_b} a(i)\left(V_{k+i}^n - V_{k-i+1}^n\right), \tag{7a}$$

$$V_k^{n+1} = V_k^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{S_b} a(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right), \tag{7b}$$

where $B_1 = \left(\frac{L}{R} + \frac{\Delta t}{2}\right)^{-1}\left(\frac{L}{R} - \frac{\Delta t}{2}\right)$, $B_2 = \left(1 + \frac{\Delta t}{2} R L^{-1}\right)^{-1}$.

In the iterative equations (7a) and (7b), not only the near-end boundary voltage V_1^{n+1} and far-end boundary voltage V_{Nz+1}^{n+1} are derived but also the iterative equations of the voltages and currents near the boundaries also need to be updated. Near the boundaries the voltages are represented by V_i^{n+1} and V_{Nz+1-i}^{n+1} for $i = 2, 3, \cdots, S_b$ and the currents by $I_{i+\frac{1}{2}}^{n+\frac{1}{2}}$ and $I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}}$ $i = 1, 2, 3, \cdots, S_b - 1$. All these voltages and currents have some terms that exceed the index range in iterative equations (7a) and (7b).

i	Connection coeff. $a(i)$ for D_4
1	1.3110340773
2	−0.1560100110
3	0.0419957460
4	−0.0086543236
5	0.0008308695
6	0.0000108999
7	0.0000000041

Tab. 1. Connection coefficients $a(i)$ of Daubechies' scaling functions (D_4) [16].

For updating the iterative equations of voltages and currents, equation (7a) and (7b) need to be decomposed using the relation in [20], which satisfies the coefficients $a(i)$ given by

$$\sum_{i=1}^{S_b}(2i-1)a(i) = 1. \tag{8}$$

Substituting (8) into (7b), we get

$$\sum_{i=1}^{S_b}(2i-1)\,a(i)\,V_k^{n+1} = \sum_{i=1}^{S_b}(2i-1)\,a(i)\,V_k^n - \sum_{i=1}^{S_b}\frac{\Delta t}{(2i-1)} \Delta z C^{-1}\left[(2i-1)a(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right]. \tag{9}$$

Considering the corresponding terms with i, we can decompose (7b) as:

$$(2i-1)\,a(i)\,V_k^{n+1} = (2i-1)\,a(i)\,V_k^n - (2i-1)\,a(i)\,\frac{\Delta t}{(2i-1)\,\Delta z} C^{-1}\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right), \tag{10}$$

for $i = 1, 2, 3, \ldots, S_b$.

Equation (10) is further modified by applying the boundary conditions as illustrated in Sec. 2.2 and Sec. 2.3 respectively.

2.2 Modeling of CMOS Driver

The CMOS drivers are modeled using nth power law model that considers the effect of finite drain conductance parameter (λ) along with velocity saturation. During transient simulation the operation of the pMOS and nMOS transistors are in either linear, saturation (or) cutoff regions [4].

The pMOS and nMOS current equations using n^{th} power law model are

$$I_p = \begin{cases} I_{DSATp}\left(1 + \lambda_p\left(V_{DD} - V_{DS}\right)\right) & \left(2 - \frac{V_{DD}-V_{DS}}{V_{DSATp}}\right)\left(\frac{V_{DD}-V_{DS}}{V_{DSATp}}\right) \\ & V_{DS} > V_{DD} - V_{DSATp} \\ & \text{(linear)} \\ I_{DSATp}\left(1 + \lambda_p\left(V_{DD} - V_{DS}\right)\right) & V_{DS} \le V_{DD} - V_{DSATp} \\ & \text{(saturation)} \\ 0 & V_{GS} \ge V_{DD} - \left|V_{Tp}\right| \\ & \text{(cutoff)} \end{cases} \tag{11a}$$

$$I_n = \begin{cases} I_{DSATn}\left(1+\lambda_n V_{DS}\right)\left(2-\frac{V_{DS}}{V_{DSATn}}\right)\left(\frac{V_{DS}}{V_{DSATn}}\right) & V_{DS} < V_{DSATn} \\ & \text{(linear)} \\ I_{DSATn}\left(1 + \lambda_n V_{DS}\right) & V_{DS} \ge V_{DSATn} \\ & \text{(saturation)} \\ 0 & V_{GS} \le V_{Tn} \\ & \text{(cutoff)} \end{cases} \tag{11b}$$

where I_{DSATp} (I_{DSATn}), λ_p (λ_n), V_{DSATp} (V_{DSATn}), and V_{Tp} (V_{Tn}) are the drain saturation current, finite drain conductance parameter, drain saturation voltage and the threshold

voltage of pMOS (nMOS) respectively. The drain saturation voltages and currents of pMOS and nMOS are obtained from

$$V_{\mathrm{DSATp}} = K_{\mathrm{p}}\left(V_{\mathrm{DD}} - V_{\mathrm{GS}} - \left|V_{\mathrm{Tp}}\right|\right)^{m_{\mathrm{p}}}, \tag{12a}$$

$$V_{\mathrm{DSATn}} = K_{\mathrm{n}}\left(V_{\mathrm{GS}} - V_{\mathrm{Tn}}\right)^{m_{\mathrm{n}}}, \tag{12b}$$

$$I_{\mathrm{DSATp}} = \frac{W_{\mathrm{p}}}{L_{\mathrm{eff}}} B_{\mathrm{p}}\left(V_{\mathrm{DD}} - V_{\mathrm{GS}} - \left|V_{\mathrm{Tp}}\right|\right)^{n_{\mathrm{p}}}, \tag{12c}$$

$$I_{\mathrm{DSATn}} = \frac{W_{\mathrm{n}}}{L_{\mathrm{eff}}} B_{\mathrm{n}}\left(V_{\mathrm{GS}} - V_{\mathrm{Tn}}\right)^{n_{\mathrm{n}}}. \tag{12d}$$

The parameters $K_{\mathrm{p}}\,(K_{\mathrm{n}})$ and $m_{\mathrm{p}}\,(m_{\mathrm{n}})$ control the linear region, whereas $B_{\mathrm{p}}\,(B_{\mathrm{n}})$ and $n_{\mathrm{p}}\,(n_{\mathrm{n}})$ control the saturation region characteristics of pMOS (nMOS) transistor. The effective channel length is represented by L_{eff} and the width of pMOS (nMOS) represented by $W_{\mathrm{p}}\,(W_{\mathrm{n}})$. The model parameters [9] of pMOS and nMOS transistors are listed in Tab. 2 for 32-nm technology node.

Parameter	pMOS	nMOS
m	0.087	0.211
n	1.07	0.915
B	8.01×10^{-6}	35.5×10^{-6}
K	0.316	0.369
λ	3.11	0.867
V_T	0.366	0.36

Tab. 2. Model parameters of pMOS and nMOS for 32-nm technology node [9].

2.3 Modeling of DIL System

Modeling of the DIL system is incorporated with the boundary conditions. The current equations incorporate near-end and far-end interconnect terminal conditions, where the nodal equation of the source current (I_0) at the near-end terminal (at $k = 1$) is given by:

$$I_0 = C_{\mathrm{m}}\frac{\mathrm{d}V_s}{\mathrm{d}t} - \left(C_{\mathrm{m}} + C_{\mathrm{d}}\right)\frac{\mathrm{d}V_1}{\mathrm{d}t} + \left(I_{\mathrm{p}} - I_{\mathrm{n}}\right) \tag{13}$$

where $V_s = V_{\mathrm{GS}}$ and $V_1 = V_{\mathrm{DS}}$.
By applying the Galerkin technique [13] to eq. (13), we obtain

$$\begin{aligned}(\Delta z)(\Delta t)\, I_0^{n+1} = {} & C_{\mathrm{m}}(\Delta z)\left(V_s^{n+1} - V_s^n\right) - \left(C_{\mathrm{m}} + C_{\mathrm{d}}\right)(\Delta z) \\ & \left(V_1^{n+1} - V_1^n\right) + (\Delta z)(\Delta t)\, I_{\mathrm{p}}^{n+1} - (\Delta z)(\Delta t)\, I_{\mathrm{n}}^{n+1}.\end{aligned} \tag{14}$$

So, the voltage at near-end terminal of interconnect is obtained by substituting $k = 1$ in equation (7b)

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{S_{\mathrm{b}}} a(i)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}\right). \tag{15}$$

Equation (15) is decomposed by following the steps from the equations (8)–(10). From the decomposition, we know that the subscript of the term $I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}$ in equation (15) exceeds the index range, for $i = 2, 3, \cdots, S_{\mathrm{b}}$. So, a forward difference scheme is used to overcome this difficulty. Therefore, the final iterative equation for near-end terminal voltage $\left(V_1^{n+1}\right)$ is updated as

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{L_s} 2a(i)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right). \tag{16}$$

In equation (16), by substituting $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and I_0^{n+1} from equation (14) we get

$$\begin{aligned}V_1^{n+1} = {} & V_1^n - A_1 A_2 \left(2\sum_{i=1}^{S_{\mathrm{b}}} a(i) I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - \sum_{i=1}^{S_{\mathrm{b}}} a(i)\right. \\ & \left.\left(I_0^n + C_{\mathrm{m}}\left(\frac{V_s^{n+1} - V_s^n}{\Delta t}\right) + I_{\mathrm{p}}^{n+1} - I_{\mathrm{n}}^{n+1}\right)\right),\end{aligned} \tag{17}$$

where, $A_1 = \left(1 + \frac{C^{-1}}{\Delta z}\left(C_{\mathrm{m}} + C_{\mathrm{d}}\right)\sum_{i=1}^{S_{\mathrm{b}}} a(i)\right)^{-1}$ and $A_2 = \frac{\Delta t}{\Delta z} C^{-1}$.

Similarly, at the far-end terminal $(k = Nz+1)$, the nodal equation of the load current (I_{Nz+1}) is given by

$$I_{Nz+1} = C_{\mathrm{L}}\frac{\mathrm{d}V_{Nz+1}}{\mathrm{d}t}. \tag{18}$$

The final iterative equation at the far-end terminal is given by

$$V_{Nz+1}^{n+1} = V_{Nz+1}^n - D_1 D_2\left(\sum_{i=1}^{S_{\mathrm{b}}} a(i)\, I_{Nz+1}^{n+\frac{1}{2}} - \sum_{i=1}^{S_{\mathrm{b}}} 2a(i)\, I_{Nz+1-i+\frac{1}{2}}^{n+\frac{1}{2}}\right), \tag{19}$$

where, $D_1 = \left(1 + \frac{C_{\mathrm{L}}}{\Delta z} C^{-1}\sum_{i=1}^{S_{\mathrm{b}}} a(i)\right)$, $D_2 = \frac{\Delta t}{\Delta z} C^{-1}$.

In continuation with the algorithm, to derive and update the iterative equations, some term indices exceed the index range for all nodes between the terminal, therefore a truncation method is employed.

Taking V_k^{n+1} as an example for $k = 2, 3, \ldots, S_{\mathrm{b}}$ and following the steps of equation (9) and (10), we can decompose (7b) as

$$a(1)\, V_k^{n+1} = a(1)\, V_k^n - a(1)\,\frac{\Delta t}{\Delta z} C^{-1}\left(I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}}\right), \tag{20a}$$

$$3a(2)\, V_k^{n+1} = 3a(2)\, V_k^n - 3a(2)\,\frac{\Delta t}{3\Delta z} C^{-1}\left(I_{k+\frac{3}{2}}^{n+\frac{1}{2}} - I_{k-\frac{3}{2}}^{n+\frac{1}{2}}\right), \tag{20b}$$

$$\vdots$$

$$\begin{aligned}(2k-1)\, a(k)\, V_k^{n+1} = {} & (2k-1)\, a(k)\, V_k^n - (2k-1)\, a(k) \\ & \frac{\Delta t}{(2k-1)\,\Delta z} C^{-1}\left(I_{2k-\frac{1}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}}\right),\end{aligned} \tag{20c}$$

$$\begin{aligned}(2k+1)\, a(k+1)\, V_k^{n+1} = {} & (2k+1)\, a(k+1)\, V_k^n - (2k+1)\, a(k+1) \\ & \frac{\Delta t}{(2k+1)\,\Delta z} C^{-1}\left(I_{2k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right),\end{aligned} \tag{20d}$$

$$\vdots$$

$$\begin{aligned}(2S_{\mathrm{b}}-1)\, a(S_{\mathrm{b}})\, V_k^{n+1} = {} & (2S_{\mathrm{b}}-1)\, a(S_{\mathrm{b}})\, V_k^n - (2S_{\mathrm{b}}-1)\, a(S_{\mathrm{b}}) \\ & \frac{\Delta t}{(2S_{\mathrm{b}}-1)\,\Delta z} C^{-1}\left(I_{k+S_{\mathrm{b}}-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-S_{\mathrm{b}}+\frac{1}{2}}^{n+\frac{1}{2}}\right).\end{aligned} \tag{20e}$$

From the equations (20a)–(20e), it can be observed that for the first k terms, the indices of the equations doesn't exceed the index range, whereas, all the equations for which

the index terms exceed the index range appear in the rest $S_b - k$ terms. As $S_b - k$ terms go out-of-bounds, these equations are unavailable for forming iterative equations in MRTD method. To avoid this problem, a truncation is made in the equations where the index range is exceeding.

By summing up the first k terms in equations (20a)–(20e), we can obtain the modified iterative equations for $k = 2, 3, \cdots, S_b$

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{k} (2i-1)\, a(i)\right)^{-1} D_2 \left(\sum_{i=1}^{k} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right). \tag{21}$$

Using the same steps illustrated in equations (20a)−(20e), a modified iterative equations of voltages at interior points as shown in equation (22) and voltages near the load as shown in equation (23).

For $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$,

$$V_k^{n+1} = V_k^n - D_2 \left(\sum_{i=1}^{S_b} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right), \tag{22}$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$,

$$V_k^{n+1} = V_k^n - \left(\sum_{i=1}^{Nz-k+1} (2i-1)\, a(i)\right)^{-1} D_2 \left(\sum_{i=1}^{Nz-k+1} a(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right). \tag{23}$$

The iterative equations of current can be updated by following the same steps of voltage iterative equations with a slight difference. As shown in Fig. 3, it is observed that the current nodes appear at the half-integer points, which means that all the currents are located at the interior points of terminals. So, the currents near the terminals need to be modified.

For the iterative equations of current near the terminals, we need to decompose (7a) by using the steps from voltage iterative equations. The final modified current iterative equations are obtained as

for $k = 1$, near the source

$$I_{1+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{1+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{i+1}^{n+1} - V_1^{n+1}\right)\right), \tag{24}$$

for $k = 2, 3, \cdots, S_b$

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{k} (2i-1)\, a(i)\right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{k} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1}\right)\right), \tag{25}$$

for $k = S_b + 1, S_b + 2, \cdots, Nz - S_b, Nz - S_b + 1$, iterative equations at interior points are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{S_b} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1}\right)\right), \tag{26}$$

for $k = Nz - S_b + 2, Nz - S_b + 3, \cdots, Nz$, iterative equations near the load are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = B_1 I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - B_2 \left(\sum_{i=1}^{Nz-k+1} (2i-1)\, a(i)\right)^{-1} \frac{\Delta t}{\Delta z} L^{-1} \left(\sum_{i=1}^{Nz-k+1} a(i) \left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1}\right)\right). \tag{27}$$

A bootstrapping approach is used for evaluating the updated voltage and current iterative equations. Foremost, the voltage iterative equations are solved at fixed time using equations (17), (19), (21)–(23) in terms of past values of voltages and currents. Thereafter, the iterative equations of currents are solved from equations (24)–(27) in terms of voltages evaluated initially and past values of currents. So, to get the stable output for the MRTD iterative equations, the courant stability condition [18], [20] is considered as

$$\Delta t \leq \frac{q \Delta z}{\vartheta} \tag{28}$$

which states that the propagation time must be greater than the time step, over each cell. where q is a Courant number given by $q = \frac{1}{\sum_{i=1}^{L_s} |a(i)|} = \frac{\vartheta \Delta t}{\Delta z}$ and ϑ is the phase velocity of propagation on the line.

3. Simulation Setup and Validation of Results

The proposed MRTD method is validated in HSPICE using W-element method and compared with the conventional FDTD method. The coupled interconnect lines are driven using symmetric CMOS drivers. To maintain the symmetry in operation of CMOS inverter, the aspect ratio of W_p to W_n is chosen to be 2 : 1, with the width of pMOS (W_p) is chosen to be 3.2 µm. A ramp signal falling from 0.9 V(V_{DD}) to 0 V with a transition time of 10 ps, is given as an input to the CMOS driver of aggressor line. The technology used is 32-nm with thickness and width of the interconnect line as 0.66 µm and 0.22 µm respectively, with an aspect ratio of 3:1 [9]. The height from the ground plane is considered to be equal to the thickness of the interconnect line and the spacing between the two interconnect lines is assumed to be equal to its width. The global level interconnect length, load capacitance and inter-layer metal-insulator dielectric constant of the line are 1 mm, 2 fF and 2.2 respectively. The line parasitics extracted using the setup mentioned above are shown in Tab. 3.

The corresponding mode velocities, for given line parasitics, are calculated as odd mode velocity $\vartheta_o = 1.71 \times 10^8$ m/s and even mode velocity $\vartheta_e = 1.45 \times 10^8$ m/s. To obtain high accuracy, the value of space discretization (Δz) is computed to be less than 0.46 mm, by considering break frequency of 32 GHz and even mode velocity. The time discretization (Δt) value is calculated to be 1.869 ps by using the value of (Δz) and odd mode velocity for the Courant number $q = 0.7$.

R [kΩ/m]	**L** [μH/m]	**C** [pF/m]	$\mathbf{C_C}$ [pF/m] (between A* line and V* line)	$\mathbf{M_{C12}}$ [μH/m] (between A* line and V* line)	$\mathbf{M_{C13}}$ [μH/m] (between two A* lines)
151.5	1.645	15.114	98.598	1.484	1.264

Tab. 3. Interconnect parasitics for setup mentioned in Sec. 3(A*–Aggressor, V*–Victim).

3.1 Transient Analysis of Coupled Two Interconnect Lines

The analysis of inclusive crosstalk noise at far-end terminal of the victim line is performed using, HSPICE, conventional FDTD method and the proposed MRTD method. The transient response of switching of functional crosstalk and dynamic in-phase as well as out-phase crosstalk, are illustrated in Figs. 4a–4c. For functional crosstalk, the victim line remains at ground level, whereas, the aggressor line makes a transition from the ground to V_{DD}. For dynamic in-phase crosstalk, the switching from ground to V_{DD} takes place in both aggressor and victim lines. Finally, the transition takes place from V_{DD} to ground and ground to V_{DD} in aggressor and victim lines, respectively for dynamic out-phase crosstalk. It is observed from Fig. 4 that the proposed MRTD method dominates the existing conventional FDTD method and is in good agreement with HSPICE.

Table 4 presents the computational error in predicting the crosstalk induced peak voltage and timing, on quiescent victim line, using the proposed MRTD model and the conventional FDTD, with respect to HSPICE simulations. The percentage error can be calculated for the methods (M) with respect to HSPICE (H) by using the equation (29).

$$\%\text{ age error} = \left(\frac{H-M}{H}\right) \times 100. \tag{29}$$

The model is tested for the robustness at different input transition times. It is observed from Tab. 4 that, for the proposed model, the average error in prediction of crosstalk peak voltage is 0.14 % when compared to that of 2.7 % for conventional FDTD method. It can also be inferred from the Tab. 4 that the peak noise timing is well predicted using proposed model with average error of 1.9 % when compared to that of 2.8 % using the conventional FDTD method.

3.2 Transient Analysis of Three Mutually Coupled Interconnect Lines

Further, the proposed MRTD method is extended to three-coupled interconnect lines as illustrated in Fig. 5 and it is validated using HSPICE (W-element). The interconnect line parasitics for the analysis of the crosstalk of three-coupled lines can be extracted using the setup described in Sec. 3.

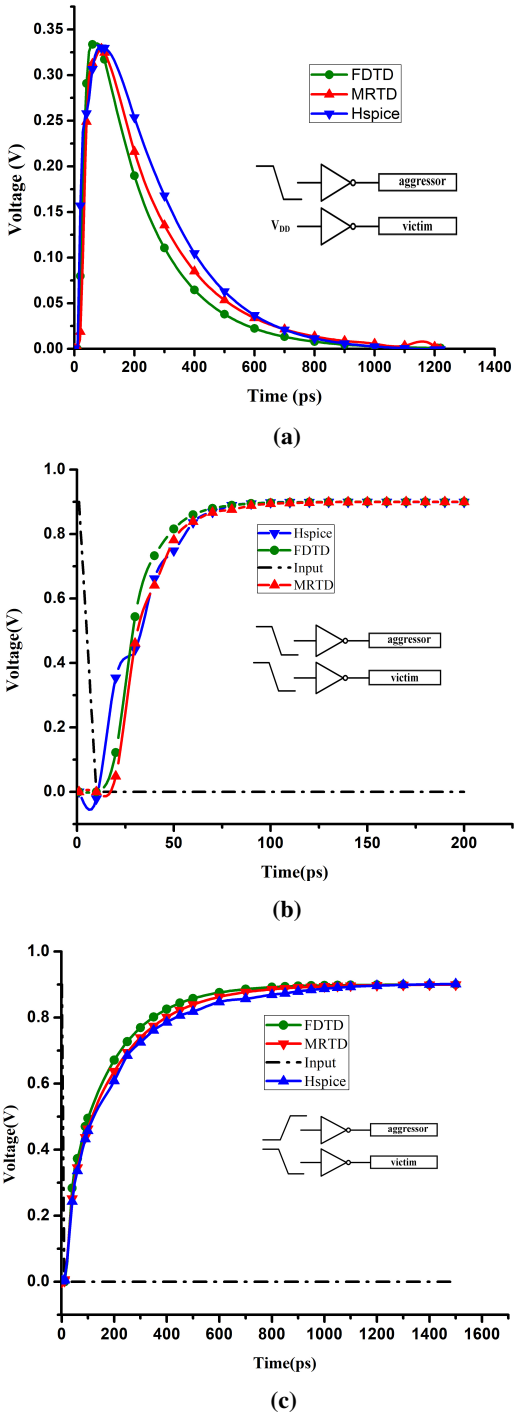


Fig. 4. Transient response at the far-end terminal of the victim line during the switching of (a) functional crosstalk (b) dynamic in-phase and (c) dynamic out-phase crosstalk.

Input Transition Time [ps]	Peak Crosstalk Noise [V]					Peak Noise Timing [ps]				
	HSPICE	Proposed Model	conv.* FDTD	% age error Proposed	% age error FDTD	HSPICE	Proposed Model	conv.* FDTD	% age error Proposed	% age error FDTD
10	0.33061	0.3288	0.34	0.55	-2.84	91.606	90	89.2	1.75	2.63
20	0.33002	0.3286	0.3398	0.43	-2.96	95.9	94	92.8	1.98	3.23
30	0.32917	0.3284	0.3392	0.234	-3.05	104.2	102.7	101	1.44	3.07
40	0.32875	0.3276	0.3385	0.35	-2.96	114.8	113.2	110.9	1.4	3.39
50	0.32834	0.3274	0.3376	0.29	-2.82	118	116.2	116	1.53	1.69
60	0.32785	0.3269	0.3366	0.49	-2.66	128.6	126.43	125	1.7	2.79
70	0.32635	0.3264	0.3355	-0.02	-2.80	134.56	132.8	131.4	1.31	2.35
80	0.32512	0.3259	0.3343	-0.24	-2.82	140.45	138.52	137.8	1.374	1.88
90	0.32382	0.3251	0.3328	-0.39	-2.77	150.2	144	142.96	4.13	4.82
100	0.32289	0.324	0.3296	-0.343	-2.07	158.31	154.83	153.6	2.19	2.98

Tab. 4. Computational error involved for peak crosstalk noise and peak noise timing on victim line (conv.*–conventional).

The coupling capacitance between the two aggressor lines can be neglected safely as the spacing between them is large [21].

$$\mathbf{R} = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{bmatrix}, \mathbf{L} = \begin{bmatrix} L_1 & M_{C12} & M_{C13} \\ M_{C12} & L_2 & M_{C12} \\ M_{C13} & M_{C12} & L_3 \end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix} C_1 + C_C & -C_C & 0 \\ -C_C & C_1 + 2C_C & -C_C \\ 0 & -C_C & C_1 + C_C \end{bmatrix}.$$

The comparison of the transient response of crosstalk switching on victim line for three-coupled interconnect lines between the proposed MRTD method, HSPICE and the conventional FDTD method for two different test cases are illustrated in Fig. 6. It is observed that the proposed MRTD method is in good agreement with the HSPICE simulation results. From Figs. 6a and 6b it is also observed that a peak is resulted in the response using the conventional FDTD method due to its numerical dispersion properties. However, the proposed MRTD method with its great advantages in numerical dispersion properties [14]–[17] dominates over the conventional FDTD method with respect to accuracy. Table 5 presents the computational error involved in predicting the crosstalk induced 50 % delay on victim line due to aggressor lines using the proposed MRTD method and the conventional FDTD method with respect to HSPICE. Table 5 shows that the proposed model has an average error less than 1 %, whereas, the conventional FDTD method has an average error more than 3 %.

The elapsed CPU time for the proposed MRTD method, the conventional FDTD method and the HSPICE (W-Element method) is determined using the Intel Core i7 - 3770 CPU (3.40 GHz). Table 6 shows the corresponding elapsed CPU times of each method. It is observed that both MRTD and conventional FDTD methods are faster than HSPICE with respect to simulation time, conventional FDTD being slightly faster than the proposed MRTD, since it requires slightly more number of iterations than conventional FDTD. Therefore, there is a trade-off between accuracy and simulation time.

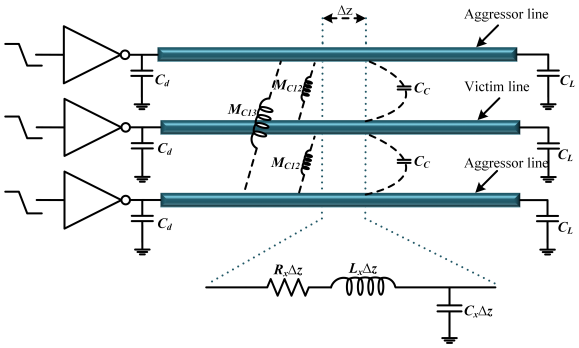
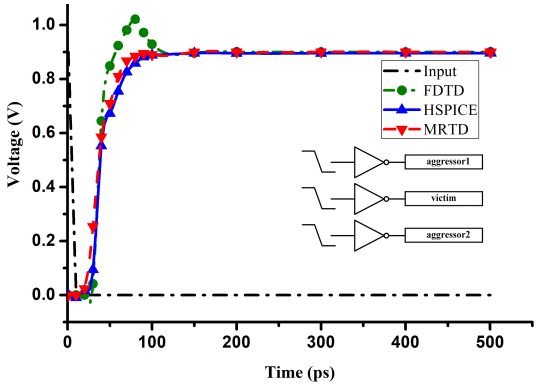
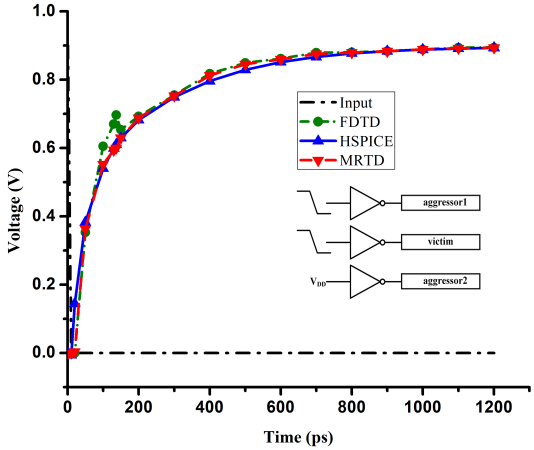


Fig. 5. Schematic of CMOS driven three-coupled interconnect lines.



(a)



(b)

Fig. 6. Crosstalk induced 50 % Delay analysis on victim line due to aggressor lines (a) test case-1, (b) test case-2 for three-coupled interconnect lines.

Input Switching Mode				50 % Delay [ps] on Victim line				
							% age error	
Test Cases	Aggressor line1	Victim line	Aggressor line2	HSPICE HSPICE	Proposed Model	conv.* FDTD	Proposed Model	conv.* FDTD
1	V_{DD} to 0	V_{DD} to 0	V_{DD} to 0	35	34.43	33.89	1.91	3.45
2	V_{DD} to 0	V_{DD} to 0	V_{DD}	66.088	66.88	64.2	-1.198	2.86

Tab. 5. Computational error involved for 50 % Delay on victim line of three-coupled interconnects (conv.*–conventional).

	Elapsed CPU time [s]		
Methods / No. of Coupled lines	HSPICE	MRTD	conv.* FDTD
Two	0.2466 ≈ 0.25	0.19035	0.1699 ≈ 0.17
Three	0.382	0.3061	0.2827

Tab. 6. Comparison of elapsed CPU time of the methods for two and three mutually coupled interconnects (conv.*–conventional).

4. Conclusion

An accurate model to analyze the crosstalk effects in coupled VLSI interconnects is proposed in this paper. The CMOS driver analyzed using the n^{th} power law model and coupled distributive RLC interconnects are modeled using the MRTD method. For different number of test cases, the proposed method shows an average error of 0.14 % and 1.9 % with respect to the peak crosstalk noise and the peak noise timing, respectively, compared to HSPICE results. For three-mutually-coupled interconnect lines, the average error for the proposed model is less than 1 % whereas the average error for the conventional FDTD method is more than 3 %. It is observed that the proposed MRTD method is in good agreement with HSPICE simulations and dominates the conventional FDTD method. Besides, the proposed MRTD method is more time efficient than HSPICE, although the elapsed CPU time of the proposed MRTD method is higher than the conventional FDTD method. Further, the proposed method is highly useful for precise estimation of crosstalk in the next-generation VLSI interconnects.

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