Wide Range High Precision CMOS Exponential Circuit Based on Linear Least Squares Approach

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Abstract. *A new strategy to implement exponential circuit in CMOS technology is presented in this paper. The proposed method is based on the new approximation function optimized by linear least squares approach to extend the output dynamic range. The current mode method is employed for realization of circuits, because of simple circuitry and intuitive topology. Unlike to the some reported circuits which were designed in the subthreshold region, the proposed design operates in the saturation region which provides acceptable bandwidth for the circuit. In order to validate the circuit performance, the post layout simulation results are presented using HSPICE and Cadence with TSMC level 49 (BSIM3v3) parameters for 0.18 µm CMOS technology. The results demonstrate 78 dB output dynamic range with the linearity error less than ±0.5 dB which shows a remarkable improvement in comparison with previously reported works. A bandwidth of 67 MHz, maximum power consumption of 0.326 mW under supply voltage of 1.5 V, and 0.77% error for temperature variations are further achievement of the design.*

Keywords

Exponential function, new approximation, analog circuit, high precision

1. Introduction

Computational circuits are important building blocks which are utilized in various applications in the field of signal processing. Exponential, logarithm, multiplication, division, squaring, square rooting are main functions which realize a multitude of circuits with a lot of applications. Multiplier and divider circuits are very useful in telecommunication circuits, fuzzy controllers and neural networks. Exponential (EXP) circuits are employed in medical equipments [1], hearing devices [2] or disk drives [3]. Squaring circuits represent the basic cell for realizing any continuous function, using function synthesizer circuits [4], [5]. Square rooting circuits are used in RMS to DC converters, function synthesizer and fuzzy systems [6].

Among these computational circuits, Exponential Function Generator (EXPFG) circuit is difficult to implement, because of its inherent nonlinear behavior. The importance of this function originates from the fact that it is utilized as a part of automatic gain controllers or variable gain amplifiers (VGA) [7], [8]. The most important aspects of EXPFG circuits include output dynamic range, linearity of the output in dB, accuracy, power consumption, and area efficiency. In the following, the literature review verified that most of the above mentioned parameters have a trade off with each other, and then different design techniques have been presented [10–21] to satisfy the compromise between the characteristics.

Considering the types of transistors, two groups of implementation using BJT and MOS transistors exist in the literature: the first approach is based on using exponential characteristic of bipolar transistor to obtain exponential function. The main drawback of using bipolar transistor is the nonzero value of the base current, and also its dependency to the temperature which causes large errors in the resulted exponential function [9]. The second group is based on the MOS transistor which employs exponential current-voltage characteristic of the transistor in subthreshold region. However, the poor circuit frequency response and narrow input dynamic range are the disadvantages of this method, which originates from very small drain currents for charging and discharging of the transistor parasitic capacitances [10–13].

Considering the mathematical techniques, three methods have been presented. The first group emphasizes on the use of expansion of the EXP functions using Taylor series [14], [15]. The main weakness of this method is given by the relatively small output dynamic range, because of neglecting superior-order terms in Taylor series. In the case of using higher-order terms, accuracy will be increased as well as the output dynamic range; however complex circuits with more silicon area are required. Therefore a trade-off between the overall circuit precision and the silicon area must be made.

The second group uses piecewise linear approximation method [16–18], which requires appropriate positioning of the breakpoints. The poor accuracy in the breakpoints as well as the complexity of the circuits are the disadvantages of this method. Also, another question is: where

and how many breakpoints should be selected. Although this problem has been examined in detail for sine function synthesis [19], there is no strategy for breakpoint selection of EXP function.

The third group deals with presenting new approximations of function in a limited range [14], [15], [20], [21] in which each term of the approximated series is realized using a voltage-mode [14], [15] or current-mode [20] circuits. The method presented in [14], [15] use pseudo-exponential functions which result in simple realization of the circuits and relatively low power consumption, however the precision and dynamic range have been sacrificed. Higher-order terms proposed in [20] benefit from higher dynamic range in comparison with above mentioned methods, at the cost of complex implemented circuits and lack of area efficiency which leads to increasing in power dissipation. Beside these classifications, designing the circuit with single power supply is preferred to those in dual mode; while the circuits reported in [7], [10], [13–15], [18], [19] require dual supply voltages. In conclusion, a circuit with wide dynamic range, high accuracy and low power consumption is expected as a further work. We introduced a method in [21] to satisfy these properties as well.

This paper proposes a new approximation for exponential function which significantly extends the dB-linear output dynamic range of the EXPFG circuit. The new function is obtained by using linear least squares approach to allocate optimum coefficient of a new fitted function on the EXP function. The resulted topology provides a 78 dB output range with the linearity error as low as ±0.5 dB, which demonstrates a significant improvement in comparison with the previously reported works. Unlike to the some reported circuits which were designed in the subthreshold region, the proposed configuration operates in the saturation region, thus provides acceptable bandwidth for the circuit. In addition, Monte Carlo analysis is performed to verify the robustness of the circuit against the process variation. Also, HSPICE and Cadence simulators are utilized to validate the theoretical formulations. The paper is organized in 6 sections: The proposed approach for implementation of EXP function is presented in Sec. 2, followed by the transistor level design of the proposed approximation in Sec. 3. In Sec. 4, post layout simulation results are presented to prove the efficiency of the design. The performance analysis of the circuit is presented in Sec. 5, and finally, conclusions are outlined in Sec. 6.

2. Proposed Approach

The proposed approach begins with presenting a new approximation formula for the exponential function as:

$$e^x \approx ax^4 + bx^2 + cx + d \tag{1}$$

where a, b, c and d are the coefficients and x is the independent variable. In order to avoid complex circuitry configuration, specific terms including x^4, x^2 and x as well as a constant value of d are only considered. In other words, the main difference in the proposed approximation rather than conventional approximations presented in [14], [18], [21] is simpler and more accurate realization in the CMOS technology. Moreover, in comparison with these works the input range of the resulted function is wider. The reason for choosing the above mentioned terms is that the term x^2 can be readily realized using a squarer (SQ) circuit, and two cascaded SQ circuits are used to provide the term x^4. Also the term x is directly generated through the input with proper gain as a coefficient.

It should be pointed out that in the exponential function circuits, there is a tradeoff between the accuracy and the input/output dynamic range; a narrow dynamic range results in higher precision, while a wide dynamic range usually decreases the accuracy of the circuit.

The objective of this paper is presenting a method to design a circuit which provides high precision performance as well as the wide input/output dynamic range. The proposed idea can be briefly explained as follows:

In order to increase the precision of EXP circuit, the input range (amplitude of the input signal) of the circuit is halved. In the next phase, the decreased signal range is compensated by squaring output signal. This means that in the first phase a high accurate circuit is implemented, and in the second, wide output range is expected. The overall procedure can be explained by the following equation:

$$e^x = \left(e^{0.5x}\right)^2 . \tag{2}$$

In the view of circuit realization, the structure consists of two stages; function of $e^{0.5x}$ is realized in the first stage, then the resulted output is applied to the SQ circuit such that the final circuit implements function of e^x.

The coefficients of polynomial in (1) are calculated using linear least squares optimization method which found as: $a = 0.01471$, $b = -0.3623$, $c = 2.306$ and $d = 0.1118$. In this regard, MATLAB *curve fitting* toolbox is employed. In the first step, the desired interval for the fitting is defined in the command window which is [0 9]. Secondly, the function for the mentioned interval is defined. In the next step, custom type of polynomials including coefficients and terms are defined which are *a, b, c* and *d* for coefficients and

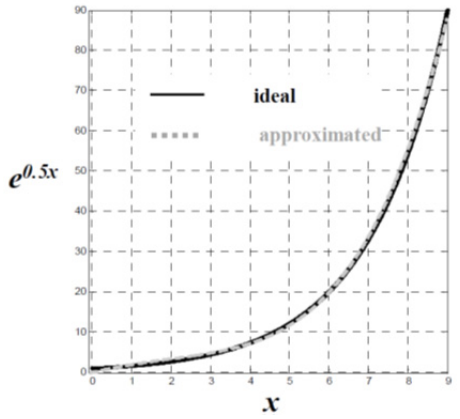

Fig. 1. Approximated EXP function using linear least squares method.

and x^4, x^2, x for terms. In the next step method of fitting is chosen which is linear least squares approach. Finally, the polynomial of ax^4+bx^2+cx+d is fitted on the exponential function in the defined interval and the optimized coefficients as well as the RMSE error are given. Therefore the final approximation formula for function of $e^{0.5x}$ is given by:

$$e^{0.5x} = 0.01471x^4 - 0.3623x^2 + 2.306x + 0.1118 \quad (3)$$

where $0 < x < 9$. In order to simple implementation of the above approximation, considering circuitry conditions, the following formula is derived:

$$e^{0.5x} = (0.348x)^4 - (0.602x)^2 + 2.306x + 0.1118. \quad (4)$$

The approximated curve (dashed line) and ideal exponential function (solid line) are shown in Fig. 1.

3. Circuit Description

The design procedure of the circuit begins with the selection of bias current of 10 μA as a normalized current. The main building block which is employed in the EXPFG circuit is current squaring circuit shown in Fig. 2(a). Consider a loop of MOS transistor *M*1 to *M*4; writing KVL in the gate-source voltages of these transistors yields:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4}. \quad (5)$$

Since all transistors are biased in saturation region, then $V_{GS} = V_t + \sqrt{\frac{I_D}{K}}$; Replacing in (5) and assuming that transconductance parameter and threshold voltage of all transistors are well matched, we have:

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}}. \quad (6)$$

Deriving currents of I_{DS3} and I_{DS4} by KCL at nodes A and B:

$$I_{DS3} = I_{SQ} + I_{in}, \quad (7)$$

$$I_{DS4} = I_{SQ} - I_{in} \quad (8)$$

where I_{in} and I_{SQ} represent input and squaring currents, respectively.

Since $I_{DS1} = I_{DS2} = I_B$, (I_B is the bias current) substituting (7) and (8) into (6) and then squaring both sides twice, the output of the circuit can be derived as:

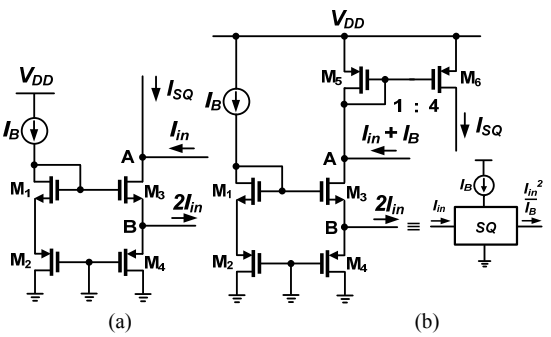

Fig. 2. Current-mode SQ circuit: (a) presented in [22], (b) modified circuit.

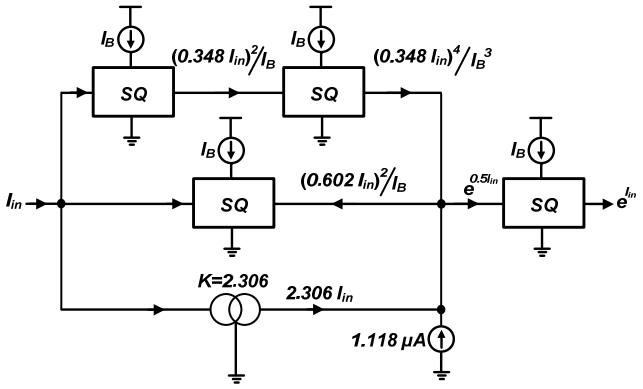

Fig. 3. The proposed block diagram for implementation of EXPFG.

$$I_{SQ} = \frac{I_{in}^2}{4I_B} + I_B. \quad (9)$$

It can be clearly seen that the squaring of input current is obtained at the output. Also, the bias current of I_B is considered as a normalized current.

In order to simple using of SQ circuit, it is better to consider the output current as I_{in}^2/I_B. Therefore, the modified circuit of Fig. 2(b) is presented to provide the required function. This can be readily done by applying $I_{DS3} = I_{SQ}/4 + I_{in} + I_B$ and $I_{DS4} = I_{SQ}/4 - I_{in} + I_B$. Following the above procedure, the desired output is obtained.

The proposed block diagram for implementation of EXPFG circuit is shown in Fig. 3. The term of $(0.348x)^4$ is implemented in the upper branch by cascading two SQ circuits in the circuitry form of $(0.348I_{in})^4/I_B^3$. The middle branch realizes $(0.602x)^2$ in the form of $(0.602I_{in})^2/I_B$ using single SQ circuit. The next branch realizes linear term of approximation which composed of a current mirror with the gain of 2.306, and finally, the DC current source implements the constant term of 1.118 μA. Take notice that since the circuit is designed in the current mode, current mirrors with defined gains are employed to realize coefficients of (4), (*a*, b, c and *d*).

4. Post Layout Simulation Results

In this section, HSPICE and Cadence simulators are utilized to prove the performance of the circuit for 0.18 μm CMOS technology. The layout pattern of the EXPFG circuit drawn by Cadence is depicted in Fig. 4 which verifies that the circuit can be realized in 75 μm × 43 μm active area. Figures 5 and 6 demonstrate HSPICE results of the circuit in the exponential form ($e^{0.5I_{in}}$) and linear mode, respectively, which shows an output range of 38 dB. It is compared with the ideal output which is confirmed by simulation results obtained by HSPICE. The error measurement is shown to validate the precision of the circuit in which the average of error is 0.16 dB. As discussed, in order to have higher accuracy, in the second phase by squaring $e^{0.5I_{in}}$ the full exponential function ($e^{I_{in}}$) is generated. Figure 7 shows the exponential output of the circuit in the form of $e^{I_{in}}$ with 78 dB output dynamic range. In addition,

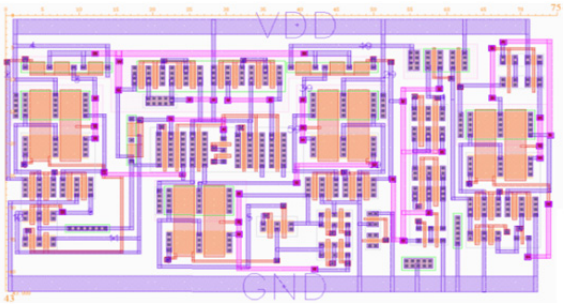

Fig. 4. Layout pattern of the proposed EXPFG circuit.

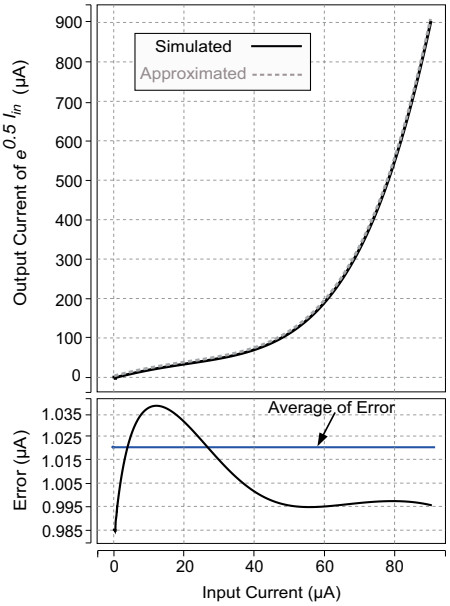

Fig. 5. HSPICE simulation result for $e^{0.5I_{in}}$ function.

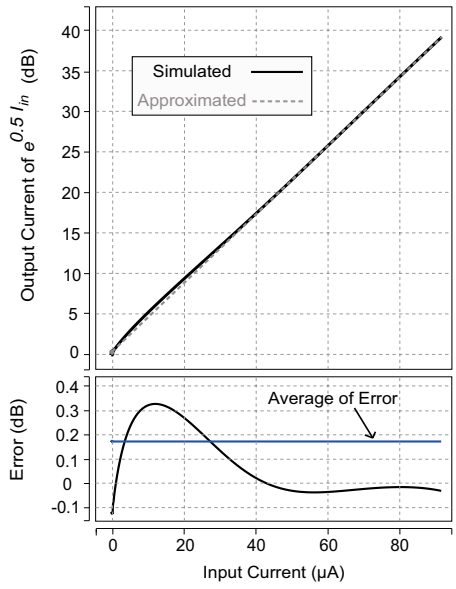

Fig. 6. HSPICE result of $e^{0.5I_{in}}$ in dB scale.

the average error of 0.29 dB shows a highly accurate performance of the circuit.

To prove the efficiency of the circuit, frequency response is provided. Since some reported works work in subthreshold region [10–13], and some others have complex structure [11], [15], [21], thus their bandwidth is limited, while in this work all of the transistors are biased in the saturation region. Frequency response of the EXPFG circuit in Fig. 9 demonstrates that –3dB bandwidth is 67 MHz. In order to calculate –3dB bandwidth of the circuit, the input

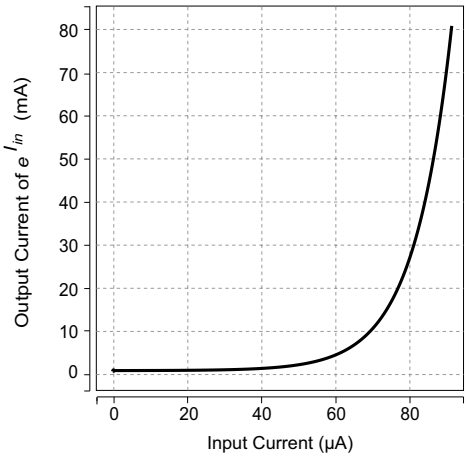

Fig. 7. HSPICE simulation result for $e^{I_{in}}$ function.

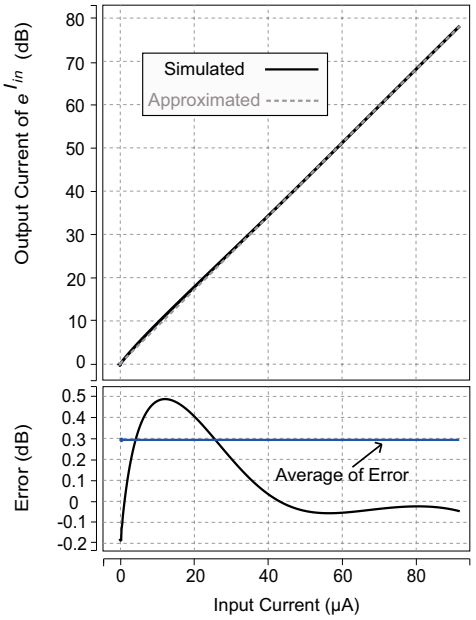

Fig. 8. HSPICE simulation result of $e^{I_{in}}$ in dB scale and its error measurement.

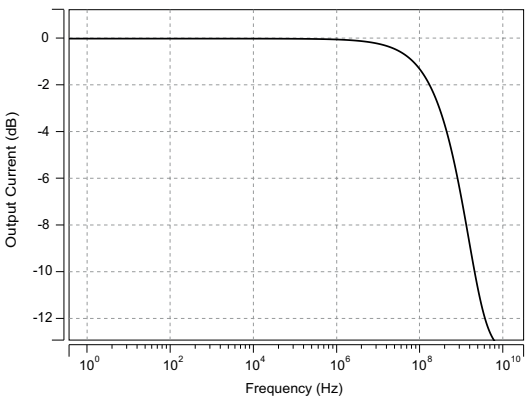

Fig. 9. Frequency response of the EXPFG circuit.

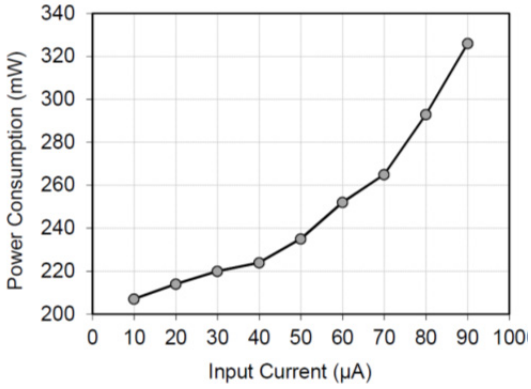

Fig. 10. Power dissipation of the proposed circuit versus different input currents.

signal is set to the value that the output current be 1 dB, and then the frequency in which the gain is –3 dB is calculated.

Figure 10 illustrates the power consumption of the EXPFG circuit for different input currents. As expected, the power dissipation is increased when the input current increased. The maximum power consumption is obtained 0.326 mW with the input current of 90 μA, while the average of power consumption is found as low as 0.248 mW.

5. Error Analysis in the Circuits

The error analysis of EXPFG circuit is examined in this section. Considering (1), the main error sources originate from terms of x^2 and x^4, which are implemented by SQ and two cascaded SQ circuits, respectively. As discussed, SQ circuit is designed using translinear loop, which was considered in an ideal form, and then (5) was derived, while the body effect was ignored. In a MOS transistor body effect is given by:

$$V_t = V_{t0} + \gamma\left[\sqrt{\left(2\phi_b + |V_{SB}|\right)} - \sqrt{2\phi_b}\right]. \tag{10}$$

Since bulk of transistors M_2 and M_4 are connected to the source terminal, therefore $V_{SB} = 0$ and then $V_t = V_{t0}$, while in M_1 and M_3 transistors $V_{SB} \neq 0$. Supposing the probable mismatch for transistors M_1 and M_3 as:

$$V_{GS1} = V_{t1} + \Delta V_1, \tag{11}$$

$$V_{GS3} = V_{t3} + \Delta V_3. \tag{12}$$

Substituting (11) and (12) into (5) yields:

$$V_{t1} + \Delta V_{1_1} + V_{GS2} = V_{t3} + \Delta V_3 + V_{GS4} \tag{13}$$

where $V_{t1} = V_t + \delta$, $V_{t3} = V_t - \delta$ and δ is the mismatch value among V_{t1} and V_{t3}.

Considering $I_B = K\Delta V^2$ then by some algebra, the output current can be written as:

$$I'_{out} = \frac{I_{in}^2}{4K\Delta V\left(\Delta V + 2\delta\right)} + \frac{K\Delta V\left(\Delta V + 4\delta\right)}{1 + \dfrac{2\delta}{\Delta V}}. \tag{14}$$

Subtracting (14) from (9), and ignoring high-order terms containing ΔV^n ($n = 3,4,5$) and also δ^2, error of the SQ circuit is derived:

$$\left|I'_{error}\right|_2 = \frac{\delta}{2K\Delta V^2} I_{in}^2 + 4K\delta\Delta V^2. \tag{15}$$

where $|I'_{error}|_2$ is the error of SQ circuit. The same analysis is simply carried out for two cascaded SQ circuits which results in the error as:

$$\left|I'_{out}\right|_4 = \frac{I_{in}^4(1+2\delta) + 8\delta I_B^2 I_{in}^2}{I_B^3(1+2\delta+\dfrac{4\delta^2}{\Delta V^2})} + \frac{4K\delta\Delta V - \dfrac{2\delta I_B}{\Delta V}}{1+\dfrac{2\delta}{\Delta V}}, \tag{16}$$

$$\left|I'_{error}\right|_4 = \frac{\dfrac{4\delta^2}{\Delta V^2}(I_{in}^4) - 8\delta I_B^2 I_{in}^2}{I_B^3(1+2\delta+\dfrac{4\delta^2}{\Delta V^2})} - \frac{4K\delta\Delta V - \dfrac{2\delta I_B}{\Delta V}}{1+\dfrac{2\delta}{\Delta V}} \tag{17}$$

where $|I'_{error}|_4$ is the error of two cascaded SQ circuits. Considering (15) and (17), the mismatch error for threshold voltages can be neglected as long as:

$$\Delta V \gg 2\delta,\ \Delta V \gg 4\delta,\ 1 \gg \frac{2\delta}{\Delta V}. \tag{18}$$

Replacing (15) and (17) into (3), the error quantity for EXPFG circuit is computed as follows:

$$I'_{error} = 0.0147(\left|I'_{error}\right|_4) - 0.3623(\left|I'_{error}\right|_2). \tag{19}$$

This equation implies that the error of two individual blocks are subtracted, thus the error at the output of EXPFG circuit is smaller than the errors in each SQ and two cascaded SQ circuits. Also, the coefficients of errors are less than 1 (0.0147 and 0.3623). This means that each resulted error is reduced which in turn degrades the overall error of the circuit. In order to verify this analysis and also to evaluate circuit robustness against the process variation, the Monte Carlo statistical analysis is carried out taking ±5% Gaussian distribution in the variation of transistors threshold voltage. The simulation results are shown in Fig. 11 where 64% of the occurrences lead to the error less than ±1%, while 13% of samples occurred with the error more than ±2%. Take notice that to calculate the error, output current (not ideal output) is compared with those obtained by Monte Carlo analysis. To prove the high linearity of the proposed circuit in dB against the process tolerances, the same analysis with the similar conditions of previous simulation is performed. The simulation results are shown in Fig. 12, and demonstrate that 84% of the samples have the error of less than ±0.6 dB, and just 6% of the occurrences lead to the error of more than ±1 dB. Also, the mismatch of the transconductance parameter can be modeled as follows:

$$\begin{aligned} K_P &= K + \Delta kK, \\ K_N &= K - \Delta kK \end{aligned} \tag{20}$$

where K is a mean value and Δk is a mismatch percentage of the parameter. Assuming this, (6) becomes:

$$\sqrt{\frac{I_{\mathrm{B}}}{K+\Delta kK}}+\sqrt{\frac{I_{\mathrm{B}}}{K-\Delta kK}}=\sqrt{\frac{I''_{\mathrm{out}}+I_{\mathrm{in}}}{K+\Delta kK}}+\sqrt{\frac{I''_{\mathrm{out}}-I_{\mathrm{in}}}{K-\Delta kK}} \quad (21)$$

where I''_{out} is the output of the squaring circuit. Simplifying (21) and ignoring terms containing Δk^2 (because $\Delta k \ll 1$), output current of squarer circuit can be written as:

$$I''_{\mathrm{out}} \approx \frac{{I_{\mathrm{in}}}^2+\Delta kI_{\mathrm{in}}}{4I_{\mathrm{B}}+2\Delta kI_B I_{\mathrm{in}}}. \quad (22)$$

Subtracting (22) from (9), following the same procedure of above mentioned mismatch for threshold voltage, then by some algebra one can find the error quantity for SQ, cascaded SQ and EXPFG circuits as follow:

$$\left|I''_{\mathrm{error}}\right|_2=\frac{{I_{\mathrm{in}}}^2+4\Delta kI_{\mathrm{B}}I_{\mathrm{in}}}{I_{\mathrm{B}}+2\Delta kI_{\mathrm{in}}}, \quad (23)$$

$$\left|I''_{\mathrm{error}}\right|_4=\frac{2\Delta kI_{\mathrm{B}}{I_{\mathrm{in}}}^4-\Delta k^2{I_{\mathrm{B}}}^2{I_{\mathrm{in}}}^2-4\Delta kI_{\mathrm{B}}}{1+2{I_{\mathrm{B}}}^2+4I_{\mathrm{B}}I_{\mathrm{in}}\Delta k-I_{\mathrm{in}}\Delta k^2-I_{\mathrm{B}}I_{\mathrm{in}}\Delta k^4}. \quad (24)$$

Replacing (23) and (24) into (3), the error quantity for EXPFG circuit is computed as:

$$I''_{\mathrm{error}}=0.026\left(\left|I''_{\mathrm{error}}\right|_4\right)+0.147\left(\left|I''_{\mathrm{error}}\right|_2\right). \quad (25)$$

Considering that the coefficients in (25) as well as $|I'_{\mathrm{error}}|_4$ and $|I'_{\mathrm{error}}|_2$ are less than one, we can ignore the mismatch of transconductance parameters. The Monte Carlo analysis is also carried out for this parameter in variation of aspect ratio of the transistors (considering $K = 0.5\mu_0 C_{\mathrm{OX}}$ (W/L)). The result is shown in Fig. 13. For channel length modulation effect, it is well known that, for long channel MOS transistors, the perfect square-law equation agrees with experimental results to a great extent [24], and since channel length for the core circuit (squaring circuit) is 3.8 μm, therefore, this effect can be negligible.

Another factor which affects the circuit performance is temperature variation which originates from dependency of the threshold voltage in CMOS circuits to the temperature. Considering the threshold voltage of MOS transistor as:

$$V_{\mathrm{T}}=\phi_{\mathrm{ms}}-\frac{Q_{\mathrm{ss}}}{C_{\mathrm{ox}}}+2\phi_{\mathrm{F}}+\gamma\sqrt{2\phi_{\mathrm{F}}} \quad (26)$$

where $\phi_{\mathrm{ms}} = \phi_\Gamma \ln(N_{\mathrm{A}}N_{\mathrm{G}}/{n_{\mathrm{i}}}^2)$ is the contact potential difference between gate and substrate, N_{G} and N_{A} are the gate and substrate doping levels, respectively and n_{i} is the intrinsic electron-carrier concentration of Si, Q_{ss} the surface-state charge density per unit area, and C_{ox} the oxide capacitance; γ is a body effect parameter and $\phi_{\mathrm{F}} = \phi_\Gamma \ln(N_{\mathrm{A}}/n_{\mathrm{i}})$ is the Fermi potential of substrate with the thermal voltage of $\phi_\Gamma = kT/q$. In the above equation, both of ϕ_{ms} and ϕ_{F} depends on ϕ_Γ, and are only parameters which depend on threshold voltage ($\partial V_{\mathrm{T}}/\partial T$) which can be written as [23]:

$$\frac{\partial V_{\mathrm{T}}}{\partial T}=\frac{\partial\phi_{\mathrm{ms}}}{\partial T}+2\frac{\partial\phi_{\mathrm{F}}}{\partial T}+\frac{\gamma}{\sqrt{2\phi_{\mathrm{F}}}}\frac{\partial\phi_{\mathrm{F}}}{\partial T}. \quad (27)$$

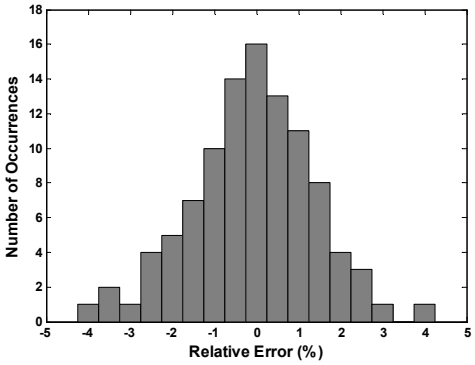

Fig. 11. Monte Carlo analysis of EXP circuit for relative error.

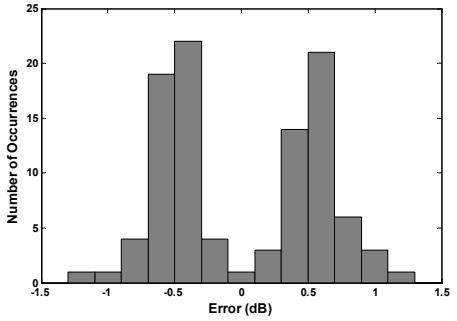

Fig. 12. The result of Monte Carlo analysis against the process variation to prove the linearity of the circuit.

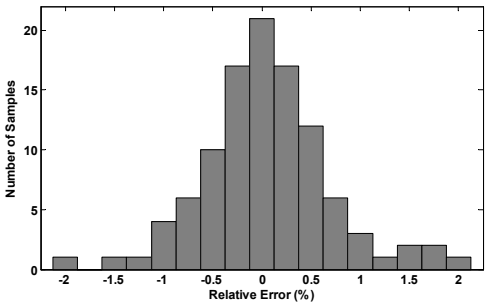

Fig. 13. Monte Carlo analysis for mismatch in transconductance parameters in EXPFG circuit.

In order to examine the performance of EXPFG circuit versus temperature tolerances, SQ circuit which is the main block in EXPFG as well as the current mirrors are discussed separately: In the current mirror circuits, corresponding transistors carry equal drain-to-source currents because of equal voltages of V_{GS} and V_{DS}. Since these voltages of corresponding transistors are equal in all conditions, any variations in threshold voltage are automatically compensated. Thus, the performance of the circuit does not depend for the probable temperature tolerances. Regarding SQ circuit, the output formula demonstrates dependency to the threshold voltage. As we discussed, the circuit is based on the translinear principle which obtains from a loop of gate-to-source voltages. Considering (15) and (17), this voltage is affected by threshold voltage and consequently by temperature variation. One can see the effect of threshold voltage at the output current by δ parameter:

$$I'_{\mathrm{out}}=\frac{{I_{\mathrm{in}}}^2}{4K\Delta V(\Delta V+2\delta)}+\frac{K\Delta V(\Delta V+4\delta)}{1+\dfrac{2\delta}{\Delta V}}. \quad (28)$$

Considering (28), δ is very small in comparison with constant voltage of ΔV which is proportion of bias current. Therefore, it is negligible in the terms of $(\Delta V + 2\delta)$ and $(\Delta V + 4\delta)$. Accordingly, in the term of $(1 + 2\delta/\Delta V)$, δ is divided to ΔV which is very large. On the other hand, the concluded value is added to 1.

As a result, threshold voltage tolerances caused by temperature variation do not notably influence the performance of the main building block e.g. SQ circuit. For the complete circuit the simulation is carried out and shown in Fig. 13, where the relative error of the circuit versus temperature validates the robustness of the EXPFG circuit against temperature variations. In this simulation, output of EXPFG at 20°C is supposed as the non-error output, and then the circuit is simulated in different temperatures. The results show that the maximum error occurred at –40°C with 0.77% error.

For channel length modulation effect, it is well known that, for long channel MOS transistors, the perfect square-law equation agrees with experimental results to a great extent [24], and since channel length for the core circuit (squaring circuit) is 3.8 µm, therefore, this effect can be negligible. In order to show the applicability of the proposed EXP circuit, it is used to realize a dB-linear variable-gain amplifier (VGA) shown in Fig. 15, an important application in radio engineering field [25], [26]. The proposed VGA employs the exponential characteristic realized in Fig. 3 and also a multiplier/divider which is implemented based on the circuit of Fig. 1 using square-difference algebraic identity: $(x+y)^2-(x-y)^2=4xy$. Therefore using two squaring circuits and one subtractor, the desired output using (9) is derived as:

$$I_{\text{out(VGA)}} = I_{\text{out2(VGA)}} - I_{\text{out1(VGA)}} = \frac{I_{\text{out(EXP)}}}{I_{\text{B}}} I_{\text{in(VGA)}} \quad (29)$$

where I_{B} is the reference current, $I_{\text{out(EXP)}}$ represents the output current of EXP circuit, having the output current explained in Fig. 3 ($I_{\text{B}} \exp(I_{\text{in}}/I_{\text{B}})$), while $I_{\text{out(VGA)}}$ expresses the output current of the dB-linear VGA circuit. Then, by replacing $I_{\text{B}} \exp(I_{\text{in}}/I_{\text{B}})$ in (29) the output is given by:

$$I_{\text{out(VGA)}} = \exp\left(\frac{I_{\text{in}}}{I_{\text{B}}}\right) I_{\text{in(VGA)}} = G I_{\text{in(VGA)}}. \quad (30)$$

Thus, the gain G of VGA circuit can be exponentially tuned by current of I_{in} through the EXP circuit.

Table 1 summarizes the related results of EXPFG circuit and allows a deeper comparison. Ref. [10] benefits from high dB gain, but it needs double power supply, and also its bandwidth and output range are limited to 0.105 MHz and ±48 dB respectively, while our proposed circuit range is 0 to 78 dB. Note that Refs. [7] and [10] have been designed in weak inversion, thus their power consumption is low. As seen their bandwidth is narrow, and also they use double power supply. Ref. [15] benefits from lower power dissipation and acceptable precision, but they suffer from low bandwidth and poor output dynamic range. Ref. [21] has a good performance in output dynamic range and power consumption, but its accuracy is comparatively low. In fact, we sacrificed the power consumption by implementing higher-order terms at the cost of more accuracy. In addition, its bandwidth is as low as one-half of the proposed circuit.

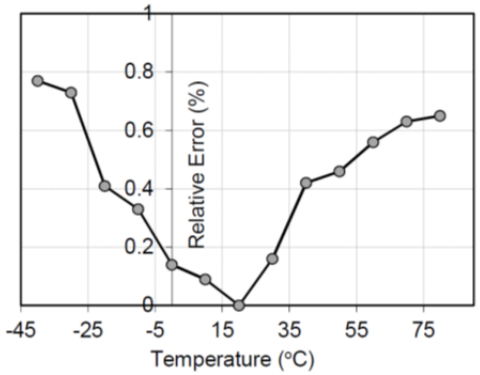

Fig. 14. Relative error of EXPFG circuit versus different temperatures.

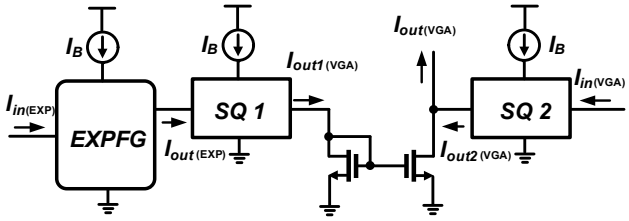

Fig. 15. VGA implementation using designed EXP circuit.

Ref.	Gain (dB)	Accuracy (Error in dB)	BW (MHz)	Supply (V)	Power (mW)	Tech. (µm)
[7]	71	0.3	0.181	± 0.75	0.013	0.35
[10]	96	±0.5	0.105	± 0.75	0.0063	0.35
[11]	48	±0.5	3	1.8	0.549	0.18
[12]	40	±0.75	NA	1.5	0.6	0.35
[15]	66	±0.5	31	± 0.75	0.17	0.18
[16]	41	±1	168.8	2.5	0.535	0.13
[20]	70	±1	32	1	0.08	0.18
Proposed	78	≤ ±0.5	67	1.5	0.326	0.18

Tab. 1. Comparative parameters of the proposed circuit with other recent works.

6. Conclusion

In this paper, a new CMOS exponential circuit has been presented. The proposed circuit enjoyed these attractive features: 1) Presenting a new approximation for exponential function in the defined range. 2) Extending output dynamic range by proposing cascaded stages up to 78 dB. 3) Obtaining very accurate performance with average error less than 0.3 dB. 4) Achieving satisfactory bandwidth resulted from current-mode realization which provided simple and intuitive configuration 5) Demonstrating acceptable performance against the process variation.

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