# Integrated M-Sequence Based Transceiver for UWB Sensor Networks

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**Abstract.** This paper deals with the realization, measurements and testing of an integrated UWB radar head operating in the continuously transmitted stimulation signal mode. The term UWB is derived from the exploited system bandwidth. Practically, the frequency bands nearly from DC to 14 GHz or those specified by the Electronic Communication Committee (ECC) or the Federal Communications Commission (FCC) regulations are used. The stimulation signal is generated by modulation of the carrier by a binary sequence which spreads the frequency spectrum of the signal. Thanks to the parameters of the resulting signal, it is not the source of interference for other radio services, but it can be observed only as an increase in noise. In the context of the UWB radars emitting the spread-spectrum signal, the term noise radar is often used, where the generated spreading signal is the result of generation of a pseudorandom noise modulation signal. The principle of generation of such a signal as well as the description of the transmitter is described in this article in more details. The reception of the UWB signals is not a trivial task. Hence in this paper, we deal with the topic of the UWB radar transceiver, relying on the equivalent time sampling approach, with attention to the receiver section. The measurements focused on qualitative parameters of the given UWB radar are evaluated as well, concentrating on the innovative integrated front-end. The main tested parameters include reliability across the whole frequency range, dynamic range, as well as crosstalk in the proposed structure.

## Keywords

UWB Radar, M-Sequence, transceiver, ASIC

## 1. Introduction

UWB radar represents a modern, sophisticated and powerful device designed for non-destructive measurement methods based on electromagnetic waves [1]. Devices of this kind are generally used for short-term as well as long-term surveillance measurements exploiting the methods of remote sensing [2]. The UWB radar can be used either as a stand-alone device or a so called UWB sensor network may be realized [3]. Before the measurement is started, certain parameters which influence the measurement results have to be adjusted. It is necessary to know the minimum dimensions of the scene under test, the distance between the antennas, as well as the parameters of the UWB radar system itself [4].

The measurements may be carried out in the indoor as well as in the outdoor environment. The device setting, calibration and testing require significant effort and time. The solution presented in this paper assumes exploitation of the integrated progressive hand-held UWB radar (device), which will be able to carry out the measurement almost instantaneously, not only as a stationary, but as a dynamic as well, e.g. using drones or other moving platforms. As an example, searching for people trapped by an avalanche [5], or in other situations [6], can be mentioned, where the different view on the given situation is crucial to decide for the optimal solution. When it comes to the mobile device, the power consumption has to be considered. Therefore, the concept of the integrated UWB radar has to count with battery or solar power supply. More on that is discussed in Sec. 4. For that purpose, the novel UWB transmitter was realized with higher resolution and better spectral efficiency. However, its disadvantage is either a drastically increased requirement on the transport of the impulse responses (IRF) to the control PC, or reduction of the measurement speed in IRF/s.



Fig. 1. Block diagram of the conventional UWB radar equipped by two receivers.

In Fig. 1, a general block diagram of the UWB radar is shown. It consists of one stimulation signal transmitter and corresponding receiving circuits. Dependent on the final application, the UWB radars can be equipped with a single receiver (1Tx 1Rx) - power consumption and cost-oriented applications; two receivers (1Tx 2Rx) - applications in 2D localization [7] and ranging, or in special cases the radars can be equipped by multiple receiving channels (pseudo MIMO). The two-channel receiver configuration is often an appropriate compromise even in the case of impedance spectroscopy application where the first channel is attached to the probe in contact with media under test (MUT) while the second channel is used as a reference for real-time calibration. A special group of UWB radars includes the applications where several transmitters and receivers are necessary, for example for 3D localization and ranging [8]. From the power efficiency and active chip area usage point of view, the UWB node configuration with a single transmitter and a single receiver seems to be an interesting alternative to the systems with 1Tx 2Rx nodes. To use the UWB nodes in the MIMO configuration [9], it is necessary to synchronously control the transmitting as well as the receiving circuits, which is a challenge for design and realization of accurate timing circuits, e.g. for measurement start. This paper deals with the integration of the RF circuits of the UWB radar into a single monolithic structure with regards to the previous versions of UWB radars. The goal is to enhance the existing chipset and enable better adaptability in practical usage, for example in the case of sensor networks. The Section 2 is dedicated to the integration itself. In Sec. 3, the concept of the monolithic structure is described as well as the overall design and capabilities of the chosen semiconductor technology. In Sec. 4, the manufactured circuits are characterized. Finally, pros and cons of our experimental results are summarized in the conclusion.

## 2. Theoretical Background and System Integration

Recently, we have been dealing with integrating of the blocks of UWB radar head into the single integrated structure. This process is one of the most challenging hardware implementations ever. It was necessary to solve the problem of the integration of the whole system (receiver, transmitter, synchronization circuits), impedance matching of the inputoutput ports, total energy consumption, efficient component placement on the chip and many other tasks until the required results were obtained. Integrated, or monolithic, systems on a chip (SoC) have become a frequently discussed topic in many scientific contributions. In the case of hardware development, it is one of the most challenging processes. Modern progressive tools and methods for system integration or integrated structures realization, especially dealing with mixed analog-digital circuits, are continuously improving by the development of new powerful technologies. One of such tasks is the design of the new integrated UWB radar based on the mixed structure in the form of an ASIC (application-specific integrated circuit).

From the UWB radar parameters given above, the most important is its operational bandwidth which is very wide compared to devices continuously emitting electromagnetic waves. UWB systems described in this contribution exploit typically a bandwidth B, given by the carrier frequency  $f_C$  as follows:

$$B = f_{\rm C}/2. \tag{1}$$

With the increase of frequency, unexpected dependencies may occur, especially in the case of wideband RF structures. The analogue, as well as mixed ASIC circuits [10], are influenced mainly by noise, crosstalk and delays [11], [12].

The signal modulated by the pseudorandom bit sequence used in this type of UWB radars has significant wide frequency band. Therefore, the so called switching noise often occurs in the process of generating such a signals. The methods of switching noise reduction have to be taken into account. An example of those methods is the usage of balanced current steering topology [13]. This method is based on an approach of using the differential structures always is possible. Therefore, the presented monolithic structure is fully differential. The transmitter, as well as the receiver, are equipped with the differential I/O ports, regardless if they serve as a clock, control or RF interfaces. In the case of the clock signal, a balun is placed directly at the input port and the signal is routed differentially thereafter. Exploiting the differential structures ensures stability and minimizes sensitivity to interference of all internal blocks of the transmitter and the receiver. These methods successfully eliminate the intermodulation distortion as well.

## 3. Monolithic Structure of UWB Radar

The overall structure of the integrated analogue UWB radar head is depicted in the block diagram in Fig. 2. The proposed and realized the idea is based on the adapted and simplified conventional UWB radar concept from Fig. 1. During the integration process, the transmitter circuits have been redesigned and replaced by the latest generation of the 15-bit M-sequence generator. The transmitter block was enhanced by the clock signal control as well. The main reason is to allow the operation in a multi-channel system [14] and to interconnect the devices to create sensor networks in combination with other sensors [3], [15]. As an example, applications requiring functionally-safe non-optical high-resolution 3D sensing for autonomous robots can be mentioned, designed for operation in unknown environments. Creation of the necessary hardware basis contributes to the penetration of the robotics into the new fully automated activities and services with the emphasis on safety. The core concept is the fusion of partially redundant information from various types of sensors (ultrasonic, stereo-optical, RF, mechanical, etc.) aimed at the assurance of the highest possible safety for humans even in the case of malfunction of one or more networked sensors of either the same or a different type.



Fig. 2. Block diagram of the UWB radar integrated structure (SoC).

From the UWB localization and imaging point of view, one of the solutions is to place multiple 1Tx1Rx UWB nodes on a moving platform. Regarding the costs, it is necessary to mitigate the need for RF cables in this case. Therefore, the autonomous driving of each node by the clock signal and synchronous stimulation signal generation control is required. In the proposed structure, the whole process is carried out by the low voltage differential signals (LVDS). This solution was chosen for its compatibility with available components, for example a digital communication unit which is equipped by the LVDS interface as well. The communication unit includes an FPGA module operating in the role of communication interface as well as performing computations for raw radar data preprocessing.

The proposed monolithic structure includes the wideband receiver circuits as well. Because the transmitted signal has specific characteristics, the digitalization is preceded by primary signal preprocessing. Here, the equivalent time sampling is used [1]. The sampling is carried out by a wideband sampling block consisting of receiving circuits (low noise Cherry-Hooper amplifier [16]), the sampling core itself, and the input and output buffers for data transfer between the input block and the digital part of the receiver. More on the sampling principle is discussed in Sec. 4.

The transmitter and the receiver are interconnected via the synchronization unit. It is a substantial system element, because of the highly accurate synchronization between the transmitter and the receiver is the key parameter for correct signal processing. The synchronization unit consists of an ultra-fast binary divider, whose core is created by a shift register.

#### 3.1 AMS Process Technology and ASIC Prototyping

All circuits used in the analog part of the UWB radars, as well as the proposed concept, are built on the ASIC platform. The ASIC service is offered by a chip foundry as support for universities and other research institutions. This design was realized in the 0.35 µm SiGe BiCMOS (S35D4) technology supplied by AMS, Austria. This process allows the realization of mixed analog-digital structures on a single chip. Another parameter important for the RF design is the transit frequency  $F_t$ = 70 GHz, availability of four metal layers, support for 3.3 V supply voltage for CMOS and high voltage bipolar junction transistor (HBT) as well as an option to use 5 V HBTs. The noise parameters of the given technology are sufficient for wideband applications as well.

## 4. Measurement Approach

As the output of the Multi Project Wafer program, only bare dies of the proposed UWB radar were available. Therefore, they were measured at the microprobe testing station at first. By this approach, the basic functionality of the components of the transmitter and the receiver can be verified. Detailed view on the measurement fixture is shown in Fig. 3.

The photograph of the UWB radar die is shown in Fig. 4. For extended measurements, the development kit was designed and manufactured (Fig. 13), and the dies were packaged. The development kit employs two UWB radar chips – one as the receiver and the other as the transmitter.



Fig. 3. Detail of microprobes attachment to the proposed UWB radar die.



Fig. 4. Bare die of the proposed UWB radar.

Basic technical parameters of the proposed integrated structure are as follows:

- overall power consumption 1.6 W, (TX 790 mW and RX 810 mW);
- used clock frequency nearly from DC up to 14 GHz;
- RF output power up to  $-7 \, \text{dBm}$ ;
- 1 dB compression point -7.9 dB.

# 4.1 Measurement of Basic Parameters on the Die

The basic elements of the receiver connected in cascade create a two-port network characterized by its parameters. The important parameters from the linearity point of view are gain compression and intermodulation distortion. The gain compression is expressed by the 1 dB compression point.

The comparison of the measured and the simulated results for 1 dB compression point of the sampling circuits is shown in Fig. 5. From the figure, the difference between the simulation and the measurement is obvious. It can have several reasons, from simulation setup and component models up to manufacture, assembly, die packaging and PCB design deviations. However, the obtained result is fully sufficient for the needs of received UWB radar signals processing because the power density of the spectral components, as well as the signal level itself is very low. The power of the signal reflected to the receiver is in the range of  $0.35 \,\mu$ W.

An important parameter of amplifiers is their bandwidth. In our case, the bandwidth of the whole receiver was measured and simulated, from analog wideband input to narrowband output (Fig. 7). In Fig. 6 the simulation and measurement results are shown.

The measurement of the realized receiver was taken directly at the monolithic structure, eliminating the influence of bonding wire inductances between the die and the IC package. The simulation data show that the frequency bandwidth of the receiver output would be about 1 GHz. The measurement revealed the 3 dB signal attenuation already at about 700 MHz. This value is sufficient for processing of the radar signals, as the maximum frequency of the subsampled signal is 25 MHz if 13.82 GHz clock frequency is used for the M-sequence generation. The frequency of the subsampled signal is given by the ratio of the binary divider included in the synchronization unit (Fig. 2).

On the facts given above, we may conclude that the receiver circuits belong into the group of circuits which transform the signal bandwidth between the input and the output. The input signal (units to tens of GHz) is transformed into the signal with a bandwidth of a few MHz to be processed by the A/D converter.

The frequency of the receiver output signal depends on the clock frequency of the control signals driving the sampling circuits. As the sampling circuit, an amplifier featuring high current gain and the high input impedance is employed. These properties are important particularly during the sampling process when the hold capacitor  $C_H$  is charged to serve as the signal source in the hold mode. The simplified block diagram of the receiver circuitry is presented in Fig. 7. From the mode of operation of the sampling circuits, it is obvious that the stroboscopic sampling, or equivalent time sampling, is used (Fig. 8).

The time domain signal after the equivalent time sampling process is shown in Fig. 11. This method may be applied only to periodic signals. The generated stimulation signal is the pseudo-random M-sequence. At the first glance, the generated sequence looks like a random signal, but a comprehensive analysis reveals that it has certain period given by parameters of the transmitter (order of the M-sequence generator shift register).



Fig. 5. Comparison of measured and simulated results for 1 dB compression point of sampling circuits in sampling mode.



Fig. 6. AC response of the sampling circuits of the receiver operated in sampling mode.



Fig. 7. The simplified block diagram of the receiver topology.



Fig. 8. The timing diagram of the equivalent time sampling.

#### 4.2 Time-Domain Measurements on Evaluation Module

The next subsections present the dynamic properties of the transmitter and receiver circuits. The measurements were carried out separately for the transmitter and the receiver, although they are manufactured on the same monolithic structure. The realization of the monolithic structure allows us to attach the transmitter and the receiver to separate power supplies. That is inevitable because the circuits are designed to be operated with different supply voltages. For optimal functionality, -3.3 V supply was chosen for the transmitter and -5 V for the receiver. The module with two integrated radars packaged in QFN32 package (see Fig. 13) was designed and assembled for testing purposes. Thanks to the external pins of transmitter, receiver and control circuits, it is possible to understand the behavior of internal signals and therefore determine the dynamic performance of the system components.

#### 4.3 Dynamic Properties of Transmitter Circuits

In addition to the implementation of both UWB radar transmitter and receiver circuits into the single monolithic structure, the proposed topology includes several innovative elements. For example, the support for UWB multi-radar sensor network or the realization of the multichannel UWB sensor system with simultaneous generation of stimulation signals by multiple transmitters (so called pseudo-MIMO system) can be mentioned.

For the correct functionality of the multichannel systems, strict synchronization is crucial. In general, the synchronous operation can be achieved by accurate control. However, the control signals may be influenced by hardware. To mitigate the influence of the hardware, the input differential circuits were designed which operate with low voltage differential signals.

This approach results in the suppression of overshoots caused by logic circuits switching. In Fig. 9, the clock signal waveform is captured at the input as well as at the output of the control circuits. The clock signal is transferred to the output if the LVDS control signal is active. In detailed view in Fig. 9, the instant of output turn-on is shown, where the



switching transients are almost totally suppressed. This fact remarkably improves the measurement consistency because the stimulation signal generation of multiple radars can be turned on exactly at the same time, e.g. in a sensor network or a multichannel system.

#### 4.4 Dynamic Properties of the Receiver Circuits

In the receiver case, the measurements were concentrated mostly on the functionality of the sampling circuits. The time instants when transients between the sampling circuit (track and hold, T&H) states occur are important.

In general, there are two types of sampling circuits: T&H and S&H (sample and hold). The difference between them is in the manner how the samples are acquired, particularly in the signal shape at the output of the sampling circuit (see Fig. 10).

The sampling circuits perform the equivalent-time sampling of the input analogue signal x(t). In the sample acquisition instant, the instantaneous value is stored into the memory module (so called hold capacitor C<sub>H</sub> in Fig. 7), which becomes the information source for a short time. In the UWB radars, this information is available for the analogdigital conversion. In the next sampling phase, the capacitor is again charged and then again becomes the source of the value of the input signal. In the sampling phase, using the T&H circuits, the output is connected directly to the input between the HOLD periods. The sampling circuits copy the input signal x(t) to the output z(t). Therefore, this method is more convenient because the capacitor has to source the signal for a shorter time than in the case of S&H circuits where the output signal y(t) during the whole of the sampling periods has the signal value at instant of sampling as shown in Fig. 10 (left).



Fig. 10. Comparison of S&H (left) and T&H (right) sampling methods.

In the realized integrated UWB radar receiver, the equivalent time sampling with T&H method is exploited. The resulting output signal is shown in Fig. 11. The sampling process is strictly synchronous with the basic clock control pulses. In Fig. 11, the sampling process with clock synchronization signal frequency of 1.953 MHz is presented. The frequency is the result of the main clock signal frequency  $F_{\rm t} = 1 \, {\rm GHz}$  divided by the binary divider in the synchronization block (Fig. 2) with the ratio of 512. The sampling circuits react to the clock control pulse by changing from TRACK to HOLD mode or vice versa. During this process, the transients occur, defining one of the basic T&H circuit parameter, so called switching time delay. The detail of such a transient is shown in Fig. 11. The aim of the proposed concept of the UWB radar monolithic structure is to reduce those transients as much as possible. In the realized radar, the transients are much less apparent. Therefore, the sampling circuits require shorter timespan for their regeneration if compared to the previous versions, thus reducing the error rate of the A/D conversion.

Another parameter of the T&H circuits is the decrease or the fluctuation of signal voltage in the HOLD state. This feature is known as the pedestal error. The pedestal error can be partially compensated for by the increased offset of the clock control signals. The impact of the clock DC offset is illustrated by Fig. 12. In this manner, it is also possible to suppress the crosstalk which appears during the sampling process as well as optimize the receiver properties.

In Fig. 12 it can be observed that the output voltage in the HOLD mode becomes stable if sufficient offset voltage is provided. The offset can be set precisely according to the requirements. The waveform shown in Fig. 12 for  $U_{\text{Track}} = 200 \text{ mV}$  represents the output signal pre-sampled for the A/D converter. The A/D converter is driven by the same clock signal as the sampling circuits. It acquires always only one sample within each HOLD period. At the A/D converter output, the raw radar data are present and handed over for further digital preprocessing. The example of the digital preprocessing and analysis of the raw radar data is described in [4] and [17].

The module was designed solely for testing of the proposed integrated UWB radar. In the design phase, attention was paid to the best possible impedance matching of the RF paths from the connectors to the QFN package of the integrated UWB radar. To minimize the losses, the ceramic QFN32 package was chosen for testing, assembled on the fiberglass substrate Rogers RO3210. The RF substrate's thickness is 1.27 mm with a dielectric constant of 10.2, enabling to realize narrow paths which can be directly attached to the QFN package. For various applications, the designed and realized integrated UWB radar can be used in a similar manner. Progressive ceramic materials, like LTCC structures, may be exploited as well, allowing for the implementation of further structures, like input and output filters, to conform with the ECC and FCC standards [18], [19].



Fig. 11. Signal waveforms of the M-sequence sampling process.



Fig. 12. Sampling quality dependence, on the voltage offset of the clock synchronization signal.



Fig. 13. Evaluation module with integrated UWB radar, transmitter (left) and receiver (right).

## 5. Conclusion

The concept of the realized monolithic structure presented in this article represents the first step in the integration process of the wideband circuits for the UWB technology. It was a long way from the idea to this functioning device realized in the  $0.35 \,\mu\text{m}$  SiGe BiCMOS technology process using the newest version of libraries from the AMS and Cadence Virtuoso software for ASIC design. The main idea of this work was to make a test structure to gather a lot of new information about this kind of integrated UWB radar. As mentioned earlier, this structure integrates one transmitter – the M-sequence generator – and one wideband receiver on a single chip. The topology of the subcircuits is a practically verified solution, however, it has never been implemented in a single silicon substrate until now. Moreover, the transmitter, as well as the receiver circuits, were enhanced by the realization of the 15-bit M-sequence generator and the sampling process was improved at the receiver. The presented technology operates for the negative supply voltage, therefore it was necessary to solve the signal integrity issues between the analog and control parts of the device. For that purpose, an interface with support for LVDS communication was added. Regarding the testing, all basic parameters (AC, DC, nonlinear and dynamic) have been measured. As the next task, the proposed structure will be tested as the whole 15-bit UWB radar unit and the tests will be concentrated on the long-term reliability.

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