System Level Design of RF Receivers Based on Non Linear Optimization and Power Consumption Models

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Abstract. *This work presents a method to optimally distribute the block specifications in an RF receiver in order to reduce power consumption. The parameters are Gain (G), Noise Figure (NF) and Input Third Order Intercept Point (IIP3). The method is based on setting the signal quality per block at the output; Signal to Noise Ratio (SNR) for noise and Signal to Noise plus Distortion ratio (SNDR) for linearity. Both are limited in order to fulfill the sensitivity and intermodulation tests of a given standard. Nonlinear power models can be used as the method is based on heuristics associated with non linear optimization. First, random valid sets are tested "A" times, while the best candidate is chosen as starting point for a nonlinear optimization with bounds based on interior point algorithm. The process is repeated "B" times, and the best candidate is chosen. To validate the method, a direct-conversion receiver was dimensioned for the Long Term Evolution (LTE) and Bluetooth Low Energy (B-LE) standards. Three power models were used, labeled PM1, PM2 and PM3. First the LTE is considered. When compared to predetermined signal quality distributions, the method reduced the power consumption by* 65% *and* 41%, *considering PM1 and PM2, respectively. Then the B-LE is chosen with power model* 2. *This model is linear and has an analytical minimum derived in the literature. The optimization achieved a precision of* 0.2% *to the analytical minimum using* $A = 1000$ *and* $B = 15$.

Keywords

System level design, power consumption model, RF receiver, LTE, nonlinear optimization.

1. Introduction

The wireless communication market grew up exponentially in the last decades. While many topologies were invented and new technologies appeared, the main concern on RF receivers was to find the best possible performance on the circuit level, where in the system level design, little evolved. In a digital wireless transmission, the project of an RF receiver starts by defining the minimum performance of a receiver in terms of sensitivity and intermodulation characteristics. The traditional system design methods are still based on the system designer's experience and on cascaded performance equations such the Friis formula [1] to calculate the Noise Figure (NF) and the cascaded Input Third Order Intercept Point (IIP3) for linearity. Circuit designers normally seek the best block performance. This article is about aiming the lowest power consumption while the blocks have the minimum acceptable performance. To achieve optimization, it is necessary to find an optimal distribution for the gain (G), NF and IIP3 of the building blocks over the receiver chain. This distribution depends on how the block performance is related to its power consumption, in other words, the block power model.

It is a concern in the literature to model the power or energy consumption of RF transceivers to optimize the communication as a whole [2–8]. In [2], The concept of Figure of Merit (FoM) is introduced, the power consumption being linearly dependent on the G over NF. No averaged value is provided for the FoM. In [3], the parameters of IIP3 and the operating frequency f are added and a list of FoMs are provided for different building blocks and technologies. The power models for the voltage Controlled Oscillator (VCO) and Analog to Digital Converter (ADC) are also provided. An in-depth power model is provided for ADC and Analog Filter in [4], considering design parameters such transistors transconductance and the ADC input capacitance, showing that the top-down and bottom-up parametric simulations can help global optimization. In [5] an optimization is proposed along with the power model, which does not depend on the circuit gain, but on its dynamic range (IIP3 over NF). The work in [6] presented the power consumption of the communication, considering transmitter and receiver and the communication states: active and idle. When the Channel State Information (CSI) is not possible, such in a decentralized sensors network, optimizing the receiver has sensible impact on the global power consumption. In [7] presents an optimization in which the NF does not vary or is considered in the power model, but the G and IIP3 are optimized.

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To foresee the power consumption in future communications, the work in [8] shows a broad survey on the receiver blocks. It considers that the receiver power consumption comes mainly from the LNA and the ADC, providing power models for them. The power consumption considers the following parameters: Gain, Bandwidth, Signal Carrier, IIP3 and NF.

It was observed in [9] that for the designed LNA, in order to greatly reduce power consumption, little is degraded in terms of performance. If a linear a model is considered, a different FoM is obtained for each operating mode. These results clearly show a nonlinear power model. Some topologies and blocks present high linearity without increasing too much power consumption. For others it may be the gain that can be increased or the noise figure that can be decreased with less impact on the power consumption. Power models may come from circuit theory, parametric circuit level simulations or measurement results from the state of the art. This work is motivated by optimizing the receiver power consumption regardless the power model applied.

In [10], it was presented a method to distribute these parameters introducing a performance parameter dependent on the block NF and IIP3. The goal was to achieve the system requirements while minimizing the overall performance parameter. The performance parameter is considered equal for every building block, leading to an uniformly distributed signal quality degradation. It was shown in [3] performance parameter differs greatly between blocks, making this approach non optimal.

Similarly, the work in [5] links the power of a building block and its performance through the Power Coefficient (P_C). This time G is not considered in this model. Being the P_C different for each building block, the optimal signal quality degradation is not uniform. The optimization became an extremal problem with constraints where an analytical solution is found through Lagrange multipliers. The optimized signal degradation distribution is no longer uniform. The solution is only optimal to the given linear power model. In addition, the model does not set upper and lower bounds for the individual blocks.

In [7], it is proposed a power model which does not depend on the NF, but on G and IIP3. The FoM depends on the technology and the limiting bandwidth. Since the power model remains linear, the Lagrange Multipliers are also used to solve the optimization problem.

The proposed optimization method is based on combining an heuristic approach with nonlinear optimization with bounds. In the method, instead of optimizing the blocks G, NF and IIP3 directly, the signal quality at the block output are used. The metrics are the Signal to Noise Ratio (SNR) and the Signal to Noise plus Distortion Ratio (SNDR). The signal degradations are limited and summed up until the minimum required SNR and SNDRis obtained at the chain output. These limits and the achievable block performances for each circuit are the optimization bounds.

The document is depicted as follows. The basics on the system level design are revisited in Sec. 2. The optimization for RF dimensioning is revisited in Sec. 3. Two power models from the literature are presented in Sec. 4. In Sec. 5 the method is compared with pre-determined signal degradation distributions and the analytical approaches of [5] and [7]. Conclusions and perspectives for future work are given in Sec. 6.

2. Theoretical Background on RF Receiver Design

Radio frequency receivers must comply with a minimum signal quality delivered to the demodulator. The sensitivity (P_s) is the minimum signal level in dBm that the receiver can demodulate respecting a given Bit-error-Rate (BER) defined by the standard. The noise figure of the receiver is how much the receiver degrades the SNR from the input (SNR_{in}) in decibels to the output (SNR_{out}) specified as [11]

$$NF_{rx} = P_s - SNR_{min} - 10\log_{10}(kT \cdot BW) - 30\,[\mathrm{dB}] \quad (1)$$

where SNR_{min} is the minimum SNR required for the standard, k is the Boltzmann constant, T is the temperature in Kelvin, and BW is the bandwidth occupied by the modulated signal. Since a receiver consists of multiple stages, the SNR is progressively degraded until it achieves SNR_{min}. In presence of interferers, the minimum desired signal level to be demodulated can be M dB above P_s. Usually $M = 3$ dB. The SNDR is then added to consider the distortions caused by interfering signals, such as aliasing, phase noise intermodulation, or nonlinear intermodulation. The latter is mostly from third order intermodulation (IMD3) in dBm, which is be related to the receiver linearity through the IIP3:

$$IIP3_{rx} = \frac{1}{2}\left(3P_I - IMD3\right)\ [\mathrm{dBm}] \quad (2)$$

where P_I is the power of an interferer in dBm at the input. The maximum allowed level for IMD3 is defined as

$$IMD3 = 10\log_{10}\left(10^{\frac{P_s+M}{10}} - 10^{\frac{P_s}{10}}\right) - SNR_{min}\,[\mathrm{dBm}]. \quad (3)$$

The receiver consists of a cascade of stages, each one with a specific function. The main building blocks are: the RF filter (RFF) which limits the out of band interferences; the low noise amplifier (LNA) which provides gain at the beginning of the receiver chain adding as less noise as possible, and masking the the noise of subsequent blocks; the mixer (MX) which downconverts in frequency the modulated signal; the base band filter (BBF) which provides in-band interference rejection and anti-aliasing filtering; the variable gain amplifier (VGA), to complete the Automatic Gain Control (AGC); and the Analog to Digital Converter (ADC).

The cascade of the noise figures is given by the Friis [1] formula

$$NF_{\mathrm{rx}} = 10\log_{10}\left(10^{\left(\frac{NF_1}{10}\right)} + \sum_{i=2}^{n}\frac{10^{\frac{NF_i}{10}}-1}{\prod_{k=1}^{i-1}10^{\frac{G_k}{10}}}\right)[\mathrm{dB}], \quad (4)$$

while the cascaded IIP3 is obtained through [11]

$$IIP3_{\mathrm{rx}} = -10\log_{10}\left(\frac{1}{10^{\frac{IIP3_1}{10}}} + \sum_{i=2}^{n}\frac{\prod_{k=1}^{i-1}10^{\frac{G_k}{10}}}{10^{\frac{IIP3_i}{10}}}\right)[\mathrm{dBm}]. \quad (5)$$

There are infinite combinations for G_k, NF_i and $IIP3_i$ which meet the system specifications. The system level designers rely on their experience to set typical values for the block parameters and then evaluate if the cascaded performance ((4) and (5)) is compliant with the standard. The parameters may come from fabricated circuits, with the idea of reusing blocks from other standards. The cascaded results often do not achieve specifications or have too much margin, which is considered over dimensioning. The process is iterative in the sense that if the performance is not compliant in a first attempt, the specifications are adjusted for redesigning individual blocks.

A method to avoid over dimensioning is proposed in [12]. It is based on setting distributions for G, SNR and SNDR per block, until it achieves SNR_{min} in the sensitivity and linearity tests. The individual block parameters are attached to the signal quality degradations. This way the system always falls to the specified NF_{rx} of (1) and $IIP3_{\mathrm{rx}}$ of (2). It can be interpreted as an inversed Friis formula. First, the total gain depends on the maximum input level in dB ($P_{\mathrm{in_{max}}}$) and the ADC full scale ($P_{\mathrm{in_{ADC}}}$), both in dBm:

$$G_{\mathrm{max}} = \sum_{i=1}^{n} G_i = P_{\mathrm{in_{ADC}}} - P_{\mathrm{in_{max}}}\,[\mathrm{dB}]. \quad (6)$$

The total SNR degradation in decibels equals the circuit noise figure and it is the sum of the individual block SNR degradations in dB:

$$SNR_{\mathrm{deg_{TOT}}} = NF_{\mathrm{rx}} = \sum_{i=1}^{n} SNR_{\mathrm{deg}_i}\,[\mathrm{dB}]. \quad (7)$$

Then, the SNR at the output i^{th} block becomes

$$SNR_i = P_{\mathrm{s}} - 10\log_{10}(\mathrm{k}T\cdot BW) - 30 + \sum_{k=1}^{i} SNR_{\mathrm{deg}_k}\,[\mathrm{dB}]. \quad (8)$$

The input referred noise generated by a block depends on the output SNR of the previous stage and the given stage:

$$P_{\mathrm{n}_i} = 10^{\frac{P_{\mathrm{s}}}{10}}\prod_{k=1}^{i-1}10^{\frac{G_k}{10}}\left(\frac{1}{10^{\frac{SNR_i}{10}}} - \frac{1}{10^{\frac{SNR_{i-1}}{10}}}\right)[\mathrm{mW}]. \quad (9)$$

The block noise figure is then derived from P_{n_i}:

$$NF_i = 10\log_{10}\left(\frac{P_{\mathrm{n}_i}}{\mathrm{k}T\cdot BW\times 10^3} + 1\right)[\mathrm{dB}]. \quad (10)$$

Then, the SNDR degradation per block is defined as

$$SNDR_{\mathrm{deg}_i} = SNR_{\mathrm{deg}_i} + \lambda_i[\mathrm{dB}], \quad (11)$$

where λ_i is the incremental degradation from SNR_{deg_i} to $SNDR_{\mathrm{deg}_i}$, and is limited by M:

$$\sum_{i=1}^{n}\lambda_i = M[\mathrm{dB}]. \quad (12)$$

The SNDR at the block output is

$$SNDR_i = P_{\mathrm{s}} - 10\log_{10}(\mathrm{k}T\cdot BW) - 30 + M + \sum_{k=1}^{i} SNDR_{\mathrm{deg_k}}. \quad (13)$$

The distortion power P_{d_i} generated by a block is added to the noise and depends on the output SNDR of the previous stage and the given stage:

$$P_{\mathrm{d}_i} = 10^{\frac{P_{\mathrm{s}}+M}{10}}\prod_{k=1}^{i-1}10^{\frac{G_k}{10}}\left(\frac{1}{10^{\frac{SNDR_i}{10}}} - \frac{1}{10^{\frac{SNDR_{i-1}}{10}}}\right) - P_{\mathrm{n}_i}\,[\mathrm{mW}]. \quad (14)$$

Considering that P_{d_i} comes uniquely from third order intermodulation distortion, the block IIP3 becomes

$$IIP3_i = 5\log_{10}\left(\frac{\left(10^{\frac{P_\mathrm{I}}{10}}\prod_{k=1}^{i-1}10^{\frac{G_\mathrm{k}}{10}}\right)^3}{P_{\mathrm{d_i}}}\right)[\mathrm{dBm}]. \quad (15)$$

3. The Proposed RF Dimensioning Method

First, the objective function to minimize is the receiver overall power consumption P_{rx}:

$$P_{\mathrm{rx}} = \sum_{i=1}^{n} P_i\,[\mathrm{W}]. \quad (16)$$

where P_i is the power consumtion of the i^{th} block. The block power consumption is a function of G, IIP3, and NF, and indirectly, a function of the signal quality degradations:

$$P_i = f_{i1}(NF_i, IIP3_i, G_i)\,[\mathrm{W}]. \quad (17)$$

Assuming that these functions (power models) are different for each building block, the overall power consumption is a sum of functions of different natures

The the optimization algorithm varies G_i, SNR_{deg_i} and λ_i since their bounds are easily set by sum functions (6), (7) and (12). This grantees that any set of G_i, NF_i and $IIP3_i$ fulfills the standard and there is no over-dimensioning.

Indeed, the optimization variables are G_i, NF_i and $IIP3_i$. To evaluate P_i, one has to calculate NF_i from SNR_{deg_i} through (7)–(10), $IIP3_i$ from λ_i through (11)–(15), and then proceed with (17). Due to technological and practical circuit limitations, a valid set of G_i, NF_i and $IIP3_i$ in terms of cascaded performance may fall into unfeasible parameters individually. The building block parameters have lower and upper bounds, which are introduced as constraint functions in the optimization problem.

$$NF_{i_{\min}} \le NF_i \le NF_{i_{\max}}, \tag{18}$$

$$IIP3_{i_{\min}} \le IIP3_i \le IIP3_{i_{\max}}, \tag{19}$$

$$G_{i_{\min}} \le G_i \le G_{i_{\max}}. \tag{20}$$

Different technologies, topologies and applications lead to a wide range of possible results when looking at the many existing circuits in the literature. In [11], an extensive survey is provided.

In resume, the optimization problem is to find the minimum of the constrained nonlinear multivariate function of (16), considering the power models of (17), and optimizing G_i, NF_i and $IIP3_i$ with bounds defined by (6), (7), (12) and (18)–(20).

To deal with the local minima problem, a heuristic approach is adopted based on a *Two-phase Method* for Global Optimization [13]. It is a *Multi-start Problem* with *Pure Random Search* in the global phase and a *Convex Optimization Problem* in the local phase. The *Pure Random Search* in the global phase considers a total of "*A*" random samples tested without optimization. The best candidate between the "*A*" samples is then the starting point for a convex optimization problem, which is done through the *Interior-Point Method* in MATLAB® optimization toolbox. The *Interior-Point Method* is based on encode the feasible convex set using barrier methods [14], but details on the algorithm are not explored in this work. This process is then repeated "*B*" times. The work is also related to the *Repeated Local Search* since a random sampling generate a new state to optimize. It is heuristic in the sense that, instead of optimizing at each iteration, a total of "*A*" random samples are tested and the best candidate is then optimized. The algorithm is also different from *Pure Random Search* since after "A" iterations, the *Pure Random Search* takes the candidate as is, and our proposition is to start, from this point, a nonlinear optimization.

The complete algorithm is presented in Fig. 1. In steps 1 and 2 of the algorithm, the overall performance is calculated from the specifications to set the bounds of (6), (7) and (12). Then, in step 3, G_i, $SNR_{\deg_i}$ and λ_i are randomly generated, and normalized to respect the sums of (6), (7) and (12). In step 4 the individual block parameters are calculated through (10) and (15) and compared in step 5 with the bounds of (18), (19) and (20). Only valid sets increment the iteration counter (step 6). Steps 1 to 10 are repeated as long as "*A*" valid sets are achieved (step 7). When there is a valid set, the power consumption is evaluated in step 8, while when it is found to be a minimum the set is kept (steps 9 and 10). After "*A*" random valid set iterations, the best candidate of distributions so far is optimized with nonlinear optimization with constraints through the interior point algorithm, which is done in MATLAB (steps 11 to 13). Again, the power consumption is evaluated in step 14, compared to a minimum candidate from the optimization sets in step 15 and saved if it is the minimum in step 16. The nonlinear optimization occurs "*B*" times (step 17). The algorithm outputs are $P_{\min-\text{opt}}$, $G_{i-\text{opt}}$, $SNR_{\deg_{i-\text{opt}}}$ and $\lambda_{i-\text{opt}}$.

4. Power Consumption Models

There are some power models proposed in the literature [2–8] dependent on the block system level parameters. In this article, three models are adopted to evaluate the method, labeled power model 1 (PM1) [3], power model 2 (PM2) [5] and power model 3 (PM3) [7]. PM1 defines the power consumption for any amplifier, but more specifically, the LNA. It also covers the ADC power consumption. For all blocks but the ADC the power consumption is modeled as [3]

$$P_i = \frac{10^{\frac{G_i}{10}}\, 10^{\frac{(IIP3_i-30)}{10}} f_{ci}}{\left(10^{\frac{NF_i}{10}} - 1\right) FoM_i}\ [\mathrm{W}] \tag{21}$$

where f_c is the operating frequency in Hz, and FoM is the figure of merit in Hz. The FoM is a performance parameter which depends on the circuit type, the technology, topology and operating frequency. To estimate the power consumption (21) in a linear model, the FoM is considered constant for a certain range of performance parameters. The ADC power consumption is defined as

$$P_{\mathrm{ADC}} = \frac{2^{\mathrm{ENOB}} f_s}{FoM_{\mathrm{ADC}}}\ [\mathrm{W}] \tag{22}$$

where f_s is the ADC sampling frequency in Hz, ENOB is the effective number of bits, dependent of the ADC dynamic range, and FoM_{ADC} is the ADC FoM given in 1/J, which is considered constant for a given range of performance parameters.

PM2 [5] is simpler than PM1 [3]. Nevertheless, it represents a good first approach to distribute block specifications. The power consumption of a block is

$$P_i = \frac{P_{\mathrm{C},i} V^2_{IIP3,i}}{V^2_{\mathrm{n}_i}}\ [\mathrm{W}] \tag{23}$$

where $P_{\mathrm{C},i}$ is the block power coefficient, $V^2_{IIP3,i}$ is the block third order intercept point in $\mathrm{V}^2_{\mathrm{RMS}}$ and $V^2_{\mathrm{n}_i}$ is the block generated noise in the band of interest, input referred in $\mathrm{V}^2_{\mathrm{RMS}}$/Hz. In a linear model, $P_{\mathrm{C},i}$ is considered constant for a range of values for the performance parameters. In [5], neither the operating frequency nor the gain are considered, but since in there is an optimization involved, this model is used for comparison purposes.

In [7], the power model is valid close to the circuit initial parameters. It does not depend directly on the NF, which is let fixed in the optimization. The power consumption is approximated by

$$P_i = \frac{f_i}{k_i} 10^{\frac{G_i}{10}}\, 10^{\frac{(IIP3_i-30)}{10}}\ [\mathrm{W}] \tag{24}$$

where k_i is the block FoM and f_i the power limiting bandwidth, both in Hertz.

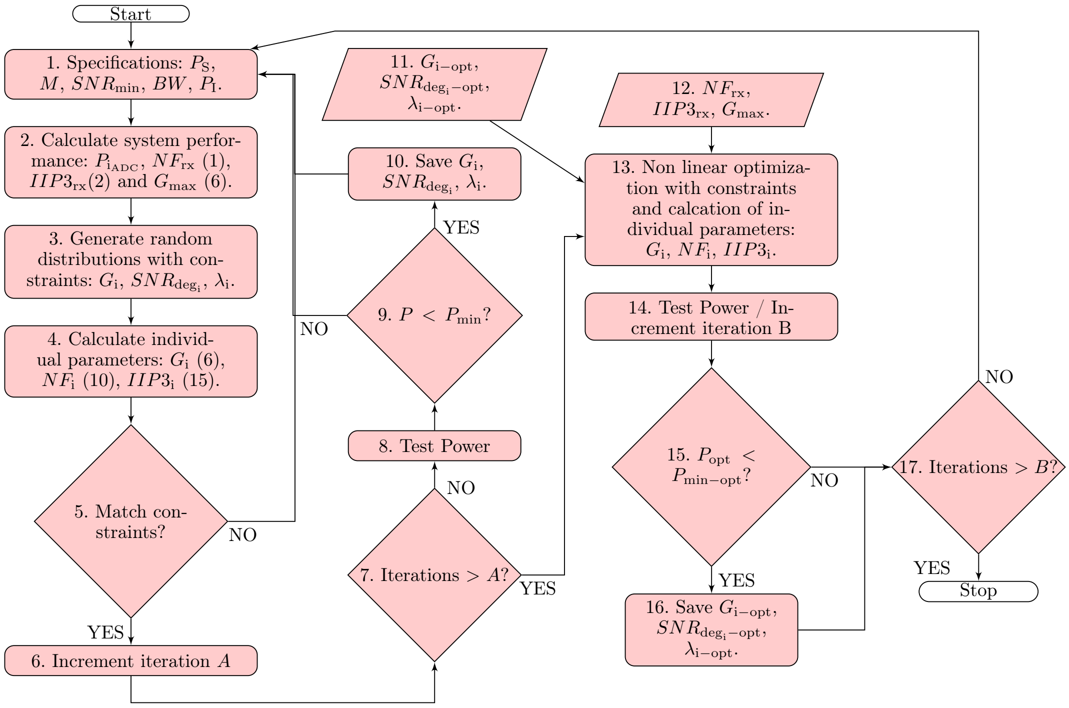

Fig. 1. Flowchart for the proposed system design method.

4.1 RF Circuits FoM, Power Coefficients and Parameters Bounds

The RF building blocks of interest in this study are the RFF, LNA, MX, BBF, VGA and ADC. The blocks FoMs for PM1 ((21) and (22)) are presented in [3]. Considering the 130nm CMOS as aimed technology, FoM_{LNA} = 10 GHz. The other blocks are not set in [3] and for simplicity the FoM will be considered the same as the LNA. The LNA and the mixer will operate at 2.5 GHz, while it is considered a bandwidth of 100 MHz (twenty times the signal band) for the BB filter and the VGA. The FoM for a 130nm CMOS ADC is $FoM_{ADC} = 0.4 \times 10^{12}$ 1/J. The aimed sampling frequency is f_s = 50 MHz.

For power PM2 (23), the power coefficients considered in [5] are: $P_{C,LNA} = 6.818 \times 10^{-20}$ and $P_{C,MX} = 5.476 \times 10^{-18}$. In [5], the BB filter has gain and is merged with the VGA. To test the same receiver in both models, the filter is considered with 0 dB gain followed by the VGA, deviding their power consumption. The power coefficients considered are $P_{C,BBF} = P_{VGA} = 9.595/2 \times 10^{-18}$. There is no power model for the ADC in [5], therefore PM1 is considered when applicable. The power coefficients in [5] were obtained from measurement results of a single receiver that aimed the B-LE standard.

For PM3 (24), three circuits for 65nm CMOS technology were considered. The NF does not change in the optimization, and the blocks FoMs, derived directly from the reference circuits, were: k_{LNA} = 25.87 GHz, k_{MX} = 3.31 GHz and k_{BBF} = 2.84 GHz. The circuits power limiting bandwidth were: f_{LNA} = 100 MHz, f_{MX} = 2.5 GHz and f_{BBF} = 30 MHz.

Lower and upper bounds for the circuit performance parameters are presented in [11] and summarized in Tab.1.

	RFF	**LNA**	**MX**	**BBF**	**VGA**	**ADC**
G_{min}	−2	0	−5	0	0	0
G_{max}	−2	25	20	0	40	0
NF_{min}	2	2	5	20	5	40
NF_{max}	2	3	20	40	60	70
$IIP3_{min}$	-	−20	−10	10	15	20
$IIP3_{max}$	-	0	11	35	40	45

Tab. 1. Block parameters constraints [11]. All units are in dB, except IIP3 in dBm.

5. Method Validation

5.1 Optimization Versus Pre-Determined Distributions, LTE Standard and Zero-IF Architecture

The specifications for the LTE standard [15] has many options in BW, modulation, sensitivity and bit rate. The performance analysis of the standard for a typical operating point for the LTE is presented in [16], leading to the system specifications and performance (steps 1 and 2 of Fig. 1), which are summarized in Tab. 2.

LTE Specifications		
$P_S = -98$ dBm	$SNR_{min} = 2$ dB	$P_I = -39$ dBm
$M = 3$ dB	$BW = 5$ MHz	$P_{in_{max}} = -68$ dBm
System Performance		
$P_{in_{ADC}} = -0.1$ dBm		$G_{max} = 67.9$ dB
$NF_{RX} = 7$ dB		$IIP3_{RX} = -19$ dBm

Tab. 2. LTE Specifications and System Performance.

For comparison purposes, three distributions for SNR_{deg_i} and λ_i are tested. Case 1 is an uniform distribution for SNR_{deg_i} and λ_i, case 2 is a linear decreasing distribution for SNR_{deg_i} and λ_i, and case 3 is a linear decreasing distribution for SNR_{deg_i} and linear increasing for λ_i. In all cases the gain is uniformly distributed amongst the LNA, MX and VGA. The block parameter bounds are neglected to fulfill the pre-determined distributions. Case 1 considers that if the blocks contributes equallyto the power consumption, the uniform distribution is the most fit for reducing power consumption, as presumed in [10]. Case 2 considers that once the first blocks mostly defines the system noise, they should degrade more the SNR at the beginning of the receiver. In addition to the noise hypothesis of case 2, case 3 considers that for the nonlinearity, the last blocks are the most constraining, so the nonlinear distortion should be higher at the end of the chain. Table 3 summarizes the pre-determined distributions along with the individual blocks parameters and the cascaded performance.

For all cases, one notice that some variables are quite stringent, such the NF_{LNA} for case 1 and the $IIP3_{\text{ADC}}$ in all cases, not matching the conditions of Tab. 1. Although applying such distributions always leads to the required cascaded performance, local parameters may fall in unrealistic values.

Table 4 summarizes the derived degradations and blocks parameters when applying the optimization and the conditions of Tab. 1. The loop parameter A and B where set empirically, considering a trade-off between precision and simulation time. The precision is measured by the relative normalized standard deviation δ_n of resulting power consumption:

$$\sigma_n = \frac{\sigma_p}{E[p]} \cdot 100[\%] \tag{25}$$

where δ_p and $E[p]$ are the the standard deviation and average of the resulting power consumptions, respectively. The whole optimization was repeated 100 times in order to evaluate δ_p in steps A and B. For $A = 1000$ the simulation time for the random sets was 0.4 s in a AMD A8 PRO-7600B R7 3.1 GHz clock processor and $\sigma_n = 23.3\%$. For $B = 15$, the overall simulation takes 29 s and $\sigma_n = 0.55\%$.

Figures 2, 3 and 4 highlight the Gain, SNR_{deg}, λ_i distributions, respectively.

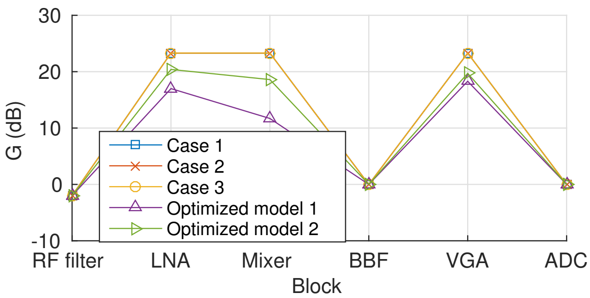

Fig. 2. The gain distributions.

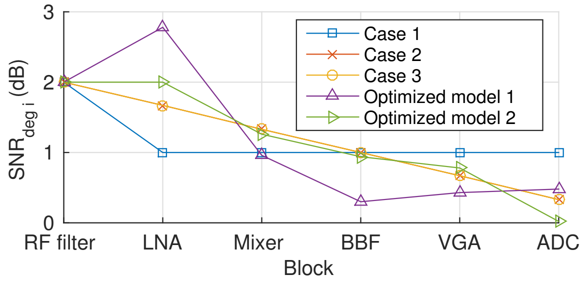

Fig. 3. SNR degradations.

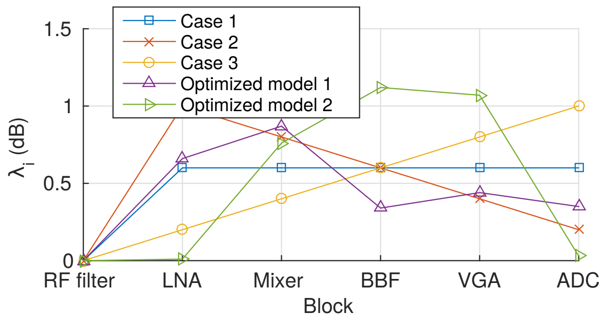

Fig. 4. λ_i distributions.

	RFF	LNA	MX	BBF	VGA	ADC	Tot.
	Gain for all cases						
G_i	–2	23.3	23.3	0	23.3	0	67.9
	Other parameters for case 1						
SNR_{deg_i}	2	1	1	1	1	1	7
λ_i	0	0.6	0.6	0.6	0.6	0.6	3
NF_i	2	1	18.5	42.7	43.7	68	7
$IIP3_i$	-	–14.8	10.3	33.3	32.7	41.7	–19
	Other parameters for case 2						
SNR_{deg_i}	2	1.67	1.33	1	0.7	0.33	7
λ_i	0 1	0.8	0.6	0.4	0.2	3	
NF_i	2	1.7	20.5	43.7	42.8	63.6	7
$IIP3_i$	-	–16.4	8.9	32.7	33.9	46.3	–19
	Other parameters for case 3						
SNR_{deg_i}	2	1.67	1.33	1	0.7	0.33	7
λ_i	0	0.2	0.4	0.6	0.8	1	3
NF_i	2	1.7	20.5	43.7	42.8	63.6	7
$IIP3_i$	-	–12.7	10.32	32.6	31.9	41.23	–19

Tab. 3. Distributions and block parameters for the test cases. All units are in decibels, except IIP3 in dBm.

	RFF	LNA	MX	BBF	VGA	ADC	Tot.
	PM1						
G_i	–2	17	11.7	0	18.3	0	45
SNR_{deg_i}	2	2.78	0.96	0.3	0.43	0.48	6.94
λ_i	0	0.66	0.87	0.34	0.44	0.35	3
NF_i	2	2.8	13.9	21	22.8	42.1	6.94
$IIP3_i$	-	–16	2	17.9	16.5	21.5	–19
	PM2						
G_i	–2	20.4	18.6	0	19.7	0	56.7
SNR_{deg_i}	2	2	1.26	0.94	0.78	0.02	7
λ_i	0	0.01	0.76	1.12	1.07	0.03	3
NF_i	2	2	17.7	36.1	36.1	40.1	7
$IIP3_i$	-	–6.5	4.2	23	23	44.9	–19

Tab. 4. Distributions and block parameters for the optimized receiver. All units are in decibels, except IIP3 in dBm.

At first, one observe that less gain was employed in both optimizations. The ADC plays a major role in relaxing the analog and RF blocks parameters by having a higher resolution. This is due to its better FoM compared to the remaining blocks. For PM1, the SNR degradation was optimized to relax the LNA in terms of noise and the Mixer in terms of linearity, since they presented the worst FoMs. For PM2, the mixer, the BBF and the VGA present the worst power coefficients, due to the application and topologies applied in [5]. While the mixer specification was relaxed in terms of noise, the linearity was the bottleneck for the BBF and VGA. The constraints are pushed to the other blocks, the LNA and the ADC, achieving the boundaries set for them, even if the LNA presented the highest SNR degradation. According to this power model, the gain does not affect the power consumption directly. In the system level, on the other hand, more gain would demand more linearity and less gain would require lower noise figure for the remaining blocks. The power consumptions for the different distributions are given in Tab. 5. Figures 5 and 6 show how the power consumption distributes over the blocks for PM1 and PM2, respectively.

In PM1 (Fig. 5), configurations of cases 1 and 3 pushed the constraints to the first blocks, which presented worse FoM. Letting more distortion in the front end in case 2, compensated that situation. In the optimization the ADC power consumption became the highest. Still, the overall power is reduced by 65% if compared to case 2. It is worth noticing that the BBF did not present significant levels of power consumption, A more accurate power model for this block in particular, could the filter order on the model or a worse FoM than the LNA.

For PM2 (Fig. 6), case 1 became the worst configuration since the presented quite different power coefficients, not fit for uniform distributions. Cases 2 and 3 relaxed the mixer constraints and reduced the overall power consumption. The LNA and the ADC presented by far the best power coefficients, achieving the performance bounds after optimization. In other words, they could not have any better specifications to relax the other blocks parameters. The mixer remained the most power hungry block, but its consumption was divided by 4 when compared to the uniform distribution. The overall power was reduced by 41.6% if compared with the case 3 distribution.

	RFF	LNA	MX	BBF	VGA	ADC	Tot.
	PM1						
Case 1	0	6.77	8.33	0	0.17	0.1	15.37
Case 2	0	2.62	3.62	0	0.27	0.2	6.72
Case 3	0	6.15	5.11	0	0.17	0.2	11.64
Optim.	0	0.35	0.25	0	0.16	1.6	2.37
	PM2						
Case 1	0	2.16	213.18	136.71	93.96	1.6	447.6
Case 2	0	0.84	92.65	93.96	152.24	1.6	341.29
Case 3	0	1.96	130.64	93.6	98.05	1.6	325.86
Optim.	0	6.58	62.35	59.18	59.04	3.2	190.35

Tab. 5. Evaluation in mW on the power consumption for the different distributions.

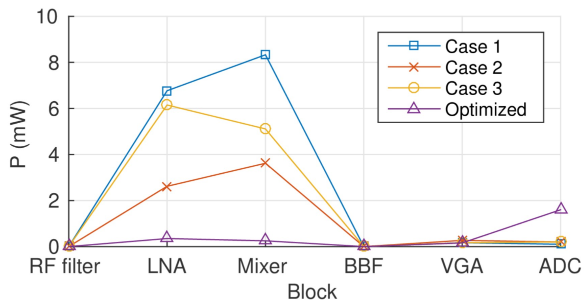

Fig. 5. Power consumption for PM1.

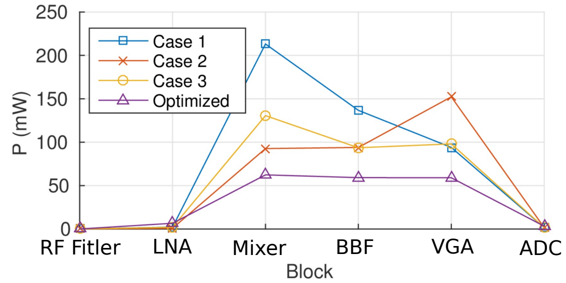

Fig. 6. Power consumption for PM2.

PM1 and PM2 differ greatly due to the fact that power PM1 is an averaged result from the literature and power PM2 comes from the measurements of a single circuit. The results shown in Tab. 5 demonstrates the capability of the method to find an optimized solution regardless the model. PM2 seems rather pessimistic, but the circuit in [5] was developed for the B-LE and the specifications fell far from the operating points on the measurement, giving such high power consumption.

5.2 Comparison with the Optimization Presented in [5]

In this subsection, the proposed method is applied in a system with the same conditions of the receiver optimized in [5]. The power coefficients of PM2 were obtained from measurements of a receiver dedicated to the B-LE standard [17]. The standard has very relaxed constraints in noise and linearity, aiming very low power consumption transceivers. Although the receiver in [5] has a much better system performance than the minimum required for the standard, the optimization will use it for a fair comparison. The optimization in [5] considered the following blocks: LNA, MX and BBF with gain, so it is called BBF amplifier (BBFA). Table 6 presents the measurement results for the receiver in [5]. It achieves an overall performance of NF_{rx} = 10.51 dB and $IIP3_{rx}$ = −18.24 dBm. The optimizations proposed in [5] and in this work are also presented in Tab. 6. Figures 7, 8 and 9 highlight the gain, SNR_{deg} and λ_i distributions, respectively.

	LNA	MX	BBFA	TOT
Measured receiver in [5].				
G_i (dB)	18	12	15	45
SNR_{deg_i} (dB)	3.53	4.75	2.23	10.51
λ_i (dB)	0.92	13.12	7.42	21.46
NF_i (dB)	3.5	24.5	36.5	10.51
$IIP3_i$ (dBm)	–0.14	5.7	14.2	–18.24
Optimization in [5].				
G_i (dB)	18	12	15	45
SNR_{deg_i} (dB)	2.95	4.98	2.59	10.53
λ_i (dB)	8.66	9.42	3.29	21.37
NF_i (dB)	2.9	24.3	37	10.53
$IIP3_i$ (dBm)	–7	4.3	15.6	–18.24
Optimization using the proposed algorithm in this work				
G_i (dB)	13.6	13.7	13.7	41
SNR_{deg_i} (dB)	2.97	4.96	2.6	10.53
λ_i (dB)	9.06	9.04	3.29	21.39
NF_i (dB)	2.9	19.9	34.3	10.53
$IIP3_i$ (dBm)	–7.2	0	12.9	–18.24

Tab. 6. Distributions and block parameters for the receiver in [5].

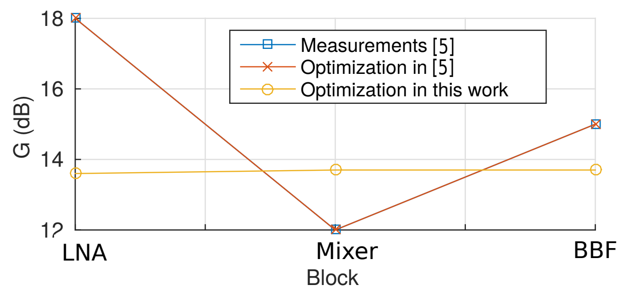

Fig. 7. The gain distributions for the B-LE test.

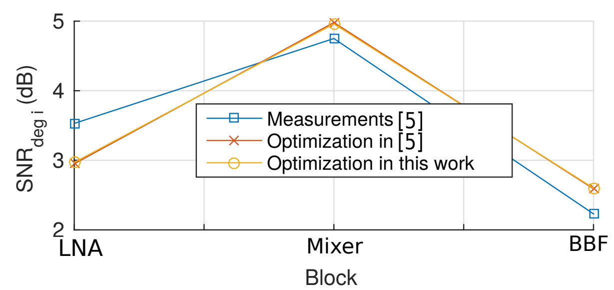

Fig. 8. SNR degradations for the B-LE test.

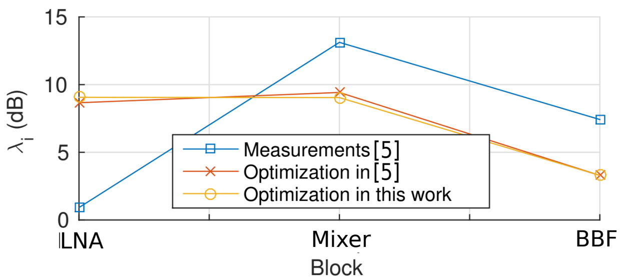

Fig. 9. λ_i distributions for the B-LE test.

	LNA	MX	BBFA	TOT
Measured [5]	13.12	17.9	14.02	45.04
Optimized [5]	3.5	13.99	17.19	34.68
Optimzed in this work	3.29	14.21	17.13	34.64

Tab. 7. Power consumption in mW for the for receiver in [5].

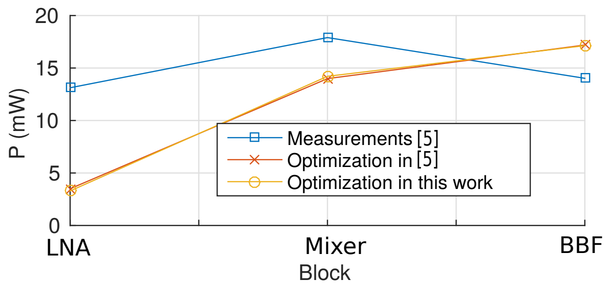

Fig. 10. Power consumption for the bluetooth test.

The optimization in [5] was based on finding an analytical minimum without changing the gain distribution (Fig. 7). The SNR_{deg} has not changed significantly (Fig. 8). It can be observed that, in order to reduce power consumption, the $IIP3_{\text{LNA}}$ was fairly decreased without changing the cascaded performance, where both optimizations relaxed the λ_i distributions for them (Fig. 9). The proposed optimization reduced the total gain, leading to more strict MX and the BBFA noise figures, but also relaxing the IIP3 constraints for these blocks. The estimated power consumption is shown in Tab. 7 and Fig. 10. While the analytical solution will certainly lead to the minimum possible, the proposed optimization resulted in a power consumption 40 µW (0.2%) lower, probably due to rounding in the presented numbers in [5]. The optimization was repeated 100 times, where all of the obtained optmizatoin fell inside this difference of 0.2%. Both optimizations reduced by 23% the power consumption in comparison with the measured circuit.

5.3 Comparison with the Optimization Presented in [7]

The blocks considered in the receiver for optimization in [7] where the LNA, MX and BBF. The blocks performance were retrieved from the literature and the cascaded performance calculated, regardless the aimed standard. The optimization varies the blocks G and IIP3. The NF remains fixed. As constraint, the cascaded performances G_{rx}, $IIP3_{\text{rx}}$ and NF_{rx} are also fixed. These conditions are added as constraints in the proposed optimization: $\sum G_i = 38.1$ dB, $\sum \lambda_i = 46.32$ dB, $NF_{\text{LNA}} = 3.5$ dB, $NF_{\text{MX}} = 6.5$ dB, $NF_{\text{BBFA}} = 21.8$ dB. With few optimization variables, the proposed optimization fell in the same configurations and power consumption, considering the precision of the numbers presented in [7]. Table 8 presents the receiver specifications in the measured and optimized cases.

The power consumption in the different cases are shown in Tab. 9. The power consumption and the cascaded performance were recalculated from the local parameters presented in [7], showing that most probably the block parameters were rounded for presentation.

	LNA	MX	BBFA	TOT
Measured receiver in [7]				
G_i (dB)	18.6	14.5	5	38.1
SNR_{deg_i} (dB)	3.50	0.09	0.14	3.73
λ_i (dB)	0.88	44.75	0.69	46.32
NF_i (dB)	3.5	6.5	21.8	3.73
$IIP3_i$ (dBm)	0.00	–7.50	17.00	–26.52
Optimization in [7]				
G_i (dB)	27.9	3.2	7.0	38.1
SNR_{deg_i} (dB)	3.50	0.01	0.22	3.73
λ_i (dB)	17.97	26.71	1.69	46.37
NF_i (dB)	3.5	6.5	21.8	3.73
$IIP3_i$ (dBm)	–12.20	2.51	11.60	–26.55
Optimization using the proposed algorithm in this work				
G_i (dB)	27.96	3.17	6.97	38.10
SNR_{deg_i} (dB)	3.50	0.01	0.22	3.73
λ_i (dB)	18.41	26.18	1.73	46.32
NF_i (dB)	3.50	6.50	21.80	3.73
$IIP3_i$ (dBm)	–12.42	2.62	11.58	–26.52

Tab. 8. Distributions and block parameters for the receiver in [7].

	LNA	MX	BBFA	TOT
Measured [7]	0.28	3.79	1.67	5.74
Optimized [7]	0.14	2.81	0.77	3.72
Optimzed in this work	0.14	2.87	0.76	3.76

Tab. 9. Power consumption in mW for the for receiver in [7].

6. Conclusions

With the goal of speeding up the RF systems design process, while bringing the best power consumption possible, this system level dimensioning method is based on individual power consumption models, on signal quality degradation distributions and on an optimization method respecting the minimum requirements of a given standard. The overall power consumption is evaluated for a set of individual block parameters with bounds.

The power models depend on many circuit topologies and technologies, and can present a nonlinear behavior, which can become an optimization problem in which the objective function presents many local minima. A combined heuristic nonlinear optimization is proposed in this context.

While considering two different power models in the literature, all simulations show the efficiency of the proposed method, when it reduces drastically the initial power consumption when a specific distribution is applied or when it achieves the same power consumption level of an analytical solution for a linear power model. It can be used if the designer wishes to reduce the RF receiver consumption to an specific application or to a receiver for multiple standard purposes. A future work will consider the local oscillator parameters and power consumption, to include the phase noise in the system level optimization.

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