

# Comparison of MOSFET Gate Waffle Patterns Based on Specific On-Resistance

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**Abstract.** This article describes waffle power MOSFET segmentation and defines its analytic models. Although waffle gate pattern is well-known architecture for effective channel scaling without requirements on process modification, until today no precise model considering segmentation of MOSFETs with waffle gate patterns, due to bulk connections, has been proposed. Two different MOSFET topologies with gate waffle patterns have been investigated and compared with the same on-resistance of a standard MOSFET with finger gate pattern. The first one with diagonal metal interconnections allows reaching more than 40% area reduction. The second MOSFET with the simpler orthogonal metal interconnections allows saving more than 20% area. Moreover, new models defining conditions where segmented power MOSFETs with waffle gate patterns occupy less area than the standard MOSFET with finger gate pattern, have been introduced.

## Keywords

Power MOSFET, waffle MOSFET, integrated circuits, specific on-resistance

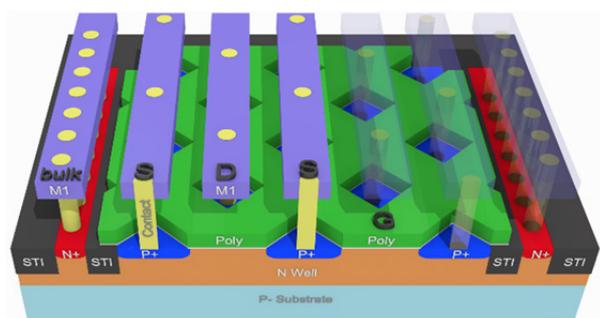
## 1. Introduction

Miniaturization in the semiconductor industry is a well-known practice. It is driven not only by price per area optimization, but it also allows realizing new types of applications, which are not easily reachable by previous generations of technologies. Actual trends and intensive developments are currently focused on mobile electronics, wearable electronics, and Internets of Things (IoT) applications that are limited by miniaturization possibilities. Applications such as smart watches, electronics pills, wireless head speakers, or Augmented Reality (AR) glasses represent a small part of new types of applications that come from progress in miniaturization. To solve high requirements on system dimensions, the highest process nodes are being used as well as whole system integration by using System in Package (SIP), System on Chip (SoC)

approach, Package on Package (PoP) or more advanced Through Silicon Via (TSV). The last TSV is used for 3D Integrated Circuits (IC) with more optimal interconnections and for more compact chips stacking. Additional advantage of smaller chip area is yield improvement [1].

In past and also nowadays, a big portion of IC chips are occupied by power management. In order to save area in SIP packages, we could use the more compact vertical power devices. Hence in more compact SoC, only lateral power devices can be used. For additional effective scaling of lateral low voltage power devices, the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) with waffle gate patterns can be used [2]. Another publication deals with RF measurement of the waffle MOSFET without defining analytic model of channel conductance [3]. Vemuru has described models for square shape waffle MOSFET in [4]. However, these models do not allow describing non-square shapes. Madhyastha [5] has described waffle MOSFET with orthogonal source and drain interconnection but its metallization is more complex and has a weak electro-migration limit. Moreover, the waffle structure robustness against threshold degradation due to ionizing dose radiation has been described in publication [6]. Shen-Li Chen [7] has described properties of lateral HV LDMOS waffle structures used for ESD of IC.

The advantage is that waffle gate topology patterns do not require any further adjustment of the process. This paper



**Fig. 1.** Waffle P-channel MOSFET with waffle gate (G) and orthogonal source (S) and drain (D) interconnections with bulk connection on each side.

Minimum Dimensions	Name	Size [-]
Poly Width	$d_1$	$\lambda$
Contact-Opening	$d_2$	$\lambda \times \lambda$
Contact-Poly Spacing	$d_3$	$\lambda$
Contact-Contact Spacing	$d_4$	$\lambda$
Poly -Poly Spacing with Contact	$d_5 = d_2 + 2d_3$	$3\lambda$
Poly-Poly Spacing with Diagonal Contact	$d_{d5} = \sqrt{2} d_2 + 2d_3$	$(\sqrt{2} + 2)\lambda$

**Tab. 1.** General designed rules for MOS layout [2].

introduces a new model allowing description and comparison of two waffle gate patterns. The first one is a MOSFET with waffle gate topology and with orthogonal source and drain interconnection (Fig. 1). This metal interconnection is more robust in term of serial resistance and electromigration than Madhyastha used [5]. The second one is a MOSFET with waffle gate topology and diagonal source and drain interconnections (Fig. 5). Both of them are compared with a standard MOSFET with finger gate topology (Fig. 3).

The IC fabrication process follows all process design rules that are collected in a design rule manual (DRM). Related to MOSFET geometry, the process design rule is often based on the scale process factor  $\lambda$  [2], [4]. Then the relationship between scale factor  $\lambda$  and the feature sizes is as shown in Tab. 1 [2]. Dimension  $d_5$  defines a minimum spacing between polysilicon gates with a contact to diffusion in between (Fig. 4). Dimension  $d_{d5}$  defines a spacing between gates with the contact to diffusion in between but contact is rotated about  $45^\circ$  (Fig. 7).

To support devices of higher voltage range from dual oxides processes, the gates length is also considered larger than minimum. In other words in this article, the gate length  $d_1$  can acquire a larger dimension than the minimum value defined in Tab. 1.

## 2. Comparison Method

For a quantitative comparison of different MOSFET structures, it is necessary to define a qualitative parameter for evaluation of benefits coming from more complex layout structures.

Drain current  $I_D$  in linear region of the MOSFET transistor with nonrectangular channel area is defined as

$$I_D = \left(\frac{W}{L}\right)_{EF} \mu C_{ox} (V_{GS} - \frac{V_{DS}}{2} - V_T) V_{DS} \quad (1)$$

where  $V_{GS}$  is gate to source voltage,  $V_T$  is threshold voltage and  $V_{DS}$  is voltage between drain terminal to source terminal of the MOSFET,  $\mu$  is charge-carrier effective mobility,  $C_{ox}$  is gate oxide capacitance per unit area and  $(W/L)_{EF}$  is an effective width to length ratio of the channel.

For small  $V_{DS}$  where  $V_{DS} \ll 2(V_{GS} - V_T)$ , the drain current is linear function of  $V_{DS}$  described by

$$I_D \cong \left(\frac{W}{L}\right)_{EF} \mu C_{ox} (V_{GS} - V_T) V_{DS}. \quad (2)$$

From known drain current  $I_D$ , it is possible to define the resistance of path from the drain to the source terminals marked as  $R_{DS-ON}$  with neglecting contacts and diffusion resistance [1] marked as

$$R_{DS-ON} = \frac{V_{DS}}{I_D} \cong \frac{1}{\left(\frac{W}{L}\right)_{EF} \mu C_{ox} (V_{GS} - V_T)}. \quad (3)$$

Equation (3) describes the main contributor to the total resistance. As can be seen, the other contributors such as package constraints, metal interconnection resistances, wire bonding or ball array that can play an important role in the total  $R_{DS-ON}$  resistance are not present in (3), because it is outside of the scope of this paper.

For regular finger shape of the MOSFET channel, the on-resistance is proportional to the channel length  $L$ , inversely proportional to the channel width  $W$ , and inversely proportional to the width to length ratio of the channel  $(W/L)_{fin}$

$$R_{fin} \cong \frac{1}{\left(\frac{W}{L}\right)_{fin} \mu C_{ox} (V_{GS} - V_T)}. \quad (4)$$

For MOSFETs with non-regular channel area such as waffle gate, the resistance  $R_{waf}$  is inversely proportional to the effective width to length ratio of the channel  $(W/L)_{waf}$

$$R_{waf} \cong \frac{1}{\left(\frac{W}{L}\right)_{waf} \mu C_{ox} (V_{GS} - V_T)}. \quad (5)$$

In practice, the power MOSFET devices are described by a figure of merit parameter known as specific on-resistance and defined as resistance on device area. In our case the specific on-resistance of MOSFET with waffle gate  $sR_{waf}$  is

$$sR_{waf} = R_{waf} A_{waf} \quad (6)$$

where  $R_{waf}$  and  $A_{waf}$  is resistance and area of the MOSFET with waffle gate topology, respectively. The specific on-resistance can be used not only to compare power MOSFETs devices but also to calculate the area for the required resistance. The area of MOSFET devices with the same resistance for waffle gate topology and finger MOSFET  $(A_{waf})_{R_{fin}}$  is described by the following expression

$$(A_{waf})_{R_{fin}} = \frac{sR_{waf}}{R_{fin}} = \frac{R_{waf} A_{waf}}{R_{fin}} = \frac{\left(\frac{W}{L}\right)_{fin} A_{waf}}{\left(\frac{W}{L}\right)_{waf}}. \quad (7)$$

The Area Increment  $AI$  of waffle MOSFET compared to finger MOSFET is

$$AI = \frac{(A_{\text{waf}})_{R_{\text{fin}}} - A_{\text{fin}}}{A_{\text{fin}}} = \frac{(A_{\text{waf}})_{R_{\text{fin}}}}{A_{\text{fin}}} - 1 \quad (8)$$

where after insertion of (7) into (8) the Area Increment  $AI$  is

$$AI = \frac{A_{\text{waf}} R_{\text{waf}}}{A_{\text{fin}} R_{\text{fin}}} - 1 = \frac{A_{\text{waf}} \left( \frac{W}{L} \right)_{\text{fin}}}{A_{\text{fin}} \left( \frac{W}{L} \right)_{\text{waf}}} - 1. \quad (9)$$

The figure of merit parameter  $AI$  quantitatively defines how much of the waffle structure area is required to achieve the same on-resistance as the standard MOSFET with finger gate topology has.

To achieve high reliability of power MOSFETs transistors, the bulk connections should be robustly connected. From a layout point of view, the bulk connection divides the whole power MOSFET into smaller segments. These segments are repeated over all structure (Fig. 2), and then the total area of the power MOSFET  $A_{\text{MOS}}$  is

$$A_{\text{MOS}} = (N_S (d_B + d_X) + d_B) d_Y \quad (10)$$

$$= N_S A_{\text{SEG}} + (N_S + 1) d_B d_Y$$

where  $N_S$  is a count of power MOSFET segments separated by bulk connection,  $d_B$  is a bulk dimension,  $d_X$ ,  $d_Y$  are X dimension and Y dimension of power MOSFET segment, and  $A_{\text{SEG}}$  is its area.

In this paper, a comparison between different power MOSFET structures has been realized at the same or very similar robustness of a bulk connection. Due to the same bulk connections and simplification of analytic models, the segment area or its subpart (core area) shown in Fig. 2 have been used for comparison of different power MOSFET structures described after.

## 2.1 Standard MOSFET Structure with Finger Gates

The basic MOSFET structures have finger gate topology where each finger has a rectangular shape of channel region as can be seen in Fig. 3. For correct and robust well polarization, the bulk connections are created on each side of the MOSFET.

An example of a segment of standard MOSFET topology with two finger gates without bulk connection is shown in Fig. 4. The Y dimension of this standard MOSFET and its width are in general defined as a real number. In this publication, it is considered as a discrete value due to alignment with waffle MOSFET dimensions and to simplify the analytic model. Due to this Y dimension of the standard MOSFET, it is possible to scale by an equivalent number of gate fingers  $N_{yF}$  in Y-axis.

For full analytical description, it is important to define not only dimensions of the whole structure but also its subparts called core area. The core area  $A_{\text{FC}}$  of the standard

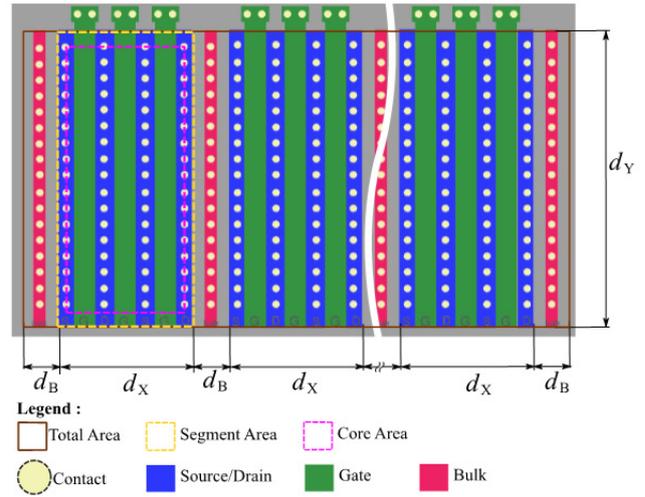


Fig. 2. MOSFET with finger gate (G) and orthogonal source (S) and drain (D) terminals segmented each  $d_X$  distance with bulk connection with dimension  $d_B$ .

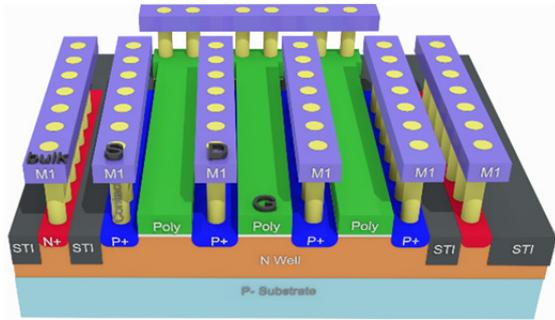


Fig. 3. Standard P-channel MOSFET with finger gate (G) and orthogonal source (S) and drain (D) terminals with bulk connection on both sides.

MOSFET segment with finger gate and without considering peripheral area outside the core area is

$$A_{\text{FC}} = (d_1 + d_5)^2 N_{xF} N_{yF} \quad (11)$$

where  $N_{xF}$  is a number of gate fingers in X-axis direction. Since the core area does not always contain whole contacts inside the boundary but also their fractions (Fig. 4). It is important to define area enlargement to allow fit of whole contacts into the boundary. In this publication, we consider enlargement of the core area about  $d_5/2$  on each side in X and Y-axis. After that, the segment area of the standard MOSFET with finger gates  $A_F$  is

$$A_F = (d_5 + (d_1 + d_5) N_{xF}) (d_5 + (d_1 + d_5) N_{yF}). \quad (12)$$

The width to length channel ratio in the core area for the standard MOSFET with finger gates  $WL_{\text{FC}}$  is

$$WL_{\text{FC}} = \frac{(d_1 + d_5) N_{xF} N_{yF}}{d_1} \quad (13)$$

and the width to length channel ratio for the standard MOSFET with finger gates on segment area  $WL_F$  is

$$WL_F = \frac{N_{xF} (d_5 + (d_1 + d_5) N_{yF})}{d_1}. \quad (14)$$

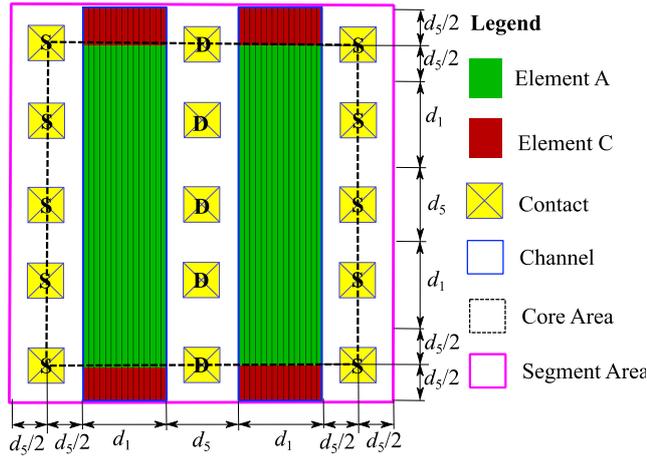


Fig. 4. Dimensions and partitioning of channel area in the segment of Standard MOSFET with finger gate and with orthogonal source (S) and drain (D) terminals to element A and peripheral element C, the whole and core structure dimension is  $N_{xF} = 2$ ,  $N_{yF} = 2$ .

## 2.2 Waffle MOSFET Structure with Diagonal Source and Drain

The MOSFETs with waffle gate topology have diagonal interconnections of source and drain terminals comparing to the standard MOSFET with finger gate topology (Fig. 5). The presented structure is compatible with all processes where diagonal interconnection is allowed and where the waffle shape polysilicon gates do not violate the process design rules. No additional process steps are required. The partitioning of the channel area of the waffle MOSFET segment is in Fig. 6.

Core area  $A_{WdC}$  of the MOSFET segment with waffle gates and diagonal source and drain interconnections without considering peripheral area outside the core area is

$$A_{WdC} = (d_1 + d_5)^2 N_{xWd} N_{yWd} \quad (15)$$

where  $N_{xWd}$  is a number of gate fingers in X-axis direction and  $N_{yWd}$  is a number of gate fingers in Y-axis direction. The segment area of the MOSFET with waffle gates and diagonal source and drain interconnections  $A_{Wd}$  is

$$A_{Wd} = (d_5 + (d_1 + d_5) N_{xWd}) (d_5 + (d_1 + d_5) N_{yWd}) \cdot (16)$$

The width to length channel ratio in core area  $WL_{WdC}$  for the MOSFET with waffle gates and diagonal source and drain interconnections is

$$WL_{WdC} = N_{xWd} N_{yWd} \left( \frac{2d_5}{d_1} + WL_B \right) \quad (17)$$

where  $WL_B$  is width to length channel ration in the region of element B (Fig. 6).

The width to length channel ratio  $WL_{Wd}$  of the MOSFET with waffle gates and diagonal source and drain interconnections on segment area is

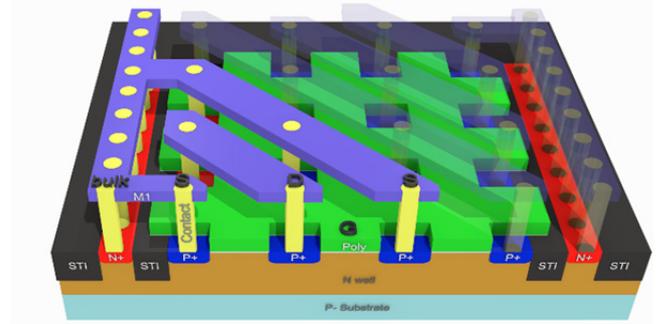


Fig. 5. P-channel MOSFET with waffle gate (G) and diagonal source (S) and drain (D) interconnections with bulk connection on both sides.

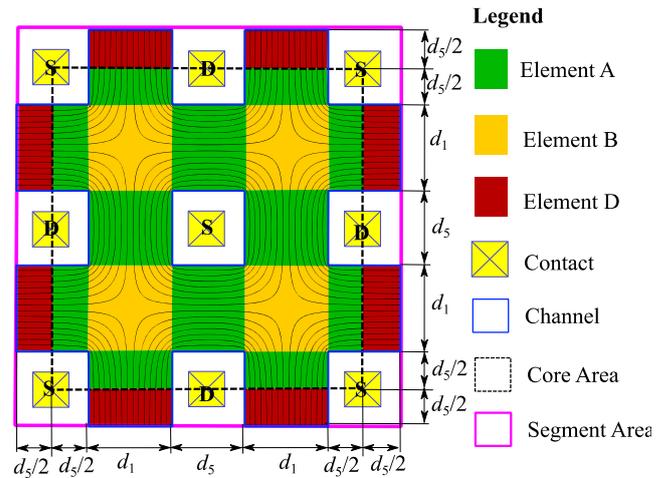


Fig. 6. Dimensions and partitioning of channel area in the segment of Waffle MOSFET with orthogonal source (S) and drain (D) terminals to element A and cross element B and peripheral elements D, the whole and core structure dimension is  $N_{xWd} = 2$ ,  $N_{yWd} = 2$ .

$$WL_{Wd} = \frac{d_5 (N_{xWd} + N_{yWd} + 2 N_{xWd} N_{yWd})}{d_1} + N_{xWd} N_{yWd} WL_B \quad (18)$$

As we can see, equation (18) describing the width to length channel ratio of the MOSFET with waffle gates and diagonal source and drain interconnections is a sum of width to length ratios of homogenous elements A, central elements B, and cross edge element E (Fig. 6).

## 2.3 Waffle MOSFET Structure with Orthogonal Source and Drain

Additional waffle structure is the MOSFET with waffle gates in orthogonal interconnections of the source and drain terminals (Fig. 1). Because source and drain contacts in the layout are not rotated, the layout of the structure (Fig. 7) is in general compatible with all processes where diagonal polysilicon gate does not violate the process design rules. No additional process steps are required. The bulk connection makes segmentation of the compact whole

power MOSFET into segments repeated over structure. To prevent process modification or design rule violations the contacts are not rotated about  $45^\circ$ . Due to this reason the spacing between two polysilicon gates  $d_{d5}$  is larger than  $d_5$  for waffle MOSFETs with diagonal source and drain interconnection as can be seen in Tab. 1. The core area of the MOSFET segment with waffle gates and orthogonal source and drain interconnections  $A_{W0C}$  without considering peripheral area outside the core area is

$$A_{W0C} = \frac{(d_1 + d_{d5})^2}{2} N_{xW0} N_{yW0} \quad (19)$$

where  $N_{xW0}$  is a number of gates in X-axis direction and  $N_{yW0}$  is a number of gates in Y-axis direction.

The segment area of the MOSFET with waffle gates and orthogonal source and drain interconnections  $A_{W0}$  is

$$A_{W0} = d_{d5}^2 + d_{d5}(d_1 + d_{d5}) \left( \frac{N_{xW0}}{\sqrt{2}} + \frac{N_{yW0}}{\sqrt{2}} \right) + \frac{(d_1 + d_{d5})^2}{2} N_{xW0} N_{yW0}. \quad (20)$$

The width to length channel ratio  $WL_{W0C}$  in core area for the MOSFET with waffle gates and orthogonal source and drain interconnections is

$$WL_{W0C} = N_{xW0} N_{yW0} \left( \frac{d_{d5}}{d_1} + \frac{WL_B}{2} \right). \quad (21)$$

The width to length channel ratio  $WL_{W0}$  for the MOSFET with waffle gates and diagonal source and drain interconnections on segment area is

$$WL_{W0} = N_{xW0} N_{yW0} \left( \frac{d_{d5}}{d_1} + \frac{WL_B}{2} \right) + (N_{xW0} + N_{yW0}) \left( WL_E - \frac{WL_B}{2} \right). \quad (22)$$

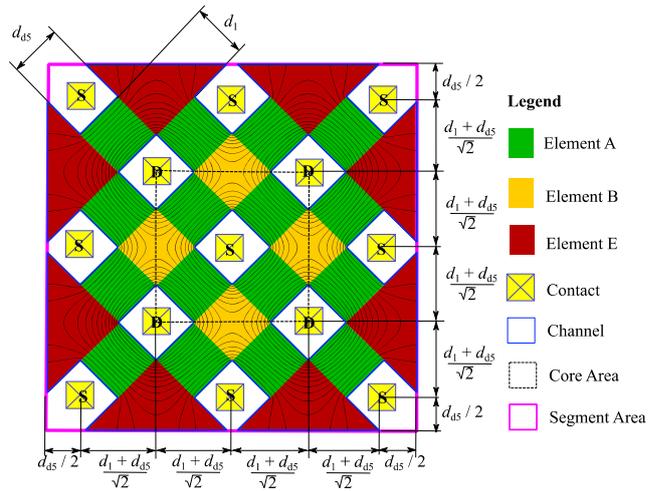
As can be seen in (22), the width to length channel ratio for MOSFET with waffle gate and diagonal source and drain interconnections is a sum of width to length ratios of homogenous elements A, central elements B and cross edge elements E.

## 2.4 Width to Length Ratio Calculation for Waffle MOSFET Elements

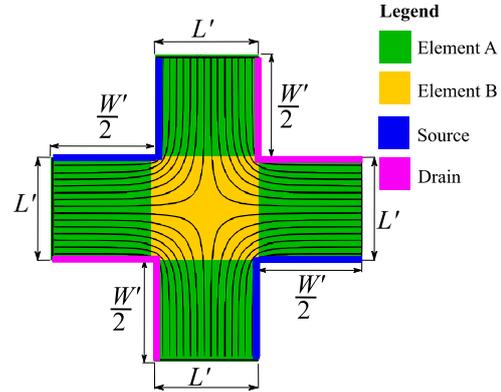
For calculation of width to length channel ratio of the element B and element E, 2D Finite Element Method (FEM) solver from TCAD SILVACO was used [8]. Test structure of element B is shown in Fig. 8.

The effective width to length channel ratio of the cross test structure  $(W/L)_{\text{cross}}$  is calculated based on the simulated 2D resistance  $R_{2D}$  and its resistivity  $\rho$  as follows

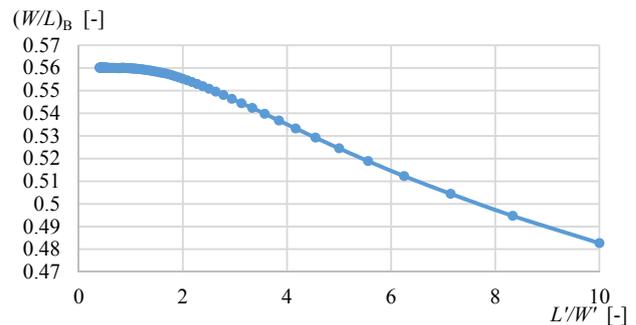
$$\left( \frac{W}{L} \right)_{\text{cross}} = \frac{\rho}{R_{2D}} = \rho \frac{I_D}{V_{DS}}. \quad (23)$$



**Fig. 7.** Dimensions and partitioning of channel area in the segment of Waffle MOSFET with orthogonal source (S) and drain (D) terminals to element A and cross element B and peripheral element E, core dimension is  $N_{xW0} = 2$ ,  $N_{yW0} = 2$  and the whole structure dimension is  $N_{xW0} = 4$ ,  $N_{yW0} = 4$ .



**Fig. 8.** The 2D cross structure used in TCAD simulation for determination of width to length channel ratio of cross element B for different dimensions  $W'$  and  $L'$ .



**Fig. 9.** The width to length channel ratio of cross element B  $(W/L)_B$  for different dimensions  $W'$  and  $L'$ .

To consider only the width to length channel ratio of element B, it is required to subtract the width to length channel ratio of four elements A. By considering homogenous current distribution in area of elements A and its subtraction from cross element, all nonhomogeneous current distributions will be pressed only into area of element B.

For homogenous current distribution in elements A, the effective width to length ratio is equal to its geometry aspect ratio

$$\left(\frac{W}{L}\right)_B = \left(\frac{W}{L}\right)_{\text{cross}} - 4\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_{\text{cross}} - 4\frac{W'}{2L'} \quad (24)$$

The result of the calculation as a function of its dimension is in Fig. 9.

For dimensions with ratio  $L'/W' < 10$ , we can approximate data from TCAD simulation by the following fitting function

$$WL_B\left(\frac{L'}{W'}\right) = \frac{5.44 - 1.146\frac{L'}{W'} + 0.56\left(\frac{L'}{W'}\right)^2 - 7 \cdot 10^{-4}\left(\frac{L'}{W'}\right)^3}{9.719 - 2.071\frac{L'}{W'} + \left(\frac{L'}{W'}\right)^2} \quad (25)$$

Another element E (Fig. 10) describing channel on the periphery can be calculated in a similar way. From known 2D resistance  $R_{2D}$  (TCAD simulation) and its resistivity  $\rho$  it is possible to calculate effective width to length channel ratio of cross test structure  $(W/L)_{\text{cross}2}$  as

$$\left(\frac{W}{L}\right)_{\text{cross}2} = \frac{\rho}{R_{2D}} = \rho \frac{I_D}{V_{DS}} \quad (26)$$

To consider only width to length channel ratio of element E, it is required to subtract the width to length channel ratio of two elements A. By considering homogenous current distribution in the area of elements A and its subtraction from edge cross element, all nonhomogeneous current distribution will be pressed into the area of element E only.

For homogenous current distribution in elements A the effective width to length ratio is equal to its geometry aspect ratio

$$\left(\frac{W}{L}\right)_E = \left(\frac{W}{L}\right)_{\text{cross}2} - 2\left(\frac{W}{L}\right)_A = \left(\frac{W}{L}\right)_{\text{cross}2} - 2\frac{W'}{2L'} \quad (27)$$

Calculated results of effective width to length channel ratio of element E are shown in Fig. 11.

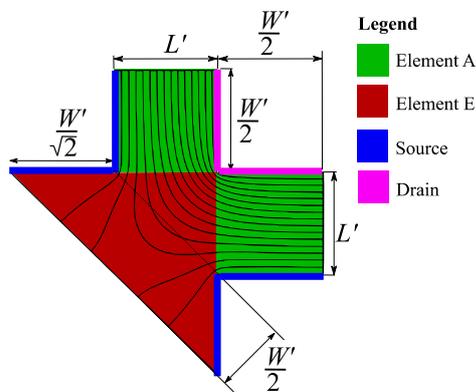


Fig. 10. The 2D structure used in TCAD simulation for determination of width to length channel ratio of peripheral element E for different dimensions  $W'$  and  $L'$ .

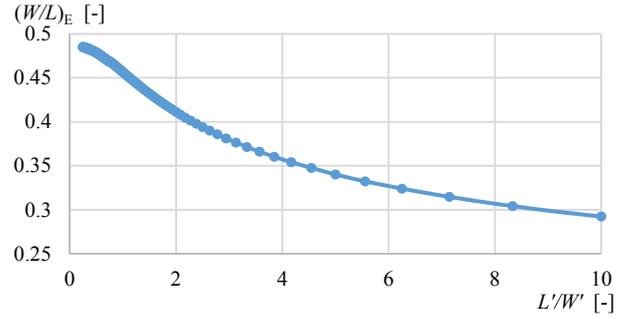


Fig. 11. The width to length channel ratio of cross element E  $(W/L)_E$  for different dimensions  $W'$  and  $L'$ .

For  $L'/W'$  value smaller than 10, we can approximate data from TCAD simulation by the following fitting function

$$WL_E\left(\frac{L'}{W'}\right) = \frac{0.72 + 1.44\frac{L'}{W'} + 0.23\left(\frac{L'}{W'}\right)^2 - 8.2 \cdot 10^{-4}\left(\frac{L'}{W'}\right)^3}{1.514 + 2.724\frac{L'}{W'} + \left(\frac{L'}{W'}\right)^2} \quad (28)$$

### 2.5 Core Structures Comparison

For core structures comparison, the figure of merit  $AI$  is used. In this section, no edge elements C, D and E will be taken into account.

In addition, the analytic model has been verified by 3D TCAD simulation from SILVACO [8] for different dimensions. The first simulated structure is the NMOSFET with finger gates (Fig. 12) and the second is the NMOSFET with waffle gates (Fig. 13). The simulated NMOSFET transistors have been in linear region where  $V_{GATE}$  is equal to 2.0 V,  $V_{DS}$  is equal to 0.2 V and gate threshold voltage  $V_{TH}$  is equal to 1.18 V.

The resistance  $R_{DS-ON}$  has been calculated from simulated drain current  $I_D$ . The Area Increment  $AI$  is calculated from  $R_{DS-ON}$  resistance of waffle and finger structures and from their areas by applying (9) (Fig. 14).

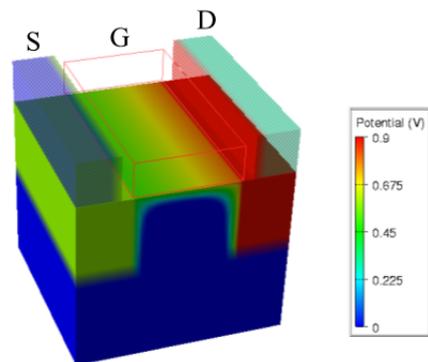
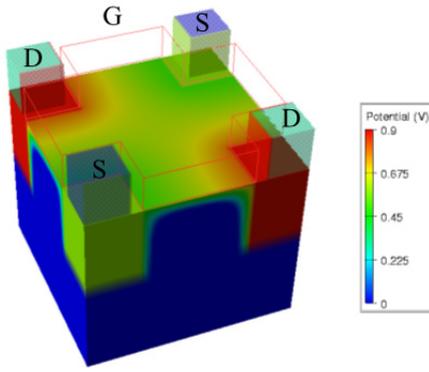


Fig. 12. Potential gradient from TCAD simulation in the standard NMOSFET with finger gate (G), source (S), drain (D) terminal and with dimensions  $N_x = 1$ ,  $N_y = 1$  without considering edge elements.



**Fig. 13.** Potential gradient from TCAD simulation in the waffle gate (G) NMOSFET with orthogonal and diagonal source (S) and drain (D) terminals with dimensions  $N_x = 1$ ,  $N_y = 1$  without considering edge elements.

To simplify the analytic model of Area Increment, we can define aspect ratio of gate dimension  $d_1$  and dimension of source or drain area  $d_5$  as follows

$$AR_{15} = \frac{d_1}{d_5}. \quad (29)$$

Putting expression (11), (13), (15), (17) and (25) into (9) and by applying (29), we have got core Area Increment  $AI_{WDC}$  of waffle MOSFETs with diagonal source and drain terminals on core area as

$$AI_{WDC} \Big|_{WL_B \rightarrow WL_B(AR_{15})} = \frac{1 + AR_{15}}{2 + AR_{15}WL_B} - 1. \quad (30)$$

It is apparent from (30) [9], the Area Increment  $AI_{WDC}$  is independent on the area dimensions of core elements  $N_{xF}$ ,  $N_{yF}$ ,  $N_{xWd}$ ,  $N_{yWd}$ .

To simplify analytic model of the waffle MOSFETs with orthogonal source and drain terminal, we can define aspect ratio of gate dimension  $d_1$  and dimension of source or drain area with diagonal contact  $d_{d5}$  as follows

$$AR_{1d5} = \frac{d_1}{d_{d5}}. \quad (31)$$

Putting expression (11), (13), (19), (21) and (25) into (9) and by applying (31), we have got core Area Increment  $AI_{WOC}$  of waffle MOSFET with orthogonal source and drain terminals on core area as

$$AI_{WOC} \Big|_{WL_B \rightarrow WL_B(AR_{1d5})} = \frac{AR_{15}(1 + AR_{1d5})^2}{(1 + AR_{15})AR_{1d5}(2 + AR_{1d5}WL_B)} - 1. \quad (32)$$

As can be seen from (32), the Area Increment  $AI_{WOC}$  is also independent on area dimensions of core elements  $N_{xF}$ ,  $N_{yF}$ ,  $N_{xW0}$ ,  $N_{yW0}$ .

Since equation (32) is a function of two aspect ratios  $AR_{15}$  and  $AR_{1d5}$ , it will be useful to simplify it. The first step is to define relation between  $d_5$  and  $d_{d5}$  by using scaling parameter  $\lambda$  from Tab. 1. Thus

$$d_{d5} \cong \frac{\sqrt{2} + 2}{3} d_5. \quad (33)$$

By inserting (33) into (31), we have got

$$AR_{1d5} = \frac{d_1}{d_{d5}} \cong \frac{3}{\sqrt{2} + 2} AR_{15}. \quad (34)$$

By inserting (34) into (32), we have got a simplified core Area Increment  $AI_{WOC}$  which depends only on one aspect ratio  $AR_{15}$

$$AI_{WOC} \Big|_{WL_B \rightarrow WL_B\left(\frac{3}{\sqrt{2}+2}AR_{15}\right)} \cong \frac{\left(\frac{\sqrt{2}+2}{3}\right)^2 + AR_{15} \left(2\frac{\sqrt{2}+2}{3} + AR_{15}\right)}{(1 + AR_{15}) \left(2\frac{\sqrt{2}+2}{3} + AR_{15}WL_B\right)} - 1. \quad (35)$$

As mentioned earlier, the figure of merit parameter Area Increment  $AI$  quantitatively defines the amount of needed areas to have the equal resistance of waffle structures and the standard MOSFETs with finger gates. When qualitative parameter Area Increment of waffle structure has negative value, it means that the waffle structure requires less area. Due to this, for real application it is very useful to know the dimensions of waffle structures where  $AI$  is negative.

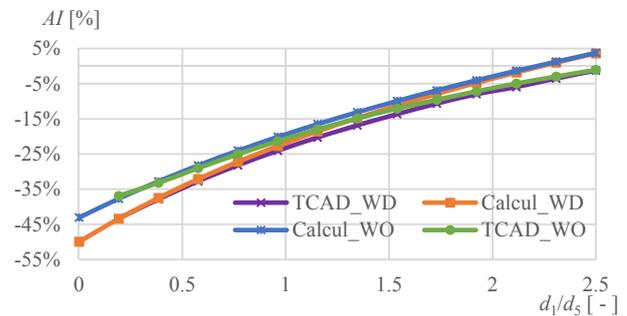
The Area Increment  $AI_{WDC}$  equation (30) is negative only if

$$0 < AR_{15} < 2.239. \quad (36)$$

The Area Increment from (35) is  $AI_{WOC} < 0$  only if

$$0 < AR_{15} < 2.237. \quad (37)$$

The equations (36) and (37) can be used for analytic definition of conditions when the area of core waffle structure occupies smaller area than the core finger structure with the same resistance.



**Fig. 14.** Dependence of Area Increment on core structures dimensions  $d_1/d_5$  for analytic model of waffle with diagonal source and drain Calcul\_WD and from 3D TCAD simulation TCAD\_WD, the analytic model of waffle with orthogonal source and drain Calcul\_WO and from 3D TCAD simulation TCAD\_WO.

### 2.6 Structures Comparison Considering Edge Elements

For more precise comparison of two topologies with considering edge elements, it is useful to have the same or similar area of each test structures. The same area of segments of the MOSFETs with finger or waffle gate topology and with diagonal source and drain terminals is guaranteed when  $N_x = N_{xF} = N_{xWd}$  and  $N_y = N_{yF} = N_{yWd}$ . After putting expressions (12), (14), (16), (18) and (25) into (9), we have got Area Increment  $AI_{WD}$  of the waffle MOSFET with diagonal source and drain terminals on segment area

$$AI_{WD} |_{WL_B \rightarrow WL_B(AR_{1d5})} = \frac{N_x(1+N_y+AR_{15}N_y)}{N_x+N_y+2N_xN_y+AR_{15}N_xN_yWL_B} - 1. \tag{38}$$

To have a similar area of the finger MOSFET as the waffle MOSFET with orthogonal source and drain terminals, it is required to set correctly the number of fingers  $N_{xF}$  and  $N_{yF}$  in the standard MOSFET. Number of gate fingers in X-axis is

$$N_{xF} = \frac{AR_{15} \left( 1 + \left( \frac{1}{\sqrt{2}} + \frac{AR_{1d5}}{\sqrt{2}} \right) N_{xwo} \right) - AR_{1d5}}{(1+AR_{15}) AR_{1d5}} \tag{39}$$

and in Y-axis it is

$$N_{yF} = \frac{AR_{15} \left( 1 + \left( \frac{1}{\sqrt{2}} + \frac{AR_{1d5}}{\sqrt{2}} \right) N_{ywo} \right) - AR_{1d5}}{(1+AR_{15}) AR_{1d5}}. \tag{40}$$

After putting (12), (14), (20), (22), (25), (28), (39) and (40) expressions into (9) and by applying (31) we have got Area Increment  $AI_{WO}$  of the waffle MOSFET with orthogonal source and drain terminals on segment area as given in (41) below.

By inserting (34) into (41), the simplified Area Increment  $AI_{WO}$  is a function of one aspect ratio  $AR_{15}$  only and thus it can be defined as given in (42) below.

$$AI_{WO} |_{WL_B \rightarrow WL_B(AR_{1d5}) \& WL_E \rightarrow WL_E(AR_{1d5})} = -1 + \frac{\left\{ \left[ -\sqrt{2} AR_{1d5} + AR_{15} \left( \sqrt{2} + (1+AR_{1d5}) N_{xwo} \right) \right] \left[ \sqrt{2} + (1+AR_{1d5}) N_{ywo} \right] \right\}}{\left\{ [1+AR_{15}] AR_{1d5} \left[ AR_{1d5} N_{ywo} (2WL_E - WL_B) + N_{xwo} \left( N_{ywo} (2+AR_{1d5}WL_B) + 2AR_{1d5}WL_E - AR_{1d5}WL_B \right) \right] \right\}}, \tag{41}$$

$$AI_{WO} |_{WL_B \rightarrow WL_B\left(\frac{3}{\sqrt{2}+2}AR_{15}\right) \& WL_E \rightarrow WL_E\left(\frac{3}{\sqrt{2}+2}AR_{15}\right)} \cong -1 + \frac{\left\{ \left[ 0.195 + \left( \frac{\sqrt{2}+2}{3} + AR_{15} \right) N_{xwo} \right] \left[ \frac{2\sqrt{2}+2}{3} + \left( \frac{\sqrt{2}+2}{3} + AR_{15} \right) N_{ywo} \right] \right\}}{\left\{ [1+AR_{15}] \left[ AR_{15} N_{ywo} (2WL_E - WL_B) + N_{xwo} \left( N_{ywo} \left( 2 \frac{\sqrt{2}+2}{3} + AR_{15}WL_B \right) + 2AR_{15}WL_E - AR_{15}WL_B \right) \right] \right\}}. \tag{42}$$

### 2.7 Definition of Waffle Use Cases Considering Edge Elements

In general, qualitative parameter Area Increment  $AI$  has negative value for all used cases, because only then the area of waffle structure occupies smaller area than finger structure with the same resistance. The Area Increment from (38)  $AI_{WD}$  is negative only if

$$0 < AR_{15} \leq 2.24 \& N_x \geq 1 \& N_y \geq 1 \tag{43}$$

and for the additional interval

$$2.24 < AR_{15} < 4.27 \& 1 \leq N_x < N_{x1} \& N_y \geq 1 \tag{44}$$

where  $N_{x1}$  can be approximated by the function

$$N_{x1} = (242975 - 51775 AR_{15} + 2.5 \cdot 10^4 AR_{15}^2) / (-242975 + 1.589 \cdot 10^5 AR_{15} - 48125 AR_{15}^2 + 11085 AR_{15}^3 + 169 AR_{15}^4). \tag{45}$$

$AR_{1d5}$  can be transformed into  $AR_{15}$  by using the following equation derived from (34)

$$AR_{15} = \frac{d_1}{d_5} \cong \frac{\sqrt{2}+2}{3} AR_{1d5}. \tag{46}$$

Then for negative Area Increment  $AI_{WO}$ , equation (42) can be calculated following conditions

$$0 < AR_{15} \leq 2.24 \& N_x \geq 1 \& N_y > N_{y2} \tag{47}$$

and for the additional interval

$$2.24 < AR_{15} < 3.35 \& 1 \leq N_x < N_{x2} \& N_y > N_{y2} \tag{48}$$

where  $N_{x2}$  can be approximated by the following function

$$N_{x2} = (-0.201 - 0.057 AR_{15} + 1.318 AR_{15}^2 + 0.044 AR_{15}^3) / (-3.637 + 0.595 AR_{15} - 1.776 AR_{15}^2 + AR_{15}^3). \tag{49}$$

Coefficient  $N_{y2}$  can be approximated by the function (50).

$$N_{y2} = 524.4 / (249.8 + 48.53 AR_{15} - 57.5 AR_{15}^2 + 1.949 AR_{15}^3 - 1.394 N_x - 6.168 AR_{15} N_x + 0.2578 AR_{15}^2 N_x + 0.4615 N_x^2 + 0.1638 AR_{15} N_x^2 - 0.017 N_x^3). \quad (50)$$

Equations (43), (44), (47) and (48) can be used for analytic definition of condition when the area of waffle structure occupies smaller area than the finger structure with the same resistance.

### 2.8 Comparison of Models with FEM Results

To analyze proposed models, more complex test structures in certain process have to be simulated in 2D FEM solver Agros2D [10] and the results are presented in Tab. 3. For test structures, the TSMC 0.35µm process design rules have been modified to be more robust (Tab. 2).

An example of potential gradient for three different gate patterns simulated in Agros2D can be seen in Fig. 15. Considering these three examples, it can be seen that they occupy similar areas (Tab. 3).

The standard MOSFET with finger gates length  $d_1 = 1.7 \mu\text{m}$ ,  $d_5 = 6.3 \mu\text{m}$  and dimension  $N_x = 5$ ,  $N_y = 5$  has

Name	TSMC 0.35µm	Modified
$d_1$ [µm]	1.7	1.7
$d_2$ [µm]	2.1	2.1
$d_3$ [µm]	1.7	2.1
$d_5$ [µm]	5.5	6.3
$d_{a5}$ [µm]	6.37	7.17

Tab. 2. General designed rules for MOS layout based on standard TSMC 0.35µm process and for modified process.

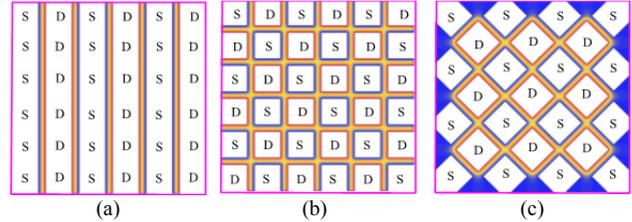


Fig. 15. The 2D simulation of channel area by Agros2D tool, illustrations of potential gradient for a) Standard MOSFET with finger gate dimension  $N_x = 5$ ,  $N_y = 5$ , b) Waffle MOSFET with diagonal source (S) and drain (D) terminals dimension  $N_x = 5$ ,  $N_y = 5$ , c) Waffle MOSFET with orthogonal source (S) and drain (D) terminals dimension  $N_x = 6$ ,  $N_y = 6$ .

area  $A_F = 2144 \mu\text{m}^2$  and width to length channel ratio calculated by analytic model is  $WL_F = 136.17$ .

MOS	$N_x$	$N_y$	$d_1$	$d_5$	$d_1/d_5$	$A_c$	$A$	$(W/L)_c$	$(W/L)$	$(W/L)_{FEM}$	$(W/L)_{ERR}$	$AI_c$	$AI$	Analytic Definition of Requirements for $AI < 0$
	[-]	[-]	[µm]	[µm]	[-]	[µm <sup>2</sup> ]	[µm <sup>2</sup> ]	[-]	[-]	[-]	[%]	[%]	[%]	
F	2	2	1.7	6.3	0.270	256	497	18.82	26.23					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y \geq 1$
Wd	2	2	1.7	6.3	0.270	256	497	31.88	46.71	46.45	0.56	-39.76	-42.99	
F	4	4	1.7	6.3	0.270	1024	1467	75.29	90.11					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y \geq 1$
Wd	4	4	1.7	6.3	0.270	1024	1467	127.54	157.19	156.1	0.70	-40.97	-42.67	
F	5	5	1.7	6.3	0.270	1600	2144	117.65	136.17					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y \geq 1$
Wd	5	5	1.7	6.3	0.270	1600	2144	199.29	236.35	234.8	0.66	-40.97	-42.38	
F	2	2	18	6.3	2.857	2362	3014	5.4	6.1					$2.24 < d_1/d_5 < 4.27$ & $1 \leq N_x < 3.41$ & $N_y \geq 1$
Wd	2	2	18	6.3	2.857	2362	3014	4.98	6.38	6.274	1.84	8.23	-4.53	
F	4	2	18	6.3	2.857	4724	5682	10.8	12.2					$2.24 < d_1/d_5 < 4.27$ & $1 \leq N_x < 3.41$ & $N_y \geq 1$
Wd	4	2	18	6.3	2.857	4724	5682	9.98	12.07	11.85	1.93	8.23	1.00	
F	2	3	1.7	6.3	0.270	384	676	28.24	35.65					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y > 2.06$
Wo	2	4	1.7	6.3 7.169*	0.270 0.237#	315	636	35.97	37.20	36.87	0.92	-35.69	-9.84	
F	3	3	1.7	6.3	0.270	576	918	42.35	53.47					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y > 2.06$
Wo	4	4	1.7	6.3 7.169*	0.270 0.237#	629	1040	71.95	73.59	72.98	0.85	-35.69	-17.66	
F	5	5	1.7	6.3	0.270	1600	2144	117.65	136.18					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y > 2.24$
Wo	6	6	1.7	6.3 7.169*	0.270 0.237#	1416	2007	161.90	164.36	163.00	0.84	-35.69	-22.43	
F	3	2	10	6.3	1.587	1594	2147	9.78	11.67					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y > 3.32$
Wo	4	2	10	6.3 7.169*	1.587 1.395#	1179	1753	7.97	8.91	8.787	1.50	-9.24	6.82	
F	2	5	10	6.3	1.587	2657	3415	16.3	17.56					$0 < d_1/d_5 \leq 2.24$ & $N_x \geq 1$ & $N_y > 3.06$
Wo	2	6	10	6.3 7.169*	1.587 1.395#	1769	2517	11.96	13.22	13.02	1.54	-9.24	-2.13	

Tab. 3. Comparison of Core Area Increment  $AI_c$  and Area Increment  $AI$  for different layout structures where  $N_x$  is the dimension in X-axis,  $N_y$  is the dimension in Y-axis,  $A_c$  is the area of the core structure,  $A$  is the area of the whole structure,  $(W/L)_c$  is the effective width to length channel ratio of the core element,  $(W/L)$  is the effective width to length channel ratio of the whole element,  $(W/L)_{FEM}$  is the effective width to length channel ratio of the whole element calculated with FEM by using Agros2D tool,  $(W/L)_{ERR}$  is the relative error between  $(W/L)$  and  $(W/L)_{FEM}$ , (\* value for dimension  $d_{a5}$ , # value for ratio  $d_1/d_{a5}$ ). F is Standard MOSFET with finger gate, Wd is MOSFET with waffle gate having diagonal interconnections of source and drain terminals and Wo is MOSFET with waffle gate having orthogonal interconnections of source and drain terminals.

The waffle MOSFETs with diagonal source and drain terminals and dimension  $N_x = 5$ ,  $N_y = 5$  has identical area  $A_{wd} = 2144 \mu\text{m}^2$  as standard MOSFET with finger gates and have width to length channel ratio calculated by analytic model  $WL_{wd} = 236.35$  which is about 0.66% higher value than calculated by FEM  $WL_{wd} = 234.8$ . From these analytic values by using (9), the Area Increment  $AI = -42.38\%$  can be calculated.

Based on this figure or merit parameter, it can be concluded that the waffle MOSFET with diagonal source and drain terminals with the same resistance as the standard MOSFET with finger gates occupies about 42.38% less area than finger structure, or equivalently for the same area, it has about 42.38% less resistance. On top of that, the analytic definition of requirements for  $AI_{wd} < 0$  based on (43), (44) ( $0 < d_1/d_5 \leq 2.24$  &  $N_x \geq 1$  &  $N_y \geq 1$ ) is consistent with observation where  $d_1/d_5 = 0.27$ . For additional structure with these parameters  $d_1 = 18 \mu\text{m}$ ,  $d_5 = 6.3 \mu\text{m}$ ,  $d_1/d_5 = 2.857$ ,  $N_x = 4$ ,  $N_y = 2$ , the Area Increment  $AI_{wd} = +1\%$ . Thus it has positive value because it exceeds predicted requirements ( $2.24 < d_1/d_5 < 4.27$  &  $1 \leq N_x < 3.41$  &  $N_y \geq 1$ ).

Similar comparison can be performed for the waffle MOSFET with orthogonal terminals. This test structure with gate  $d_1 = 1.7 \mu\text{m}$ ,  $d_5 = 6.3 \mu\text{m}$  and dimensions  $N_x = 6$ ,  $N_y = 6$  has area  $A_{wo} = 2007 \mu\text{m}^2$  which is about 6.3% smaller area than for the standard MOSFET with finger gates with calculated dimension  $N_x = 5$ ,  $N_y = 5$  from (39), (40). The width to length channel ratio calculated by analytic model  $WL_{wo} = 164.36$ , which is about 0.84% higher value than calculated by FEM  $WL_{wo} = 163.00$ .

The Area Increment for analytic values is  $AI = -22.43\%$ . In addition, the analytic definition of requirements for  $AI_{wo} < 0$  based on (47), (48) ( $0 < d_1/d_5 \leq 2.24$  &  $N_x \geq 1$  &  $N_y > 2.24$ ) is consistent with observation where  $d_1/d_5 = 0.27$  is recalculated based on (46) from  $d_1/d_5 = 0.237$ .

From the results, it is also apparent that the Area Increment calculated for core area  $AI_c$  presented by [2] is independent on segment dimensions and depends on aspect ratio of  $d_1/d_5$  or  $d_1/d_{d5}$  only. Because it does not consider peripheral elements, it cannot be used for precise description of power MOSFETs with segmentation.

### 3. Discussion

In this work, the gate length  $d_1$  is considered in wider range. Due to this, the aspect ratio  $AR_{15}$  defined by (29) can be larger than minimum ratio 1/3 used in [3] and [4] defined based on the  $\lambda$  scale process factor. The reason for larger gate length variability is to cover dimensions of low voltage MOSFETs with higher voltage range used by processes with dual oxide. In these processes, the gate with thicker oxide also has a larger length to sustain the higher voltage, but minimum contact to polysilicon spacing  $d_3$  is robust so that it can remain the same. Hence, also the di-

mension  $d_5$  can remain unchanged. Additional used cases for longer gate are in analog design where different  $W/L$  ratios are required.

In general, width to length channel ratios of non-homogenous elements B and E with non-homogenous current distribution are fixed values and do not have to vary with different element geometry. In opposite, width to length channel ratios of homogenous elements A, C and D with  $d_5 \gg d_1$  have mostly homogenous current distribution and have to vary with ratio of element geometry. For  $d_5 \leq d_1$ , the elements C and D mostly have non-homogenous current distribution. In publications [2], [3], [4], and [5], only homogenous currents are considered for these partially homogenous elements. In this work, all non-homogenous current distributions are considered to reach higher precision of width to length channel ratio calculation in range  $d_5 \leq d_1$ . This error correction is presented in the value of width to length channel ratio of non-homogenous elements B and E. This is the reason why width to length channel ratios of non-homogenous elements B and E are not fixed values and have to vary with different element geometry (25) and (27). Due to this reason, the precision less than 2% can be reached even for larger  $d_1$  (see Tab. 3 test structure:  $d_1 = 18 \mu\text{m}$ ,  $d_5 = 6.3 \mu\text{m}$ ,  $d_1/d_{d5} = 2.857$ ,  $N_x = 4$ ,  $N_y = 2$  then  $WL_{ERR} = 1.93\%$ ).

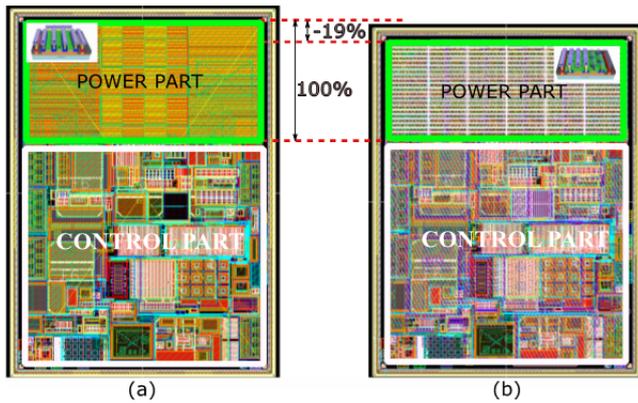
More precise  $AI$  equations (380 and (41) are function of multiple variables such as channel geometry  $AR_{15}$ ,  $AR_{1d5}$ ,  $WL_B$ ,  $WL_E$  and segment dimensions  $N_x$ ,  $N_y$ . Therefore, the conditions for negative  $AI$  are not simple to recognize. To overcome these drawbacks, conditions (43), (44), (47) and (48) have been calculated where the MOSFETs structures with waffle gates occupy less area than the standard MOSFETs with finger gates with the same channel resistance.

### 4. Waffle MOSFET Implementation in Power Integrated Circuits

Advantage of waffle MOS structures is that it allows improving of specific on-resistance of power MOSFET structures even without additional process steps or process modification of mature process. To reach the same  $R_{DS-ON}$  with using waffle MOS topology, the smaller power MOS area structure is required.

In order to use the waffle MOS concept in real application, the test chip has been designed and fabricated. In power management product from STMicroelectronics, made in 160nm BCD8sp process, the main low voltage (5V) power MOSFET Fig. 3 has been replaced with the equivalent waffle power 5V MOSFET with orthogonal source and drain interconnections Fig. 1. Because the waffle MOSFET has the same orthogonal source and drain interconnection as the original finger MOSFET, the replacement was faster and easier.

The proposed new IC with smaller power part passed all standard product validation tests [11]. Measured on-resistance of the original power MOSFET with finger gates



**Fig. 16.** Improvement of power management ICs in 160nm BCD8sP process: (a) Original IC with the standard finger power 5V MOSFET. (b) Reduced power MOSFET area about 19% by using the waffle power MOSFET with orthogonal source and drain interconnections.

was 397.53 m $\Omega$ , and measured resistance of the waffle MOSFET was 397.92 m $\Omega$ . Even we can consider the same on-resistance for both power MOSFET structures, the area of waffle MOSFET is about 19% smaller compared to the finger MOSFET structure Fig. 16. Due to the smaller power MOS area and the same control part area, the total chip area has been reduced about 6%.

## 5. Conclusion

To achieve high reliability of power MOSFET structures, the bulk connections have to be robustly connected [12]. This segmentation of power MOSFETs influences the specific on-resistance parameter. In this article, two MOSFET topologies with waffle gate with a diagonal and orthogonal source and drain interconnections have been compared and the new analytic models have been described for the first time. The proposed models in comparison to Vemuru [4] allow evaluating non-square shapes of power MOSFETs. Moreover, proposed orthogonal source and drain interconnections of waffle structure are much simpler in comparison to orthogonal topology proposed by Madhyastha [5] where an orthogonal source and drain interconnection has more complex metallization and has a weak electro-migration limit.

In addition, the analytic models of effective width to length channel ratio have been compared by numerical 2D FEM simulation. Here, the good match has been observed between analytical and numerical models with differences less than 2% for both waffle structures.

This paper confirms that models [2] considering only core area elements are not sufficiently precise for the accurate description of power MOSFETs with segmentation. Therefore, in this work, the new more precise models have been presented.

The examples of MOSFET topology with waffle gate pattern with diagonal source and drain interconnections and the standard MOSFET with finger gates have been com-

pared with the condition of the same on-resistance. As a result of this comparison, the waffle gate pattern with diagonal source and drain interconnections occupies 42.38% less area than the standard one.

Similarly, the second example of MOSFET topology with waffle gate with an orthogonal source and drain interconnections occupies 22.43% less area compared to the standard MOSFET with finger gates with the condition of the same on-resistance.

Moreover, in this paper, for the first time conditions have been defined where the segmented power MOSFETs structures with waffle gates occupy less area than the standard MOSFET structures with finger gates having the same channel on-resistance.

All analytical models of power structures have been realized based on FEM simulations. The silicon measurements of on-resistance for power MOSFET with finger and waffle gate have been proposed in the real application. In the power IC, it has been presented 19% area saving of power 5V MOSFET in 160nm BCD8sP process by using waffle power MOSFET with orthogonal source and drain interconnections.

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