# A Novel Design of Single Branch Wideband Rectifier for Low-Power Application

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**Abstract.** *This paper proposes a novel design of single branch wideband rectifier working at low input power level. Both the impedance tuning part and a dual-band matching network are adopted for wideband impedance matching. Theoretical analysis of the proposed wideband rectifier is presented and its closed-form design equations are derived. As an illustrated example, a wideband rectifier is designed and fabricated. Experimental results show that the fabricated rectifier features wide operated fractional bandwidth of more than 50%, low input power level from −5.0 dBm to 5 dBm, as well as a simple circuit structure and design procedure.*

## Keywords

Wideband, rectifier, wireless energy harvesting, impedance matching

## 1. Introduction

With the rapid increase of ambient wireless power density, wireless energy harvesting provides an attractive solution to supply low-power electronic devices for wireless sensor network, the internet of things, and low power consumer electronics applications [1]. High-efficiency rectifiers are crucial for realizing a large amount of dc output power in above devices [2], [3]. Since the environment contains substantial signal power spread over a wide frequency spectrum, the multiband or wideband rectifier, which can harvest the ambient RF power at multiple frequencies simultaneously, features higher RF-DC conversion compared with a single narrow band rectifier.

By connecting several rectifying branches in parallel, multiband rectifiers are implemented in [4], [5] while each operates in a narrow band. In order to simplify the circuit structure, each rectifying branch can realize impedance matching at more than one frequency band by using multi-band impedance matching network in [6], [7]. However, these designs all require multiple rectifying branches, leading to a relatively complex design process and high manufacturing cost.

Using voltage doubling circuit topology, a wideband rectifier with broad bandwidth from 4.0 to 6.3 GHz and wide input power range from 4 to 20 dBm is implemented in [8]. To extend the operation bandwidth, a novel matching network is presented in [9] through three-step impedance manipulating a fractional bandwidth of 44.9% is obtained with the minimum input level of 3 dBm. For low input power level application, an impedance matching network with operated band from 0.45 to 0.9 GHz is presented in [10] based on a shunt and series LC bandpass matching topology, and the efficiency increases linearly with the input power from −30 to 0 dBm.

Recent study rarely seeks balance between the input power density, the operated frequency bandwidth, and the design simplicity of the structure [8–14]. A more concrete design rule with closed-form equation needs to be further investigated for the efficient design of wideband rectifier. In this work, a single branch wideband rectifier is proposed by applying the presented wideband impedance matching network (WIMN). By controlling the input impedance and introducing a dual-band matching network, the input impedance of the rectifier can be optimized over a wide band to achieve wideband matching. Moreover, the closed-form design equations are derived for efficient design process. A wideband rectifier is then designed and fabricated to validate the proposed design method.

## 2. Wideband Rectifier Design

The proposed wideband rectifier as shown in Fig. 1 is composed of a full-wave voltage doubler rectifying circuit (C1, C2, D1 and D2), the presented WIMN (including Part I, Part II) and a resistive load $R_L$. It is worth pointing out that the WIMN is the key to realize a broadband rectifier and we will give its design process in detail.

### 2.1 Voltage Doubler Rectifying Circuit

The full-wave voltage doubler rectifying circuit converts RF power to DC power. The load $R_L$ is placed at the output port for collecting the DC power. The diodes D1 and D2 of the rectifying circuit are chosen as SMS7630 from
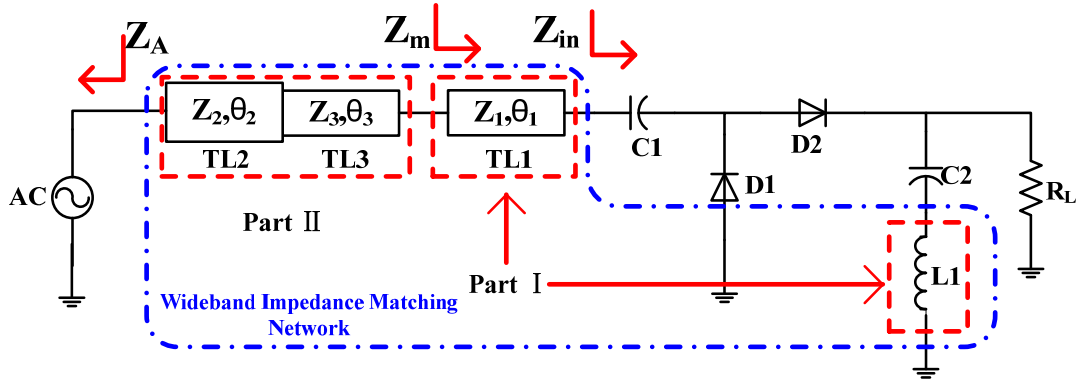
**Fig. 1.** The scheme of the proposed wideband rectifier.

Skyworks due to their low threshold voltage which makes them suitable for low power application. The two chip capacitors C1 and C2 are properly selected to ensure that the AC energy is fully stored during rectification.

## 2.2  Design of Part I in WIMN

The Part I composed of an inductor L1 and a transmission line TL1 is used to tune the input impedance $Z_m$. The introduction of L1 is to balance the input impedance $Z_{in}$ and make it maintain a constant slope over the whole operated frequency band. The design principle of L1 is to shift the natural resonant frequency of the original rectifying circuit to a lower frequency away from the operated frequency band. To meet the condition of impedance matching in the following Part II, we could make the real part of $Z_m$ remain stable while the imaginary part of $Z_m$ to be odd symmetry about the center frequency of the expected bandwidth. This means the impedance $Z_m$ at the starting frequency and ending frequency of the operation bandwidth is conjugated.

To solve the characteristic impedance $Z_1$ and electric length $\theta_1$ of TL1, we choose the starting frequency $f_1$ and ending frequency $f_2$ of the expected frequency band as the first pair of frequencies. The input impedances $Z_{in}$ are assumed as $Z_{in1} = R_{in1} + jX_{in1}$ at $f_1$ and $Z_{in2} = R_{in2} + jX_{in2}$ at $f_2$ respectively. According to the transmission line theory, the impedance $Z_m$ at $f_1$ and $f_2$ can be expressed as:

$$Z_m(f_1) = Z_1 \frac{(R_{in1} + jX_{in1}) + jZ_1 \tan\theta(f_1)}{Z_1 + j(R_{in1} + jX_{in1})\tan\theta(f_1)}, \quad (1)$$

$$Z_m(f_2) = Z_1 \frac{(R_{in2} + jX_{in2}) + jZ_1 \tan\theta(f_2)}{Z_1 + j(R_{in2} + jX_{in2})\tan\theta(f_2)}. \quad (2)$$

The relationship between $f_1$ and $f_2$ is defined as $p = f_2/f_1$ ($p \geq 1$). If we make the impedance $Z_m$ to be conjugated at $f_1$ and $f_2$:

$$\begin{cases} Z_m(f_1) = R_{m1} + jX_{m1}, \\ Z_m(f_2) = R_{m1} - jX_{m1}. \end{cases} \quad (3)$$

Then the characteristic impedance $Z_1$ and electric length $\theta_1$ can be calculated from (1) – (3) as:

$$Z_1 = \sqrt{R_{in1}R_{in2} + X_{in1}X_{in2} + \frac{X_{in1} + X_{in2}}{R_{in2} - R_{in1}}(R_{in1}X_{in2} - R_{in2}X_{in1})}, \quad (4)$$

$$\theta_1 = \frac{n\pi + \arctan\left[\dfrac{Z_1(R_{in1} - R_{in2})}{R_{in2}X_{in1} - R_{in1}X_{in2}}\right]}{1 + p}, \quad n = 1, 2, \ldots \quad (5)$$

## 2.3  Design of Part II in WIMN

The Part II consists of two transmission lines (TL2, TL3) with different parameters (($Z_2$, $\theta_2$), ($Z_3$, $\theta_3$)). The dual-band matching network is employed for the second pair of frequencies ($f_3$, $f_4$), which are also symmetrical to the center frequency $f_0 = f_1/2 + f_2/2$. The initial value of $f_3$ is typically set as ($f_1/2 + f_0/2$), while the initial value of $f_4$ is chosen as ($f_0/2 + f_2/2$). Considering the bandwidth of each passband and the coupling between them, the final value of $f_3, f_4$ can be further obtained by optimization with the aid of advanced design system (ADS) software.

Using the impedance tuning result in Part I, the input impedance $Z_m$ at $f_3$ and $f_4$ can be expressed as:

$$\begin{cases} Z_m(f_3) = R_{m2} + jX_{m2}, \\ Z_m(f_4) = R_{m2} - jX_{m2}. \end{cases} \quad (6)$$

Suppose that the source impedance $Z_A$ is a real impedance, the electrical length $\theta_2$ and $\theta_3$ can be obtained as [15]

$$\theta_2 = \theta_3 = \frac{\pi}{1 + k} \quad (7)$$

where $k = f_4/f_3$ ($k \geq 1$).

The value of $Z_2$ can then be solved by the following quartic equation:

$$C_1 Z_2^4 + C_2 Z_2^3 + C_3 Z_2^2 + C_4 Z_2 + C_5 = 0 \quad (8)$$

where                   $G = \tan(\pi/(1+k))$,

$$C_1 = -G^2 R_{m2} \left( R_{m2} - Z_A \right),$$

$$C_2 = 2G R_{m2} \left( G^2 Z_A X_{m2} \right),$$

$$C_3 = \left( R_{m2} - R_0 \right) \left[ Z_A \left( R_{m2}^2 + X_{m2}^2 \right) - R_{m2} Z_A^2 \right]$$
$$-2G^2 \left( Z_A X_{m2} \right)^2 - G^4 \left( Z_A X_{m2} \right)^2,$$

$$C_4 = -2G^3 R_{m2} Z_A^3 X_{m2},$$

$$C_5 = G^2 R_{m2} Z_A^3 \left[ \left( R_{m2}^2 + X_{m2}^2 \right) - R_{m2} Z_A \right].$$

Choosing a positive real value in the four solutions of $Z_2$, the value of $Z_3$ can be further obtained by one of the following two equations:

$$Z_3(1) = \frac{-b - \sqrt{b^2 - 4ac}}{2a}, \quad Z_3(2) = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \quad (9)$$

where $a = -G^2 R_0$, $b = (R_0 - R_{m2})Z_2 - GR_0 X_{m2}$, $c = G^2 R_{m2}(Z_2)^2 - GR_0 X_{m2} Z_2$, $R_0$ is the source impedance. Thus, we can obtain the parameters of the TL2 and TL3 from (7) – (9).

# 3. Experimental Results

A wideband rectifier is designed based on the above design rule with the operated frequency band from 1.7 GHz to 2.5 GHz. Firstly, the center frequency of the expected band is chosen as 2.1 GHz, and the first pair of frequencies $f_1$, $f_2$ are selected as 1.7 GHz and 2.5 GHz. The capacitor C1 and C2 are both selected as 100 nF, and the load $R_L$ is chosen as 1 kΩ for our application scenario. The simulated result of input impedance $Z_{in}$ with different inductor value L1 at the input power of −5.0 dBm is shown in Fig. 2. It can be observed that the real and imaginary part of $Z_{in}$ change greatly when L1 increases to 10 nH. However, when L1 is above 30 nH, the variation of real and imaginary part as L1 changes can be neglected.

As the value of L1 increases from 0 nH to 200 nH, for the operated frequency band from 1.7 GHz to 2.5 GHz, the real part fluctuation of the input impedance $Z_{in}$ decreases from 16.8 Ω to 10.4 Ω while the imaginary part fluctuation varies from −j·64.6 Ω to −j·50.8 Ω. Therefore, the variation of input impedance is greatly reduced and a smaller slope of the input impedance $Z_{in}$ with frequency is achieved, which is helpful for broadband impedance matching. It is worth noting that for the operated band of this designed rectifier, the load impedance of D2 may be dominated by $R_L$ due to the introduced L1, leading to an increased AC component which will be discussed in the following. The final value of L1 is chosen as 200 nH in this design.

We could further obtain the input impedance $Z_{in1} = (52.2 - j·102.6)$ Ω and $Z_{in2} = (41.8 - j·51.9)$ Ω respectively at an input power level of −5 dBm. According to (4), (5), the characteristic impedance $Z_1$ and electrical length $\theta_1$ are calculated to be 175.9 Ω and 52.9° correspondingly at $f_1$. Figure 3 depicts the curve of input impedance $Z_m$ over the

whole expected frequency band at different input power levels. It is demonstrated that through the use of Part1, the real part of $Z_m$ remains stable and the imaginary part is odd symmetrical to the center frequency $f_0 = 2.1$ GHz.

Secondly, the second pair of frequencies $f_3$, $f_4$ is selected as 1.8 GHz and 2.4 GHz respectively and the impedance $Z_A$ is selected as 50 Ω. Thus, we can obtain the $Z_m(f_3) = (40.8 - j·20.0)$ Ω, $Z_m(f_4) = (39.9 + j·32.7)$ Ω at the input power level of −5 dBm. $R_{m2}$, $X_{m2}$ are taken as the average value of real part and imaginary part of $Z_m(f_3)$ and $Z_m(f_4)$ respectively, which are 40.4 Ω and −j·26.4 Ω respectively. According to (7), (8), the characteristic impedance $Z_2$ and electric length $\theta_2 = \theta_3$ are calculated to be 25.3 Ω and 77.1° at 1.8 GHz respectively. The characteristic impedance $Z_3$ is calculated to be 29.2 Ω by using (9). Finally, the above initial parameters are optimized by ADS software and the layout of the proposed rectifier is shown in Fig. 4. The capacitance model from Murata [16] and the inductance model from Coilcraft [17] are employed during the optimization process.
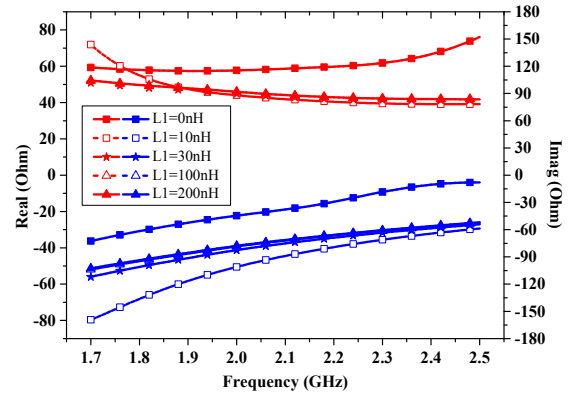


**Fig. 2.** The variation of input impedance $Z_{in}$ with different inductor value L1 at the input power of −5 dBm.
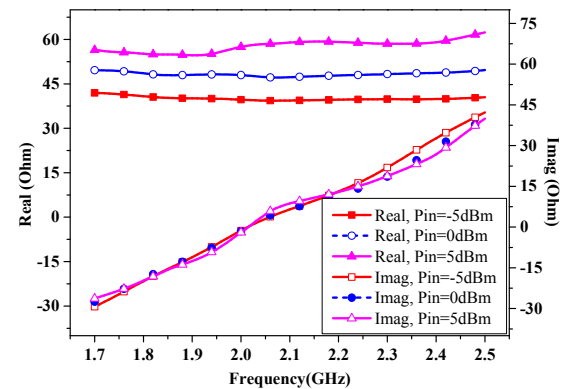


**Fig. 3.** The impedance $Z_m$ with different input power levels over 1.7–2.5 GHz.



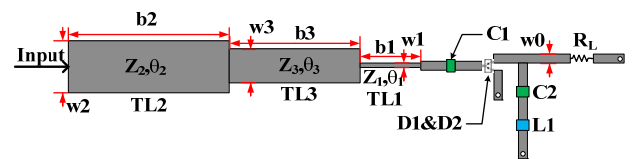**Fig. 4.** The layout of the proposed rectifier.

The final optimized values of the fabricated rectifier are the following: w0 = 1.0 mm, w1 = 0.5 mm, w2 = 8.6 mm, w3 = 7.7 mm, w4 = 0.5 mm, b1 = 9.8 mm, b2 = b3 = 26.0 mm, b4 = 8.6 mm, L1 = 200 nH. The simulated reflection coefficient of the rectifier is shown in Fig. 5, where the frequency band with $|S_{11}|$ below –10 dB is from 1.5 GHz to 2.5 GHz at the input power level from –5 dBm to 5 dBm. For comparison, the simulated reflection coefficient result in the case of the removed inductor L1 is also given in Fig. 5. It can be clearly found that the rectifier with L1 has better broadband impedance matching and wider operated bandwidth.

The above designed wideband rectifier is manufactured and Figure 6 shows the photograph of the final fabricated rectifier. The employed substrate is TANOIC TLY-5 with the thickness of 1.575 mm, relative dielectric constant of 2.2, and loss tangent of 0.0009. The package size of the employed load $R_L$ is 1206 (3.2 mm × 1.6 mm) and the pack-

age sizes of the employed capacitance (C1 and C2) and inductance (L1) are all chosen as 0805 (2.0 mm × 1.2 mm). Figure 7 shows the measured and simulated reflection coefficient $|S_{11}|$ and efficiency versus frequency at the input power of –5 dBm. It is seen that the measured $|S_{11}|$ is better than –10 dB from 1.3 GHz to 2.3 GHz, featuring a fractional frequency bandwidth of 55.6%. We could find that a small frequency shift exists between the measured and the simulated reflection coefficient results, which may result from the model discrepancy between simulation and actual circuit.

The parasitic effect and fabrication error will cause an inconsistency between the actual $Z_{in}$ and the designed value ($Z_{in1}$ and $Z_{in2}$). Thus, the actual frequency pair which meets the conjugated impedance $Z_m$ condition in Part I deviates from the originally designed frequency pair $f_1$ and $f_2$. When applying the dual-band matching network in Part II, the optimum impedance matching frequency is shifted from the original designed frequency. Moreover, the wideband impedance matching performance is slightly deteriorated due to the frequency shift.

By slighty tuning the parameters of three transmission lines (TL1, TL2, TL3), the above frequency shift can be corrected with the modified simulation result added in Fig. 7. In this case, the length b1 changes from 9.8 mm to 12.1 mm, the width w2 changes from 8.6 mm to 8.9 mm and the width w3 changes from 7.7 mm to 7.2 mm. We could find that a better agreement between simulation and measurement results is obtained and the frequency shift is corrected.

The RF-DC conversion efficiency of the rectifier can be expressed as [6]

$$\eta_{RF\text{-}DC} = \frac{P_{DC}}{P_{RF}} = \frac{V_{DC}^2}{P_{RF}R_L} \tag{10}$$

where $P_{DC}$ is the output power in dc, $P_{RF}$ is the input RF power to the rectifier, $V_{DC}$ is the output voltage. The RF signal generator (Agilent E8257D) is used to feed the proposed rectifier and the measurement setup is depicted in Fig. 8. By changing the input power and frequency, the dc voltage is measured by voltage meter.

Figure 9 shows the measured RF-DC conversion efficiency versus frequency at different input power levels for the fabricated rectifier.    When the input power varies from
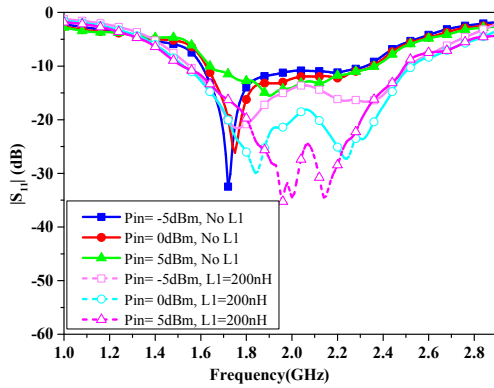


**Fig. 5.** Simulated reflection coefficient of the proposed rectifier with different inductor value L1 at the input power from –5 dBm to 5 dBm.
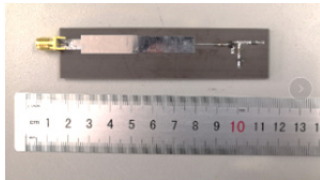


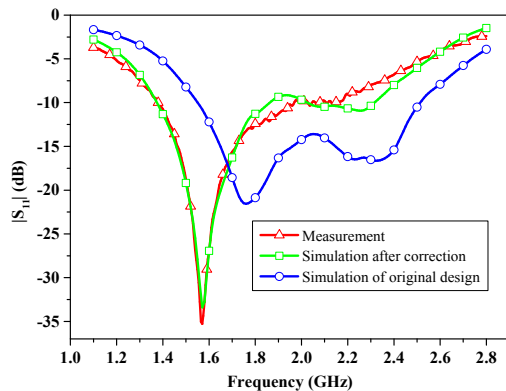**Fig. 6.** Photograph of the fabricated rectifier.



**Fig. 7.** Measured and simulated reflection coefficient $|S_{11}|$ versus frequency at the input power of –5 dBm for the designed wideband rectifier.



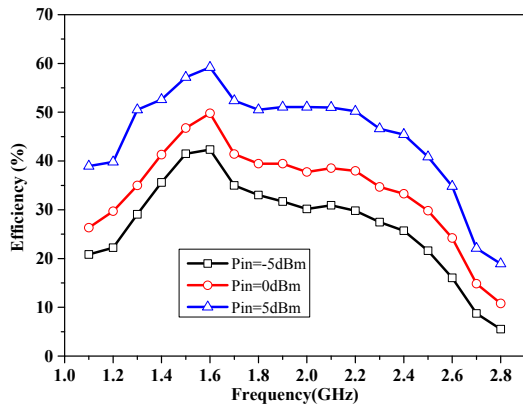**Fig. 8.** Photograph of the conversion efficiency measurement.

**Fig. 9.** Measured RF-DC conversion efficiency versus frequency for different input power levels (−5, 0 and 5 dBm).
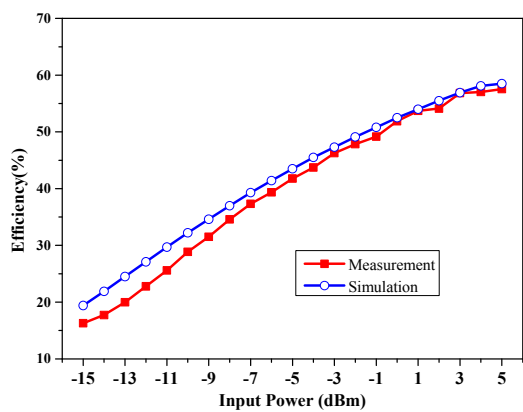
**Fig. 10.** Simulated and measured conversion efficiency at 1.6 GHz for different input power levels.
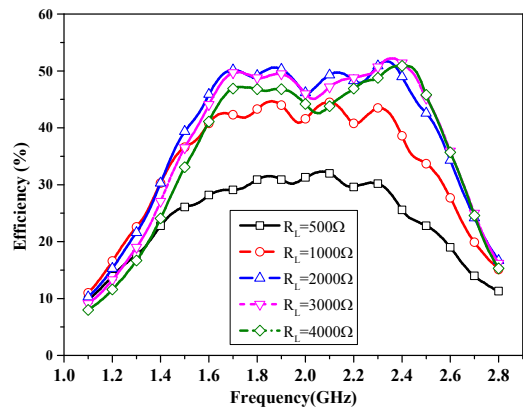
**Fig. 11.** Simulated conversion efficiency for different loads at the low input power level of −5 dBm.

−5 to 5 dBm, the power conversion efficiency is higher than 30% from 1.3–2.3 GHz, which reveals a broadband performance of the rectifier. As the input power increases up to 5 dBm, the conversion efficiency is higher than 50% from 1.3–2.2 GHz. Therefore, the rectifier can achieve high efficiency within a broad frequency band at low input power density.

The simulated and measured conversion efficiency with different input power level at 1.6 GHz is depicted in Fig. 10, where the measured results agree well with the simulated ones. When the input power level is decreased from 5 dBm to −15 dBm, the efficiency is reduced from 57.6% to 16.3% due to the nonlinearity of the rectifier. To further evaluate the load impedance on the conversion efficiency, the circuit simulation for different loads at the low input power level of −5.0 dBm is conducted with the simulated result plotted in Fig. 11. We can find that when the load impedance $R_L$ is below 2.0 kΩ, the average efficiency in the operated frequency band increases as the load $R_L$ becomes larger. As the load $R_L$ is up to 4.0 kΩ, a slight reduction of the average efficiency occurs.

Since the real high-frequency load resistance $R_L$ has apparently low parasitic capacitance, we further investigate the parasitic capacitance effect on the performance of the proposed rectifier. The simulated reflection coefficient and conversion efficiency results at the input power of −5 dBm are shown in Fig. 12 and Fig. 13 respectively. It can be observed that in Fig. 12, when the parasitic capacitance of $R_L$ increases, two resonant frequencies in the reflection coefficient are closer, leading to a slight reduction of operation bandwidth. When the parasitic capacitance increases up to 50 pF, the reduction of upper operated frequency with $|S_{11}|$ below −10 dB is 100 MHz while the lower operated frequency almost remains the same. Moreover, the frequency band for power conversion efficiency higher than 30% is changed from 1.44–2.64 GHz to 1.34–2.48 GHz. Compared with the case of no L1, the proposed rectifier with L1 features better impedance matching in the operated

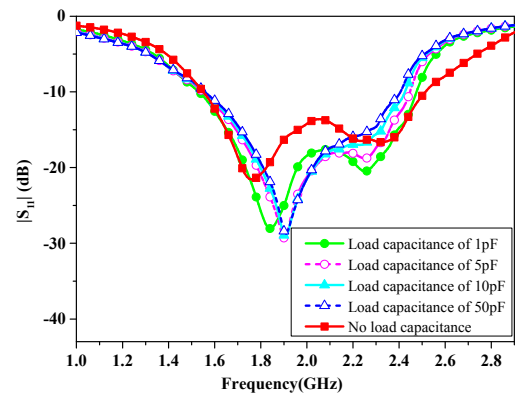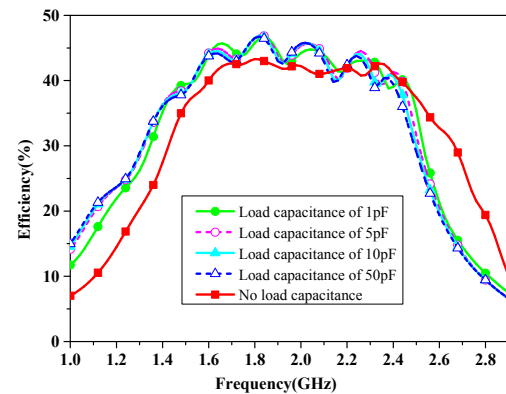**Fig. 12.** Simulated reflection coefficient for different parasitic capacitances of load at the low input power of −5 dBm.

**Fig. 13.** Simulated conversion efficiency for different parasitic capacitances of load at the low input power of −5 dBm.

| Frequency | 1.5 GHz | | | 2.0 GHz | | | 2.5 GHz | | |
|---|---|---|---|---|---|---|---|---|---|
| Model | I | II | III | I | II | III | I | II | III |
| DC | 0.353 | 0.321 | 0.332 | 0.375 | 0.355 | 0.363 | 0.350 | 0.293 | 0.344 |
| 1st harmonic | 0.004 | 0.032 | 0.195 | 0.005 | 0.086 | 0.167 | 0.007 | 0.128 | 0.142 |
| 2nd harmonic | 0.006 | 0.120 | 0.060 | 0.010 | 0.155 | 0.056 | 0.023 | 0.090 | 0.067 |
| 3rd harmonic | 0.002 | 0.005 | 0.014 | 0.010 | 0.016 | 0.026 | 0.010 | 0.046 | 0.029 |

**Tab. 1.** The DC and AC components of output voltage for different circuit simulation models.

frequency band even when the parasitic capacitance of load is up to 50 pF.

To analyze the effect of L1 on the influence of AC ripple, the high-order harmonics of the proposed rectifier are evaluated with the aid of ADS harmonic balance simulation. The harmonics simulation of three circuit models (model I, II and III) is conducted for comparison. The model III is the final circuit simulation model of the designed rectifier where both the actual parasitic effects of L1 (L1 = 200 nH) and C2 are considered. While in both model I and II, the inductor L1 is not introduced. In model I, the L1-C2 serial branch is replaced with an ideal lumped component C2 where no parasitic effect is considered. In model II, the actual parasitic effect of C2 is included.

The simulated DC and AC components of output voltage at three frequencies covering the operated frequency band are listed in Tab. 1 for the input power of −5 dBm. It can be seen that the AC component of model I for the three kinds of high-order harmonics is quite low. When the actual parasitic effect of C2 is introduced, the AC ripple of model II is largely increased especially for the 2nd harmonic, and the 1st harmonic at the higher frequency of 2.5 GHz is also increased greatly. When the actual parasitic effects of L1 (L1 = 200 nH) and C2 are both included, a big increase of the 1st harmonic occurs at 1.5 GHz and 2.0 GHz and a small increase occurs at 2.5 GHz compared with the results of model II. Moreover, a small reduction of the 2nd harmonic is observed. Thus, the introduction of L1 increases the AC component of the 1st harmonic for the proposed rectifier. In practical RF energy harvesting system, an additional low-pass filter can be employed to reduce the large AC output.

The comparison between our broadband rectifier and other related designs is shown in Tab. 2. It is worth pointing

out that the reported broadband rectifiers in Tab. 2 operate at various input power levels and frequency range for different application scenarios. As can be seen from this table, our design features a relatively wider bandwidth at the input power level around 5 dBm when compared with [8, 9, 14]. At lower input power level around −5 (−10) dBm, our design shows broader bandwidth at the expense of slightly decreased conversion efficiency when compared with [6]. References [12], [13] show higher conversion efficiency due to the increased input power level. Compared with these reported rectifiers, the proposed wideband rectifier has a single branch rectifier circuit, which features simple design complexity and concrete design rule. This will make it a great potential candidate for practical industrial applications.

# 4.  Conclusion

A single branch wideband rectifier using a novel wideband impedance matching network is proposed in this paper and its design process is provided in detail. The design process is validated by the fabricated rectifier which shows a fractional bandwidth of 55.6% at the input level of 5 dBm. With a concrete design rule and simple circuit structure, the presented wideband rectifier has great potential of ambient wireless energy harvesting application. Going forward, our study is on the improvement of conversion efficiency at lower input level, the reduction of AC ripple and the combination of the proposed rectifier with the antenna to implement high-efficiency broadband rectenna.

# Acknowledgments

| Ref. | Conversion efficiency (%) | Fractional bandwidth (%) | Input power (dBm) | Design equations | Design complexity |
|---|---|---|---|---|---|
| [6] | ≥40 | 32.5 | −10 | No | Complex |
| [8] | ≥50 | 34.5 | 4 | No | Simple |
| [9] | ≥50 | 44.9 | 3 | Yes | Medium |
| [11] | 21.5 (average) | 100 | −10 | No | Complex |
| [12] | ≥70 | 18.5 | 10 | No | Simple |
| [13] | ≥70 | 41.5 | 10 | Yes | Complex |
| [14] | ≥50 | 42.1 | 6.1 | No | Simple |
| This Work | ≥50 | 51.4 | 5 | Yes | Simple |
|  | ≥30 | 55.6 | −5 |  |  |

**Tab. 2.** Comparison of the proposed rectifier with other related broadband design.

# References

[1] CANSIZ, M., ALTINEL, D., KARABULUT KURT, G. Efficiency in RF energy harvesting systems: a comprehensive review. *Energy,* 2019, vol. 174, p. 292–309. DOI: 10.1016/j.energy.2019.02.100

[2] TAKHEDMIT, H., MERABET, B., CIRIO, L., et al. A 2.45-GHz dual-diode RF-to-DC rectifier for rectenna applications. In *The*

*40th European Microwave Conference*, Paris (France), 2010, p. 37–40. DOI: 10.23919/EUMC.2010.5616541

[3] SUN, H., ZHONG, Z., GUO, Y.-X. An adaptive reconfigurable rectifier for wireless power transmission. *IEEE Microwave and Wireless Components Letters*, 2013, vol. 23, no. 9, p. 492–494. DOI: 10.1109/LMWC.2013.2250272

[4] PALAZZI, V., HESTER, J., BITO, J., et al. A novel ultra-lightweight multiband rectenna on paper for RF energy harvesting in the next generation LTE bands. *IEEE Transactions on Microwave Theory and Techniques*, 2018, vol. 66, no. 1, p. 366–379. DOI: 10.1109/TMTT.2017.2721399

[5] KUHN, V., LAHUEC, C., SEGUIN, F., et al. A multi-band stacked RF energy harvester with RF-to-DC efficiency up to 84%. *IEEE Transactions on Microwave Theory and Techniques*, 2015, vol. 63, no. 5, p. 1768–1778. DOI: 10.1109/TMTT.2015.2416233

[6] SONG, C., HUANG, Y., CARTER, P., et al. A high-efficiency broadband rectenna for ambient wireless energy harvesting. *IEEE Transactions on Antennas and Propagation*, 2015, vol. 63, no. 8, p. 3486–3495. DOI: 10.1109/TAP.2015.2431719

[7] SONG, C., HUANG, Y., CARTER, P., et al. A novel six-band dual CP rectenna using improved impedance matching technique for ambient RF energy harvesting. *IEEE Transactions on Antennas and Propagation*, 2016, vol. 64, no. 7, p. 3160–3171. DOI: 10.1109/TAP.2016.2565697

[8] NIE, M. J., YANG, X. X., TAN, G. N. A broad band rectifier with wide input power range for electromagnetic energy harvesting. In *Proceedings of the 3rd Asia-Pacific Conference on Antennas and Propagation*. Harbin (China), 2014, p. 1187–1189. DOI: 10.1109/APCAP.2014.6992726

[9] LIN, Y. L., ZHANG, X. Y., DU, Z. X., et al. High-efficiency microwave rectifier with extended operating bandwidth. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2017, vol. 65, no. 7, p. 819–823. DOI: 10.1109/TCSII.2017.2716538

[10] SONG, C., HUANG, Y., ZHOU, J., et al. Improved ultrawideband rectennas using hybrid resistance compression technique. *IEEE Transactions on Antennas and Propagation*, 2017, vol. 64, no. 4, p. 2057–2062. DOI: 10.1109/TAP.2017.2670359

[11] DASKALAKIS, S. N., GEORGIADIS, A., COLLADO, A., et al. An UHF rectifier with 100% bandwidth based on a ladder LC impedance matching network. In *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*. Nuremberg (Germany), 2017, p. 411–414. DOI: 10.23919/EuMIC.2017.8230746

[12] SAKAKI, H., NISHIKAWA, K. Broadband rectifier design based on quality factor of input matching circuit. In 2014 *Proceedings of Asia–Pacific Microwave Conference*. Sendai (Japan), 2014, p. 1205–1207.

[13] WU, P., HUANG S. Y., ZHOU, W., et al. Compact high-efficiency broadband rectifier with multi-stage-transmission-line matching. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2019, vol. 66, no. 8, p. 1316–1320. DOI: 10.1109/TCSII.2018.2886432

[14] WU, Y. B., WANG, J., LIU, Y. Y., et al. A novel wideband rectifier design with two-stage matching network for ambient wireless energy harvesting. In *2018 Progress in Electromagnetics Research Symposium (PIERS-Toyama)*. Toyama (Japan), 2018, p. 1351–1354. DOI: 10.23919/PIERS.2018.8597623

[15] WU, Y., LIU, Y., LI, S., et al. A generalized dual-frequency transformer for two arbitrary complex frequency-dependent impedances. *IEEE Microwave and Wireless Components Letters*, 2009, vol. 19, no. 12, p. 792–794. DOI: 10.1109/LMWC.2009.2034034

[16] KEYSIGHT ADS (for 2011 and later) – Library. Available at: https://www.murata.com/en-us/tool/librarydata/library-keysight2?intcid5=com_xxx_xxx_cmn_hd_xxx

[17] CCI_RF_Library.zip. [Online] Available at: https://www.coilcraft.com/models_ads_library.cfm

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