An Independently Biased 3-stacked GaN HEMT Power Amplifier for Next-Generation Wireless Communication Systems

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Abstract. *In this paper, a design of 3-stacked GaN high-electron-mobility transistor radio-frequency power amplifier employing an independently biased technique is presented to meet stringent requirements of next-generation wireless communication systems. The ability of independently adjusting operation conditions for each transistor of the proposed amplifier makes it possible to operate not only for high efficiency, high linearity but also for both improved efficiency and linearity. Efficiency can be optimized through varying drain bias voltages. Linearity, however, can be optimized independently through varying gate bias voltages. Importantly, both efficiency and linearity can be optimized simultaneously by making a compromise between drain and gate bias voltages. In contrast to conventional methods, the proposed configuration still ensures a compact size for design of the power amplifier. This can be feasible because the proposed solution is introduced in the device level using a MMIC technology. These superior advantages make the proposed PA a promising candidate for using in transceiver of the next-generation wireless communications systems.*

Keywords

Power amplifier, GaN HEMT, independently biased, IMD3, linearity, efficiency

1. Introduction

Next-generation wireless communication systems such as fifth generation (5G) [1], [2] always require power amplifier (PA) of the transceiver to meet various stringent critical standards. Among them, efficiency and linearity are the most important parameters [3–5]. These two parameters are in contradiction because in order to deliver high efficiency the PA needs to operate in the saturated region leading to poor linearity. On the other hand, the PA needs to operate in linear region to remain its linearity at the cost of reduced efficiency. In order to surmount this inherent drawback, various state of the art solutions have been proposed including Doherty, envelope tracking and digital pre-distortion (DPD) techniques.

Doherty amplifier [6–8] improves linearity by using a back-off technique to move operation condition to the linear region at the cost of reduced output power and efficiency. The reduced efficiency at the linear region in the Doherty can be improved by using the envelope tracking technique [9–11]. This technique is implemented by employing an adaptive bias control for the saturated PA. Whenever the input power of a non-constant envelope modulation signal with high is pulled to the linear region, a control signal will be sent to the programmable power supply of the PA to change its operation condition. Thanks to this method, peak efficiency of the PA is shifted to the linear region whenever the input power drops, owing to the change of the operation condition. However, the main disadvantage of this technique is that it is relatively hard to keep synchronization between the digital line and the RF line. This becomes more serious when PA operates at higher frequencies. Moreover, this technique requires several hardware components leading to higher power consumption and thus increasing complexity of the circuit. Another recent solution to improve linearity of the PA is using the DPD technique [12–14]. This technique uses a pre-distorter to produce amplitude distortion (AM-AM) and phase distortion (AM-PM) which are inverse of that of the PA. By using such a technique, both amplitude and phase distortions of the PA can be completely or partly compensated. Although existing PAs employing DPD can offer very high linearity performance, efficiency of these PAs is difficult to optimize or improve. This makes these PAs to operate at low efficiency. In this paper, a novel approach is introduced to simultaneously improve efficiency and linearity of the PA for efficiently using in next-generation wireless communication systems. The proposed approach can be used to not only improve both efficiency and linearity but also ensure low-complexity and compactness. The approach focuses on the solution at the device level instead of at the system and circuit levels as the mentioned methods. This helps to reduce both complexity of the system and the circuit size.

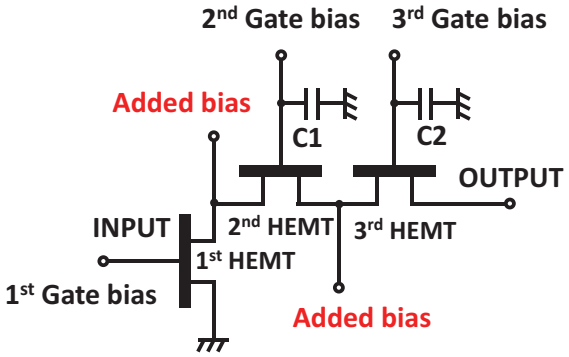

Fig. 1. Proposed 3-stacked GaN HEMT structure.

So far, various existing stacked-type device configurations have been proposed to improve performance of the PA including Darlington [15], [16], cascode [17], [18] and hybrid [19] configurations.

The Darlington configuration can handle very high current capability that is highly suitable for power amplifier design. The cascode configuration, however, can offer various advantages such as wide bandwidth and high gain. The hybrid configuration which combines a bipolar junction transistor (BJT) and a field effect transistor (FET) can offer low output impedance and low DC power consumption. Although these configurations have been proved to deliver excelent advantages, they still exhibit inherent drawbacks for high-frequency power amplifier design. One of the most critical drawbacks of these configurations is that they are not able to independently adjust bias condition of each transistor in the configuration. This reduces degrees of freedom when optimizing performance improvement. Recently, independently biased InGaP/GaAs HBT cascode [20] and independently biased 3-stacked InGaP/GaAs Heterojunction bipolar transistor (HBT) [21] configurations have been introduced for PA design for modern wireless communication systems.

Theses proposed configurations can offer the ability of independent control of bias condition. Nevertheless, they still exhibit low output power due to low power capability of bipolar transistors.

In addition to these configurations, an independently biased 3-stacked GaN high-electron-mobility transistor (HEMT) has been introduced in [22]. However, this structure was just in the form of a bare chip and the investigated results were performed at the chip level but not the circuit level. In this paper we practically implement a design of a PA based on the independently biased technique for a 3-stack GaN HEMT structure as presented in [22]. The structure is described in Fig. 1. Three GaN HEMT devices are connected to each other in a cascode-type topology. In addition to the conventional bias terminals including gate bias and drain bias, two additional bias terminals are inserted to two floating points between the first and the second transistors and between the second and the third transistors.

Owing to this approach, bias condition of each transistor in the proposed configuration can be independently controlled. An investigation on how such an independently biased approach in the 3-stacked GaN HEMT configuration can improve both efficiency and linearity is carried out. After careful investigations for performance improvement regarding the change of individual bias voltages of each transistor, an optimum operation condition can be realized. This means, the proposed structure can deliver optimum performance for efficiency or linearity or both of them just by adjusting bias condition of each transistor. This clearly exhibits superior advantages over existing traditional methods.

The rest of the paper is organized as follow: Section 2 describes in details the PA implemented on the proposed configuration. Investigation of efficiency and linearity performance of the PA is performed in Sec. 3 and Sec. 4, respectively. After that Section 5 presents experimental validation. Finally, Section 6 concludes the paper.

2. Descriptions of the PA

2.1 3-stacked GaN HEMT MMIC Chip

Schematic of the 3-stacked GaN HEMT configuration is illustrated in Fig. 2. In practice, the 3-stacked GaN HEMT structure is implemented using a MMIC (Monolithic Microwave Integrated Circuit) technology from WIN Semiconductor Corp. foundry service [23]. The process design kit (PDK) of the service includes following information: metal thickness = 4 μm, substrate thickness = 100 μm.

The schematic and MMIC layout of this structure are described in Fig. 1. As can be seen in the figure showing the MMIC layout, two RF-bypass capacitors are realized using a metal-insulator-metal (MIM) technology while input and output terminals are ground-signal-ground (GSG) connections for chip evaluation using GSG probes. Interconnects inside the MMIC chip are made using metallic transmission lines. Three GaN HEMTs have the same size of 0.25 μm × 0.75 μm × 4 fingers. The total size of the MMIC chip is 674 μm × 1025 μm.

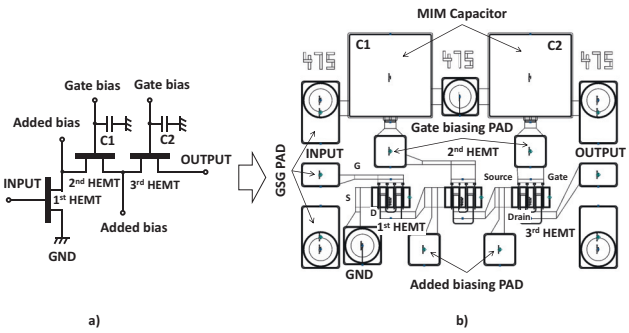

Fig. 2. MMIC layout of the proposed configuration: a) Schematic; b) MMIC layout.

2.2 Power Amplifier Schematic

Figure 3 shows descriptions of the proposed amplifier which is implemented using the 3-stacked GaN HEMT topology as an active device. The MMIC chip is connected to the external components including off-chip input/output matching networks and biasing lines via gold bonding wires (BW) with a diameter of 30 µm. Input matching network (IMN) and output matching network (OMN) are implemented using off-chip lumped components from Murata libraries [24].

Values of the IMN components are: L_1 : LQW18AN4N3C00 (4.3 nH), C_1 : GRM1555C1HR90WA01 (0.9 pF) and values of the OMN components are: L_2 : LQW18AN12NG00 (12 nH), C_2 : GRM1555C1HR30WA01 (0.3 pF). Gate bias of the first transistor and drain bias of the third transistor are implemented using Bias-Tees incorporating a RF choke inductor and a block capacitor C_b. In addition, drain bias lines of the first and the second transistors are implemented using two quarter wavelength transmission lines. Here, it is noted that the IMN and OMN are designed to match source and load impedances of the MMIC chip to 50 Ω system at the fundamental frequency only without using any harmonic termination elements. This is why the IMN and OMN just include a combination of an inductor and a capacitor as indicated in the figure.

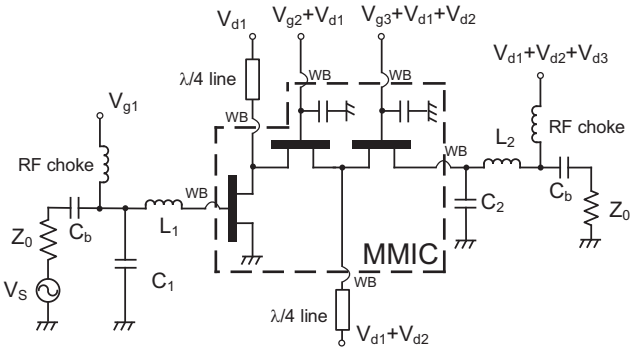

Fig. 3. PA schematic.

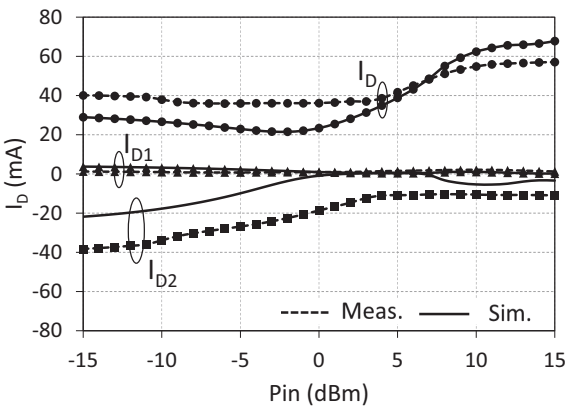

Fig. 4. Simulated and measured drain currents of the proposed configuration.

Optimum fundamental source and load impedances for efficiency are found by using a simulated load/source pull method based on non-linear models of GaN HEMT provided by WIN Semiconductor Corp. in Keysight ADS 2016 simulator. These values are: $Z_S = 79.3 + j138.6\ \Omega$, $Z_L = 134.7 + j174.1\ \Omega$ where Z_S and Z_L are the optimum source and load impedances, respectively.

3. Efficiency Evaluation

It is expected that efficiency of the PA can be improved by adjusting two added bias terminals functioned as two drain bias voltages of the first and second transistors V_{d1} and V_{d2}. This is because when adjusting these bias voltages, there is a re-contribution of quiescent drain currents among transistors leading to a re-contribution of DC power consumption. In other words, there should be an inverse quiescent drain current flowing to the bias terminal when changing bias voltages leading to lower DC power consumption. Consequently, efficiency is enhanced. This is validated by looking at Fig. 4 which shows the simulated and measured of drain currents flowing inside the configuration. Here, I_{D1}, I_{D2} and I_D denote drain currents of the first, second and third transistor, respectively. It can be clearly seen that, I_{D2} has a minus sign when input power varies. This indicates that there is an inverse drain current in the second transistor as expected.

3.1 V_{d1} Variation

The most important feature of the proposed amplifier is the high degree of freedom in bias adjustment for each transistor leading to the PA performance improvement. In the proposed circuit topology as indicated in Fig. 1, two added bias terminals have been included in order to bias the drain terminals of the first (V_{d1}) and the second (V_{d2}) transistors. This means, by appropriately controlling these bias values (V_{d1} and V_{d2}), efficiency expressed in terms of power added efficiency (PAE) and output power can be significantly improved.

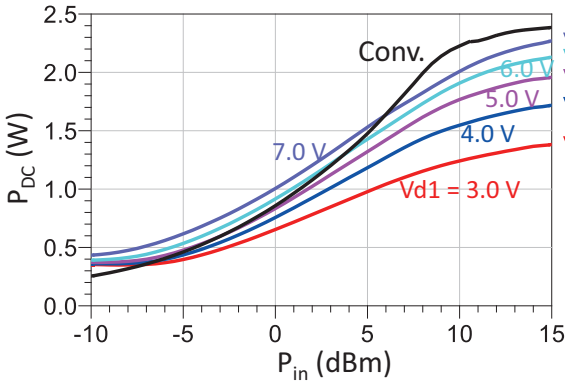

Fig. 5. DC power of the conventional and proposed 3-stacked PA vs. input power with variation of V_{d1}. The black curve represents DC power of the conventional configuration.

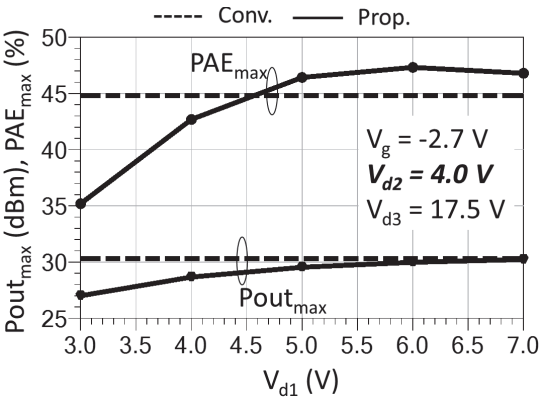

Fig. 6. Maximum PAE and Pout as a function of varied V_{d1}. Performance comparison with a conventional structure is also shown.

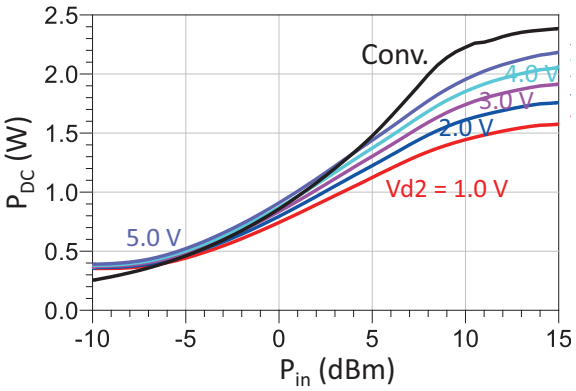

Fig. 7. DC power of the conventional and proposed 3-stacked PA vs. input power with variation of V_{d2}. The black curve represents DC power of the conventional configuration.

Firstly, the variation of V_{d1} will be investigated. One of the main contributions of this independent bias control is to re-contribute the DC power consumption of the PA. This helps to increase efficiency while still ensure sufficient output power. This re-contribution of the DC power can be seen in Fig. 5. Decreasing V_{d1} while keeping V_{d2} and V_d unchanged results in lower DC power at high input power region. This means that maximum efficiency (PAE) can be enhanced as the maximum PAE occurs at the high input power region. On the other hand, a conventional 3-stacked configuration which has a similar topology with the proposed 3-stacked one as indicated in Fig. 1 but without using two added bias terminals is not able to make this re-contribution of the DC power. Here, it is noted that all three transistors of the proposed configuration are biased in a class-AB. All three gate bias voltages are set to −2.7 V and the third drain bias voltage (V_{d3}) is kept at a constant value of 27.5 V. Similar bias conditions are made for both the conventional and proposed configurations in order to make a logical comparison between them. The effect of DC power reduction with respect to the change of V_{d1} on PA performance can be clearly seen in Fig. 6. As can be seen in the figure, when V_{d1} varies from 3.0 V to 7.0 V, both PAE and Pout can be significantly changed. When V_{d1} increases, PAE_{max} can be higher than that of the conventional one while $Pout_{max}$ can still remain the same level as the conventional one. To make a superior trade-off between efficiency and output power compared with that of the conventional one, V_{d1} should be set to 5.5 V.

3.2 V_{d2} Variation

After setting V_{d1}, V_{d2} then will be considered for efficiency improvement. Figure 7 illustrates the effect of V_{d2} on the DC power re-contribution inside the PA. It once gain can be seen that decreasing V_{d1} while keeping V_{d1} and V_d results in lower DC power at high input power region. This re-contribution of DC power also helps to increase PAE at the cost of low output power. The dependence of maximum PAE and maximum Pout of the conventional and proposed 3-stacked GaN HEMT configurations with variation of V_{d2} is shown in Fig. 8. In this figure V_{d1} is kept constant at 5.5 V.

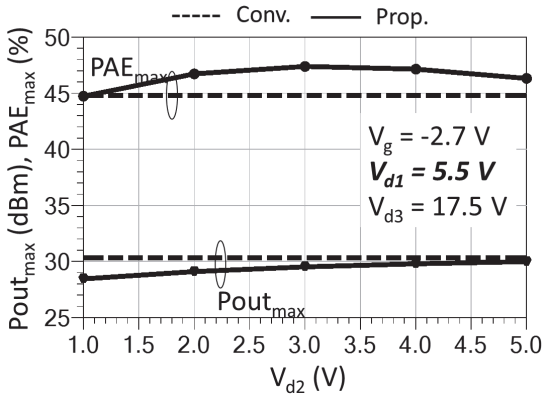

Fig. 8. Maximum PAE and Pout as a function of varied V_{d2}. Performance comparison with a conventional structure is also shown.

The figure shows that when V_{d2} varies from 1 to 5 V, maximum PAE first increases and reaches maximum values at the middle region and drop at high V_{d2} while maximum Pout increases with the increasing V_{d2}. This implies that to remain sufficient output power without degradation of efficiency over the conventional one, V_{d2} should be chosen at 4.0 V.

4. Linearity Evaluation

If V_{d1} and V_{d2} are the main factors for efficiency improvement because of the re-contribution of DC power, gate bias voltages V_{g1}, V_{g2} and V_{g3} are critical factors for linearity improvement. This is due to the fact that gate voltages control the non-linearity of each transistor transconductance. Hence, by adjusting gate bias voltages, linearity of the proposed PA can be enhanced along with the efficiency improvement. Here, linearity performance of the PA is evaluated in terms of the third-order intermodulation distortion (IMD3) with 4 MHz spacing channel.

4.1 V_{g1} Variation

Figure 9 indicates the dependence of IMD3 on the variation of V_{g1}. As can be seen, V_{g1} has a significant contribution

to the IMD3 improvement in the low power region. In addition, the "sweet point" in the IMD3 curve can also be tuned by changing V_{g1}. This fact is easy to understand as the first transistor plays a critical role in linearity of the PA.

4.2 V_{g2} Variation

The dependence of IMD3 on the variation of V_{g2} is shown in Fig. 10. As expected, V_{g2} has a less contribution to the IMD3 compared with V_{g1}. It also has a slight effect on IMD3 at low power region when adjusting at high values. This is because when setting the V_{g2} at high values, operation point of the transistors shifts to the linear region regarding the transfer characteristic. However, this may lead to lower efficiency due to the high quiescent drain current.

4.3 V_{g3} Variation

The dependence of IMD3 on the variation of V_{g3} is described in Fig. 11. As clearly seen that V_{g3} has nearly no contribution to IMD3 improvement. It has a very slight effect on IMD3 in the power region close to "sweet point". This has been pointed out previously, V_{g1} and V_{g2} are the dominant factors for IMD3 improvement compared to the V_{g3}.

In summary, from the above discussions, it can be concluded that efficiency of the PA can be tuned by adjusting V_{d1} and V_{d2} whereas its linearity can be tuned by adjusting V_{g1} and V_{g2}. These gate and drain bias voltages can be tuned independently in practice thanks to the proposed approach.

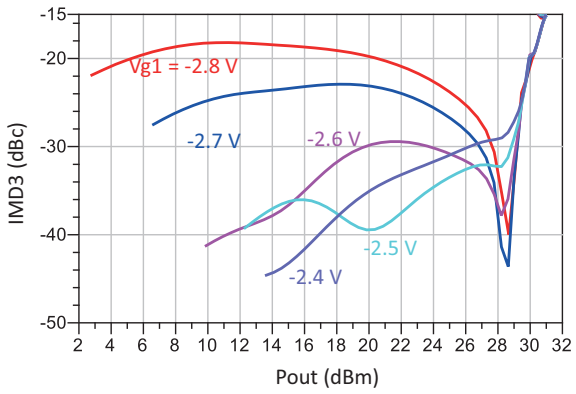

Fig. 9. Investigation of IMD3 with variation of V_{g1}.

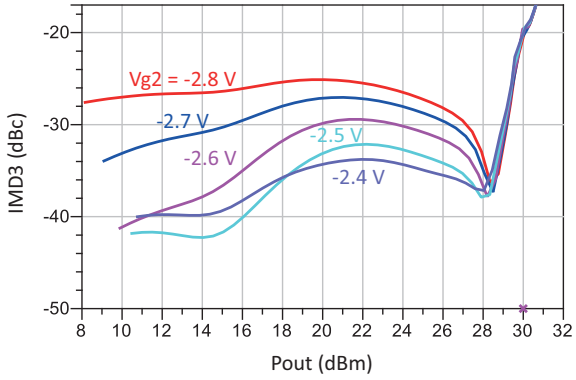

Fig. 10. Investigation of IMD3 with variation of V_{g2}.

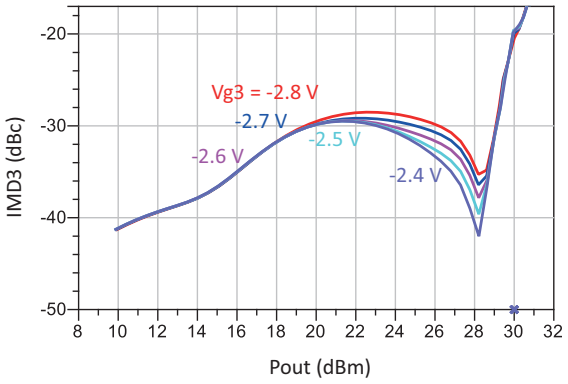

Fig. 11. Investigation of IMD3 with variation of V_{g3}.

This means the PA can operate for high efficiency, high linearity or both optimized efficiency and linearity.

5. Experiment

5.1 PA Prototype

After considering optimum bias conditions for the proposed PA, a prototype of the PA has been fabricated as indicated in Fig. 12. The external Bias-Tees for biasing the gate of the first transistor and the drain of the third transistor are not shown in the figure. Female and male SMA connectors function as the input and output ports, respectively.

The prototype was fabricated on a Megtron6 substrate from Panasonic with following parameters: dielectric constant = 3.7, substrate thickness = 0.75 mm, dissipation factor = 0.002 and copper thickness = 35 μm. In the measurement of the PA prototype, bias condition of each transistor which are determined from the previous section are used. The bias conditions for the proposed configuration are as follow: $V_g = -2.8$ V, $V_{d1} = 5.5$ V, $V_{d2} = 4.0$ V, $V_d = 17.5$ V while the bias conditions for the conventional one are as follow: $V_g = -2.8$ V, $V_d = 27$ V which is equivalent to $V_{d1} + V_{d2} + V_{d3}$.

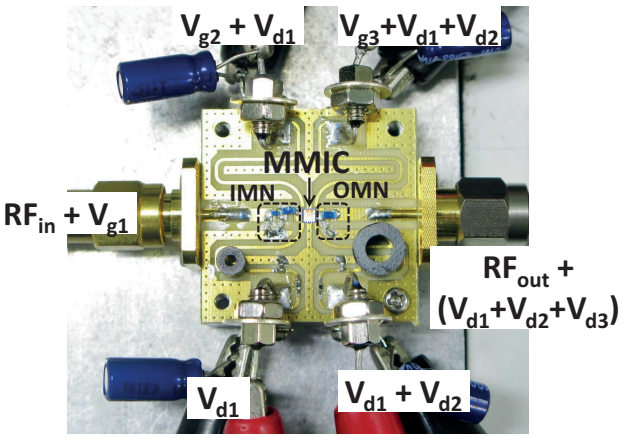

Fig. 12. Fabricated PA prototype.

5.2 Experimental Setup

The experimental setup for large-signal (efficiency) measurement of the PA prototype is described in Fig. 13. A microwave signal generator (SG) is employed to input RF signal to the PA at an operation frequency 1.6 GHz. Two Bias-Tee symbols are clearly visible in the figure. Two RF directional couplers are used to split the input and output RF signals for measurement of the input and output power.

Power measurement is made by using power sensors combined with a power meter. All components for power measurement are carefully calibrated prior to make actual measurements. A spectrum analyzer (SA) is employed to check the output spectrum as well as to verify if the PA is unintentionally oscillated during the large-signal measurement. For IMD3 measurement with two-tone signal, another SG will be used at the input, two signals are combined through a power combiner before inputting to the PA. Output spectrum will be displayed on the SA.

5.3 Measured Results

Efficiency mode

In the efficiency mode or high efficiency mode, the PA will be tuned through adjusting V_{d1} and V_{d2} while keeping V_{g1} and V_{g2} at high values. This mode helps the PA to deliver high efficiency but low linearity. The measured input-output performance including PAE, output power and gain are shown in Fig. 14 which shows the measured and simulated PAE, P_{out} and gain of the designed PA. The PA is practically biased for optimized efficiency which is found from the previous sections as follow: V_g = −2.8 V, V_{d1} = 5.5 V, V_{d2} = 4.0 V, V_d = 17.5 V. As can be seen in the figure, measured results agree well with the simulated one. This implies that the simulations predict well performance of the proposed 3-stacked Gan HEMT PA.

There are some discrepancies between simulation and measurements which are possibly caused by losses in the PA assembly procedure, in realistic lumped components and inaccuracy of MMIC chip model. Figure 15 shows the simultaneous efficiency and IMD3 as a function of output power. It clearly can be seen that at the efficiency mode, although efficiency can be high, linearity of the PA becomes very poor. IMD3 level is just −5 dBc when PAE reaches 20 %.

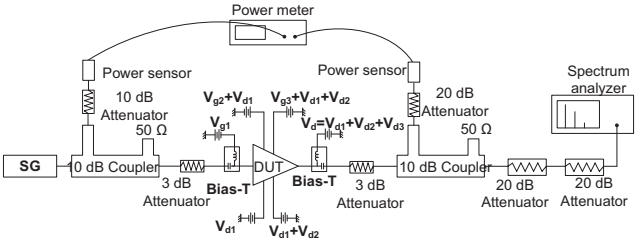

Fig. 13. Experimental setup.

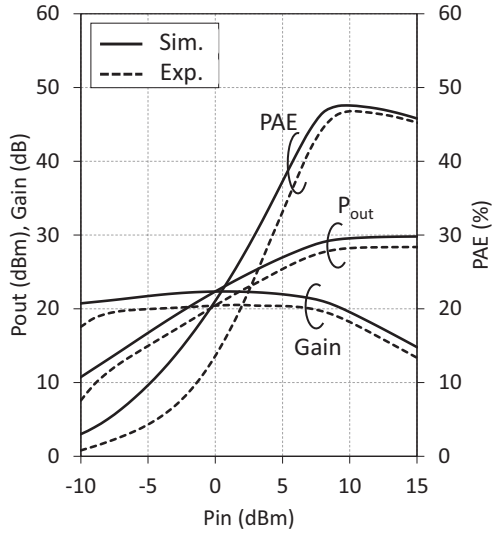

Fig. 14. Measured and simulated input-output characteristics.

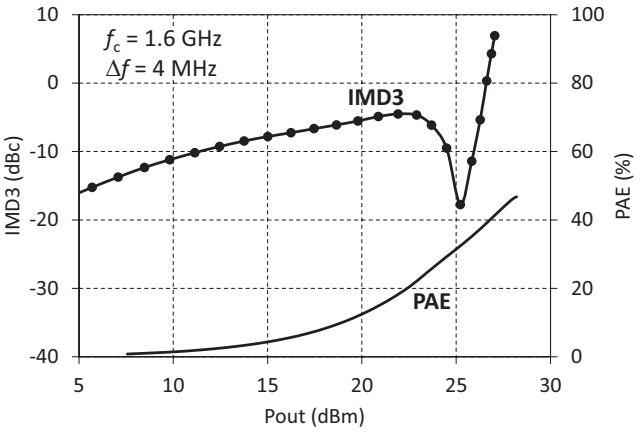

Fig. 15. Measured IMD3 and efficiency of the PA in saturated mode.

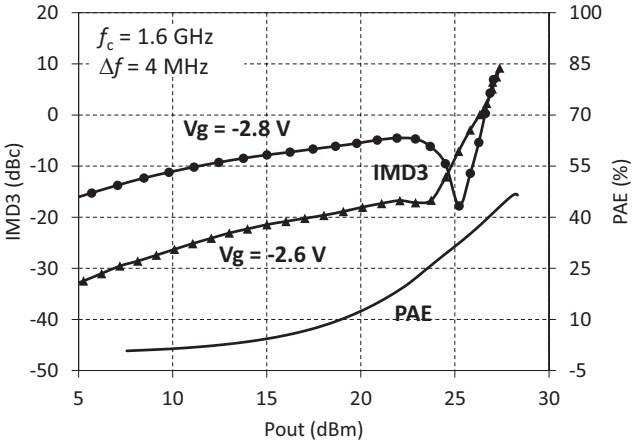

Fig. 16. Measured IMD3 and efficiency of the PA in linearity mode.

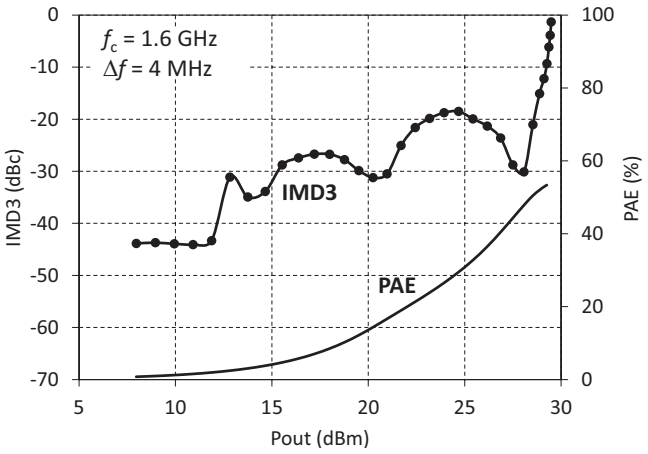

Fig. 17. Measured IMD3 and efficiency of the PA in optimum mode.

Linearity mode

In the linearity mode for high linearity, the PA will be tuned through adjusting V_g. This mode helps the PA to deliver higher linearity than the efficiency mode. This is illustrated in Fig. 16 which shows the measured efficiency and IMD3 at $V_g = -2.8$ V and $V_g = -2.6$ V. It can be seen in the figure that when tuning $V_g = -2.8$ V to $V_g = -2.6$ V, linearity of the PA can be improved without degrading efficiency. This means both efficiency and linearity of the PA can be simultaneously and independently improved.

Optimum mode

In the optimum mode, both gate bias voltage V_g and drain bias voltage V_d is adjusted independently to simultaneously improve efficiency and linearity of the PA. In this mode, V_g is tuned to a lower value of −2.4 V to obtain high linearity while V_{d3} is slightly tuned to 14 V instead of 17.5 V as indicated in previous investigations. The important point here is not only the V_{d1} and V_{d2} are tuned but also V_{d3} without affecting linearity performance. This is shown in Fig. 17 where measured IMD3 and efficiency of the PA in the optimum mode. The figure indicates that both linearity and efficiency of the PA can be both improved compared to that in the efficiency and linearity modes. PAE can reach 21% at an IMD3 level of −25 dBc.

6. Conclusion

An independently biased 3-stack GaN HEMT power amplifier is presented in this paper. The PA aims at designing for using in the next-generation wireless communication systems. By employing the independently biased method, operation condition of each transistor can be tuned independently leading to high degree of freedom in improving PA performance. By adjusting gate bias voltages V_g, linearity of the PA can be improved while tuning the drain bias voltages V_d, efficiency of the PA can be improved. This brings three promising modes of operation for the designed PA, that are efficiency, linearity and optimum modes. By appropriately adjusting both V_g and V_d, not only efficiency but also linearity of the PA can be simultaneously improved. Additionally, the proposed amplifier can be implemented in a compact size because the solution is given in the device level using the MMIC technology. Thanks to these promising advantages, the proposed PA can become a promising candidate for using in transceivers of the next-generation wireless communication systems.

Acknowledgments

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References

[1] FAN, Y., YANG, L., ZHANG, D., et al. An angle rotate-QAM aided differential spatial modulation for 5G ubiquitous mobile networks. *Mobile Networks and Applications*, 2019, p. 1–3. DOI: 10.1007/s11036-019-01399-0

[2] XU, X., LIU, X., XU, Z., et al. Joint optimization of resource utilization and load balance with privacy preservation for edge services in 5G networks. *Mobile Networks and Applications*, 2020, vol. 25, p. 713–724. DOI: 10.1007/s11036-019-01448-8

[3] BIRAFANE, A., KOUKI, A. B. On the linearity and efficiency of outphasing microwave amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 2004, vol. 52, no. 7, p. 1702–1708. DOI: 10.1109/TMTT.2004.830485

[4] FU, J. S., MORTAZAWI, A. Improving power amplifier efficiency and linearity using a dynamically controlled tunable matching network. *IEEE Transactions on Microwave Theory and Techniques*, 2008, vol. 56, no. 12, p. 3239–3244. DOI: 10.1109/TMTT.2008.2007094

[5] FAGER, C., ERICKSSON, T., BARRADAS, F., et al. Linearity and efficiency in 5G transmitters: new techniques for analyzing efficiency, linearity, and linearization in a 5G active antenna transmitter context. *IEEE Microwave Magazine*, 2019, vol. 20, no. 5, p. 35–49. DOI: 10.1109/MMM.2019.2898020

[6] KIM, B., KIM, J., KIM, I., et al. The Doherty power amplifier. *IEEE Microwave Magazine*, 2006, vol. 7, no. 5, p. 42–50. DOI: 10.1109/MW-M.2006.247914

[7] NGUYEN, D. P., CURTIS, J., PHAM, A. V. A Doherty amplifier with modified load modulation scheme based on load-pull data. *IEEE Transactions on Microwave Theory and Techniques*, 2018, vol. 66, no. 1, p. 227–236. DOI: 10.1109/TMTT.2017.2734663

[8] ABDULKHALEG, A. M., YAHYA, M. A., AL-YASIR, Y. I. A., et al. Doherty power amplifier for LTE-advanced systems. *Technologies, MDPI*, 2019, vol. 7, no. 3, p. 1–13. DOI: 10.3390/technologies7030060

[9] KIM ,D., KANG, D., CHOI, J., et al. Optimization for envelope shaped operation of envelope tracking power amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 2011, vol. 59, no. 7, p. 1787–1795. DOI: 10.1109/TMTT.2011.2140124

[10] PARK, B., KIM, D., KIM, S., et al. High-performance CMOS power amplifier with improved envelope tracking supply modulator. *IEEE Transactions on Microwave Theory and Techniques*, 2016, vol. 64, no. 3, p. 798–809. DOI: 10.1109/TMTT.2016.2518659

[11] ALT, A., HIRSHY, H., JIANG, S., et al. Analysis of gain variation with changing supply voltages in GaN HEMTs for envelope tracking power amplifiers. *IEEE Transactions on Microwave Theory and Techniques*, 2019, vol. 67, no. 7, p. 2495–2504. DOI: 10.1109/TMTT.2019.2916404

[12] WOOD, J. System-level design considerations for digital predistortion of wireless base station transmitters. *IEEE Transactions on Microwave Theory and Techniques*, 2017, vol. 65, no. 5, p. 1880–1890. DOI: 10.1109/TMTT.2017.2659738

[13] ABDELAZIZ, M., ANTTILA, L., BRIHUEGA, A., et al. Digital predistortion for hybrid MIMO transmitters. *IEEE Journal of Selected Topics in Signal Processing*, 2018, vol. 12, no. 3, p. 445–454. DOI: 10.1109/JSTSP.2018.2824981

[14] LE, D.H., HOANG, V. P., NGUYEN, M. H., et al. Linearization of RF power amplifiers in wideband communication systems by adaptive indirect learning using RPEM algorithm. *Mobile Networks and Applications*, 2020, vol. 25, p. 1988–1997. DOI: 10.1007/s11036-020-01545-z

[15] ARMIJO, C. T., MEYER, R. G. A new wide-band Darlington amplifier. *IEEE Journal of Solid-State Circuits*, 1989, vol. 4, no. 24, p. 1105–1109. DOI: 10.1109/4.34098

[16] WENG, S. H., CHANG, H. Y., CHIONG, C. C., et al. Gain-bandwidth analysis of broadband Darlington amplifiers in HBT-HEMT process. *IEEE Transactions on Microwave Theory and Techniques*, 2012, vol. 60, no. 11, p. 3458–3473. DOI: 10.1109/TMTT.2012.2215051

[17] AHY, R. M., NISHIMOTO, C., RIAZIAT, M., et al. 100-GHz high-gain InP MMIC cascode amplifier. *IEEE Journal of Solid-State Circuits*, 1991, vol. 26, no. 10, p. 1370–1378. DOI: 10.1109/4.90088

[18] SOWLATI, T., LEENERTS, D. A 2.4-GHz 0.18-µm CMOS self-biased cascode power amplifier. *IEEE Journal of Solid-State Circuits*, 2003, vol. 38, no. 8, p. 1318–1324. DOI: 10.1109/JSSC.2003.814417

[19] ROOZBAHANI, R. G. BJT-BJT, FET-BJT, and FET-FET. *IEEE Circuits and Devices Magazine*, 2004, vol. 20, no. 6, p. 17–22. DOI: 10.1109/MCD.2004.1364771

[20] LUONG, D. M., TAKAYAMA, Y., ISHIKAWA, R., et al. Power gain performance enhancement of independently biased heterojunction bipolar transistor cascode chip. *Japanese Journal of Applied Physics*, 2015, vol. 54, no. 4S, p. 1–8. DOI: 10.7567/JJAP.54.04DF11

[21] LUONG, D. M., TAKAYAMA, Y., ISHIKAWA, R., et al. Microwave characteristics of an independently biased 3-stack InGaP/-GaAs HBT configuration. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2017, vol. 64, no. 5, p. 3487–3495. DOI: 10.1109/TCSI.2016.2637406

[22] HOANG, N. H., LUONG, D. M., DUONG, B. G. A novel independently biased 3-stack GaN HEMT configuration for efficient design of microwave amplifiers. *Applied Sciences, MDPI*, 2019, vol. 9, no. 7, p. 1–16. DOI: 10.3390/app9071510

[23] *WIN Semiconductors.* [Online] Cited 2020-06-23. Available at: http://www.winfoundry.com/

[24] *Murata Inovator in Electronics.* [Online] Cited 2020-06-23. Available at: https://www.murata.com/

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