Modeling Networks of Probabilistic Memristors in SPICE

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Abstract. *Efficient simulation of stochastic memristors and their networks requires novel modeling approaches. Utilizing a master equation to find occupation probabilities of network states is a recent major departure from typical memristor modeling [Chaos, solitons fractals 142, 110385 (2021)]. In the present article we show how to implement such master equations in SPICE – a general purpose circuit simulation program. In the case studies we simulate the dynamics of ac-driven probabilistic binary and multi-state memristors, and dc-driven networks of probabilistic binary and multi-state memristors. Our SPICE results are in perfect agreement with known analytical solutions. Examples of LTspice code are included.*

Keywords

Memristors, SPICE, networks, probabilistic computing

1. Introduction

SPICE simulation [1,2] is a powerful tool in the hands of an electrical engineer. In the last decade significant progress has been made in developing SPICE models of memristive devices [3–14], as well as memcapacitive and meminductive elements [9, 15]. The common feature of these previous approaches is the use of differential equations to describe the deterministic evolution of internal state(s) of memory devices [16, 17].

However, there is a strong indication that the deterministic description fails when applied at least to certain realizations of resistors with memory [18–20]. In particular, it was shown experimentally that when a constant voltage is applied to such devices, their state changes in a step-like fashion at random times. In one group of devices, a Poisson distribution of switching times was observed [18–20]. Furthermore, another group of devices is characterized by a log-normal distribution [21]. Several theoretical models were pushed forward to account for the randmoness in the memristor switching [22, 23]. The dynamics of networks with discrete-state memristors can be imagined as a sequence of transitions between network states. Recently, we have introduced a master equation approach for the occupation probabilities of the network states [24] that can be used to describe circuits that include binary and multi-state memristors, resistors, voltage and current sources, and possibly some other components [1]. The master equation was solved analytically for networks containing N binary memrstors connected in-series or in-parallel driven by a constant voltage source [24]. It has been demonstrated in Ref. [24] that the master equation solution allows to calculate many quantities of interest including various mean switching times, mean current, resistance, etc. There are two major advantages of the master equation compared to stochastic/Monte Carlo simulations: *i*) in principle, the master equation can be solved analytically (see [24] for examples), and *ii*) using the master equation, many network characteristics can be found in a single calculation without the need for averaging. In the case of symmetries in the circuit, the additional benefit of the master equation is its compactness. This means that a single degree of freedom is required to describe equivalent circuit configurations. In this article (which is our second work in a series dedicated to probabilistic memristive networks), we introduce a methodology to simulate the probabilistic memristive networks in SPICE. The paper is organized as follows. We start with an overview of the master equation in relation to binary and multi-state probabilistic memristor networks. This is followed by a description of the SPICE implementation scheme supplemented by several examples. In particular, we consider individual probabilistic binary and tri-state memristors driven by ac-voltage, and dc-driven networks thereof. LTspice codes for some of our examples are provided in the Appendix. The approach presented in this work is relatively general and can be used to model networks combining resistors, probabilistic memristors, constant and time-dependent voltage and current sources. The application of the master equation to probabilistic memristor networks is a paradigm change in the probabilistic memristor modeling, and its SPICE implementation makes it affordable to students and researchers working in the field.

[1] A generalized approach is needed for circuits combining probabilistic memristors and capacitors/inductors.

2. Probabilistic Memristors and Master Equation

2.1 Binary Memristors

Binary memristors are described by two states, 0 (off) and 1 (on). These states correspond to the resistance states R_{off} and R_{on} with $R_{\text{on}} < R_{\text{off}}$. The switching between these states is defined by a probabilistic law with voltage-dependent switching rates (inverses of the mean switching times) given by [18–20]:

$$\gamma_{0\to1}(V) = \begin{cases} \left(\tau_{01}\mathrm{e}^{-V/V_{01}}\right)^{-1}, & V > 0 \\ 0 & \text{otherwise} \end{cases}, \tag{1}$$

$$\gamma_{1\to0}(V) = \begin{cases} \left(\tau_{10}\mathrm{e}^{-|V|/V_{10}}\right)^{-1}, & V < 0 \\ 0 & \text{otherwise} \end{cases}. \tag{2}$$

Here, $\tau_{01(10)}$ and $V_{01(10)}$ are constants and V is the voltage across the device. The probability of switching for a memristor initially in state 0 to state 1 within small time interval Δt is $\gamma_{0\to1}(V)\Delta t$. Similarly, the probability of switching for a memristor initially in state 1 to state 0 within small time interval Δt is $\gamma_{1\to0}(V)\Delta t$. The master equation is written with regard to the occupation probabilities of network states. The network state is defined by a specific combination of the off- and on-states of memristors. For a system containing N binary memristors, there exists 2^N such states. The network evolution consists of a chain of consecutive switchings of memristors (simultaneous switchings can be neglected). On average, such a process is described by the master equation with form:

$$\frac{\mathrm{d}p_\Theta(t)}{\mathrm{d}t} = \sum_{m=1}^{N}\left(\gamma^m_{\Theta_\mathrm{m}}p_{\Theta_\mathrm{m}}(t) - \gamma^m_\Theta p_\Theta(t)\right) \tag{3}$$

where $p_\Theta(t)$ is the occupation probability of state Θ, Θ_m is the network state obtained from Θ by flipping the state of m-th memristor, γ^m_Θ is the switching rate for m-th memristor in the configuration Θ, and $\gamma^m_{\Theta_\mathrm{m}}$ is defined similarly. The switching rate γ^m_Θ equals the one ((1) or (2)) for m-th memristor in the state Θ. To demonstrate (3), consider two in-series connected identical memristors subjected to a voltage waveform $V_\mathrm{a}(t)$. There are 4 possible network states that we denote as 00, 01, 10, and 11. In 00, both memristors are in the off-state, in 01, the first is in the off-, while the second is in the on-state, etc. Equation (3) has the form:

$$\frac{\mathrm{d}p_{00}(t)}{\mathrm{d}t} = \gamma^1_{01}p_{01} + \gamma^2_{10}p_{10} - 2\gamma^1_{00}p_{00}, \tag{4}$$

$$\frac{\mathrm{d}p_{01}(t)}{\mathrm{d}t} = \gamma^1_{00}p_{00} + \gamma^2_{11}p_{11} - \gamma^2_{01}p_{01} - \gamma^1_{01}p_{01}, \tag{5}$$

$$\frac{\mathrm{d}p_{10}(t)}{\mathrm{d}t} = \gamma^2_{00}p_{00} + \gamma^1_{11}p_{11} - \gamma^1_{10}p_{10} - \gamma^2_{10}p_{10}, \tag{6}$$

$$\frac{\mathrm{d}p_{11}(t)}{\mathrm{d}t} = \gamma^2_{01}p_{01} + \gamma^1_{10}p_{10} - 2\gamma^2_{11}p_{11}. \tag{7}$$

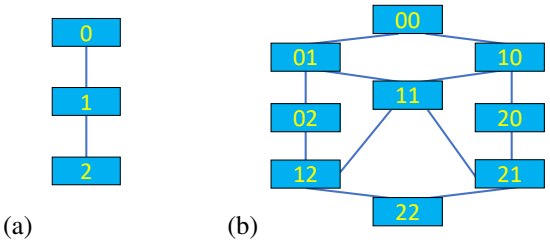

Fig. 1. Transition scheme for (a) single three-state memristor, and (b) network of two three-state memristors.

The similarity of memristors is taken into account by relations like $\gamma^1_{00} = \gamma^2_{00}$, $\gamma^2_{01} = \gamma^1_{10}$, $p_{01}(t) = p_{10}(t)$, etc. Therefore, Eqs. (5) and (6) are the same and the total number of equations that need to be solved reduces by one. In our notation, γ^1_{00} describes the switching rate from state 00 with the flipping of the 1-st memristor. The corresponding switching rate is given by Eq. (1) with $V = V_\mathrm{a}(t)/2$, etc. Importantly, the computation of the switching rate involves the voltage across the switching memristor in the given configuration at the time moment t.

2.2 Multi-State Memristors

It is assumed that in a K-state memristor the switching between its boundary states (R_{on} and R_{off}) occurs consecutively through $K-2$ intermediate resistance states. The master (3) preserves its form for multi-state memristor networks, but the network configuration space becomes more complex. Now the indices i, j, k, and so on, in the set $\Theta = (\ldots kji)$ denoting the states of the first memristor, the second one, and so on, in the network can have more than two values. Generally, this leads to the exponential growth of the number of network states and, correspondingly, the number of independent equations for occupation probabilities $p_\Theta(t)$ when N, the number of memristors, increases. Luckily, the number of nonzero switching rates γ, corresponding to the nonzero terms in the right hand side of the master equation (3) for a given network configuration Θ, does not typically grow as fast.

In order to account for potential change in parameter values between resistance states, equations (1) and (2) are modified to:

$$\gamma_{i\to j}(V) = \begin{cases} \left(\tau_{\mathrm{ij}}\mathrm{e}^{-V/V_{\mathrm{ij}}}\right)^{-1}, & V > 0, j = i+1 \\ 0 & \text{otherwise} \end{cases}, \tag{8}$$

$$\gamma_{j\to i}(V) = \begin{cases} \left(\tau_{\mathrm{ji}}\mathrm{e}^{-|V|/V_{\mathrm{ji}}}\right)^{-1}, & V < 0, j = i+1 \\ 0 & \text{otherwise} \end{cases}, \tag{9}$$

with $\tau_{\mathrm{ij(ji)}}$ and $V_{\mathrm{ij(ji)}}$ being the constant values describing the resistance switching from $i(j)$-th to $j(i)$-th memristor state, and i changes from 0 to $K-1$.

It is convenient to represent the interdependencies between different occupation probabilities in the master equation using transition schemes. As an example, Figure 1 shows the transition schemes for a single three-state memristor (a)

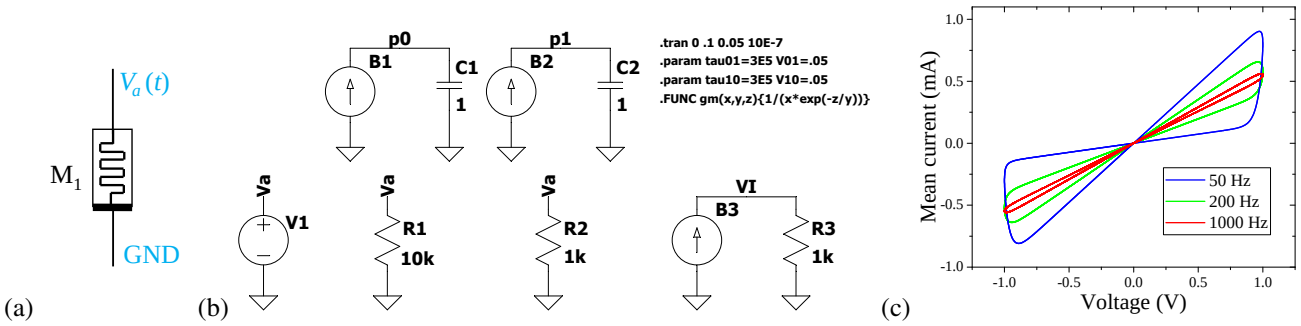

Fig. 2. Ac-driven probabilistic binary memristor: (a) simulated circuit, (b) schematics of SPICE model, and (c) example of current-voltage curves found with SPICE simulations. The listing of SPICE model is given in Tab. A.1.

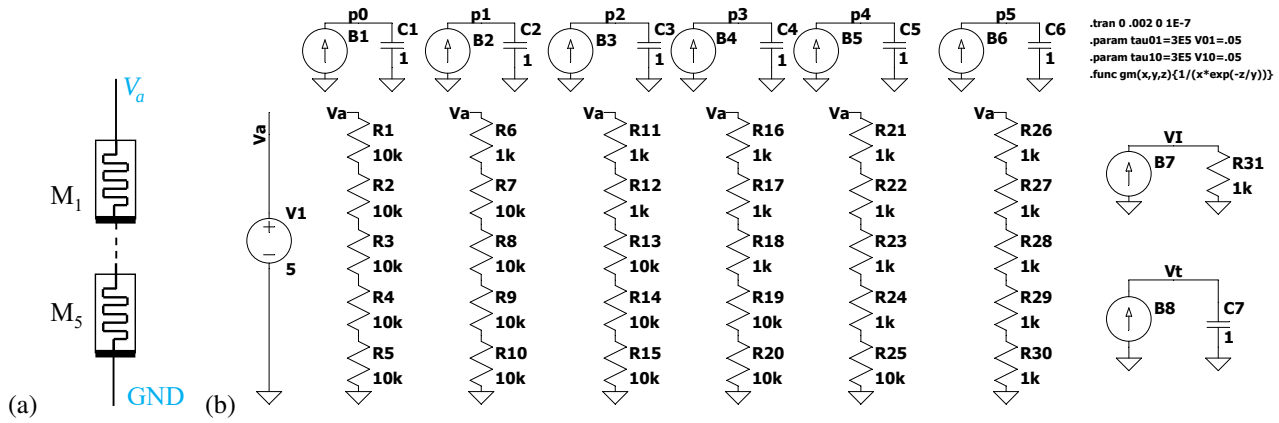

Fig. 3. Dc-driven network of five probabilistic binary memristors: (a) simulated circuit, (b) schematics of SPICE model.

and two such memristors connected into network. An important feature of these schemes is the sequential change in the state of multi-state memristors that approximates the sequential growth of filaments in physical devices. Additionally, we emphasize that the transition schemes in general do not depend on the specific connections of memristors in the network. The transition rates contain those details. In practice some of the transitions may be almost or entirely forbidden. For instance, when a positive voltage is applied to memristor described by equation (1) and (2), the transition $1 \rightarrow 0$ is forbidden as it occurs at negative voltages. If one neglects low rate and/or forbidder transitions, we obtain the reduced transition scheme, which simplifies the solution of the master equation (3) (see [24] for some examples).

3. SPICE Modeling Approach

Let M be the number of non-equivalent equations for the occupation probabilities (like the set of Eqs. (4), (5), and (7)) for a network of N memristors with K memristor states. The supremum of M is K^N. However, in practical cases M can be much smaller than K^N. For example, an in-series network of N identical binary ($K = 2$) memristors has $M = K+1$ (see [24]).

In the SPICE environment, we model each differential equation (such as (4)) by a 1 Farad capacitor charged by a voltage-controlled current source. The occupation probabilities are represented by capacitor voltages. Each source current depends on the voltage across some of the capacitors which forms the right-hand side of the master equation. These circuits are shown in the top rows of SPICE models in Figs. 2, 3, 5 and 6. The voltage-dependent switching rates (Equation. (1), (2)) are accounted for by including M copies of the network with memristors in non-equivalent combinations of states. These circuits (shown in the bottom row in Figs. 2, 3, 5 and 6) are connected to the input voltage. The voltages across memristors in these circuits are utilized to calculate the transition rates between the states. To calculate the mean current, we use a voltage-controlled current source connected by a resistor to ground to provide a current path. For instance, in the case of in-series connected binary memristors, the current source output is defined by:

$$\langle I \rangle (t) \equiv \sum_{m=0}^{N} \binom{N}{m} I_{\mathrm{m}}(t) p_{\mathrm{m}}(t) \tag{10}$$

where the number of states with the same number of memristors in the on-state is taken into account by the binomial coefficients $\binom{N}{m}$, and $I_{\mathrm{m}}(t)$ is the current through the network with m memristors in the on-state. The switching time (or any other integral) can be evaluated numerically with a capacitor-voltage-controlled current source. Examples of such calculations can be found below.

4. Simulation Examples

4.1 AC-Driven Binary Memristor

In this simulation, a single binary memristor driven by an ac source is considered as seen in Fig. 2(a). Fig. 2(b) contains the schematic for the SPICE implementation and the corresponding SPICE code can be found in appendix A.1. The memristor has two possible states, R_{on} and R_{off}, with resistance values of 1k and 10k Ohms respectively. We used the model parameter values $\tau_{01} = \tau_{10} = 3 \cdot 10^5$ s and $V_{01} = V_{10} = 0.05$ V. The ac source, $V_{\text{a}}(t)$, has a peak voltage of 1 V and is driven at various frequencies. The memristor is initialized in the off-state and will continue switching between the resistance states until the simulation has ended. The current is calculated using B4 and R4 components in Fig. 2(b). The current-voltage curves generated through SPICE simulation can be seen in Fig. 2(c) and they show the frequency behavior typical to deterministic memristive devices [16, 17]. We verified that Fig. 2(b) SPICE model reproduces some previous results found through Monte Carlo simulations [24].

4.2 DC-Driven Binary Memristor Network

For this next simulation, we consider a network of binary memristors connected in-series as shown in Fig. 3(a). The network is composed of five memristors driven by a dc source with a voltage of 5 V. Figure 3(b) contains the schematic for the SPICE implementation. Each memristor is identical to one another, meaning the model parameters and the two states are equivalent from memristor to memristor. The memristors have two possible states, R_{on} and R_{off}, with resistance values of 1 k and 10 k Ohms respectively. We used the model parameter values $\tau_{01} = \tau_{10} = 3 \cdot 10^5$ s and $V_{01} = V_{10} = 0.05$ V. Each memristor starts in the off-state and as time progresses each will switch to the on-state. When a memristor switches to the on-state, the drop in resistance causes an increase in the voltage across the off-state memristors increasing the probability of switching for the off-state memristor.

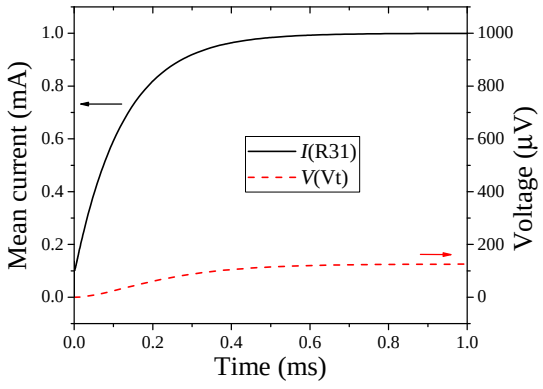

Fig. 4. Current as a function of time (black solid line), and calculation of the network switching time (red dashed line) in the dc-driven network of five probabilistic binary memristors.

According to the analytical theory [24], the network mean switching time can be calculated as

$$\langle T_{\text{N}} \rangle = \sum_{j=0}^{N-1} \frac{1}{(N-j)\gamma_{\text{j}}}. \tag{11}$$

For the parameters of simulations in Figs. 3 and 4, the above equation gives $\langle T_5 \rangle = 126$ μs. Numerically, the same quantity can be evaluated using the following integral

$$\int_0^\infty t 5 \gamma_{01111}^5 p_{01111}(t) \text{dt}. \tag{12}$$

Technically, the integration is done by the components B8 and C7 in Fig. 3, so that the averaged switching time corresponds to the saturation limit of $V(\text{Vt})$ curve in Fig. 4. We emphasize that the analytical and numerical (SPICE) values for $\langle T_5 \rangle$ are in full agreement.

4.3 Multi-State Memristors

The first multi-state simulation considered is a single tri-state memristor driven by an ac source. The ac source has a peak voltage of 1.5 V and is driven at various frequencies. Fig. 5(a) contains the schematic for the SPICE implementation and the corresponding SPICE code can be found in appendix A.2. The memristor now has three possible states, off-, intermediate, and on-state. To account for the added resistance state, a new copy of the memristor network is necessarily added to the SPICE implementation. These states have resistance values of 10 k, 3 k, and 1 k Ohm respectively. The model parameters, τ_{ij} and V_{ij}, are as specified in the SPICE model schematics (Fig 5(a)). The memristor is initialized in the off-state and will continue switching between the resistance states until the simulation has ended. Fig. 5(b) shows the current-voltage curves generated by this SPICE simulation. This next simulation is a network of two tri-state identical memristors driven by a 1.5 V dc source shown in Fig. 6(a). The resistance states and model parameters are identical to the memristor used in the previous configuration. Fig. 6(b), the SPICE schematic used for this simulation is shown. The SPICE model is designed according to the transition scheme in Fig. 1(b). The memristors are initialized in the off-state and will switch to the intermediate state before switching to the on-state during the simulation.

The evolution of resistance state probabilities for this network is shown in Fig. 6(c) and the mean current as a function of time for this SPICE simulation is shown in Fig. 6(d). The mean current increases in two steps because of the different time scales for the $0 \rightarrow 1$ and $1 \rightarrow 2$ memristor switchings.

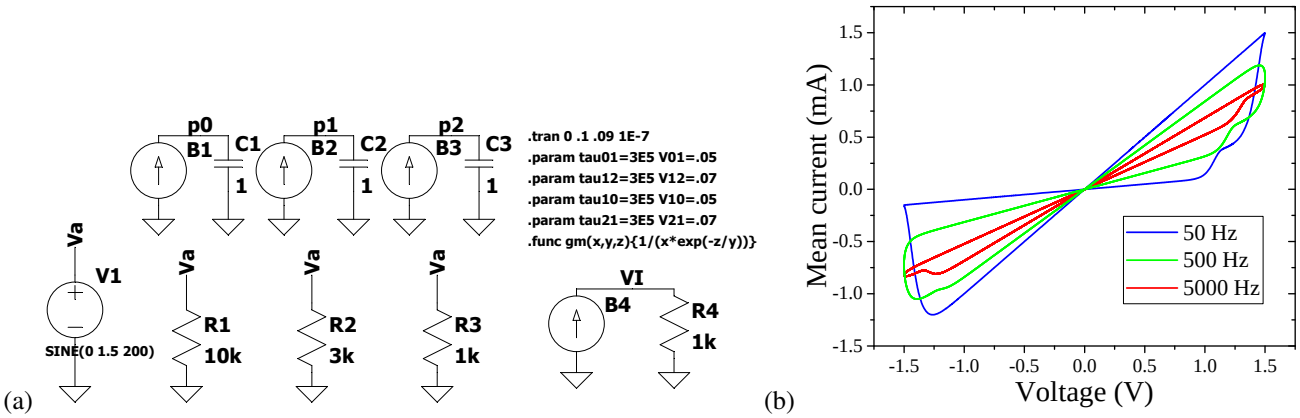

Fig. 5. Ac-driven probabilistic three-state memristor: (a) schematics of SPICE model, and (c) example of current-voltage curves found with SPICE simulations. The listing of SPICE model is given in Tab. A.2. The simulated circuit is the same as in Fig. 2(a) with the difference of different memristor type used.

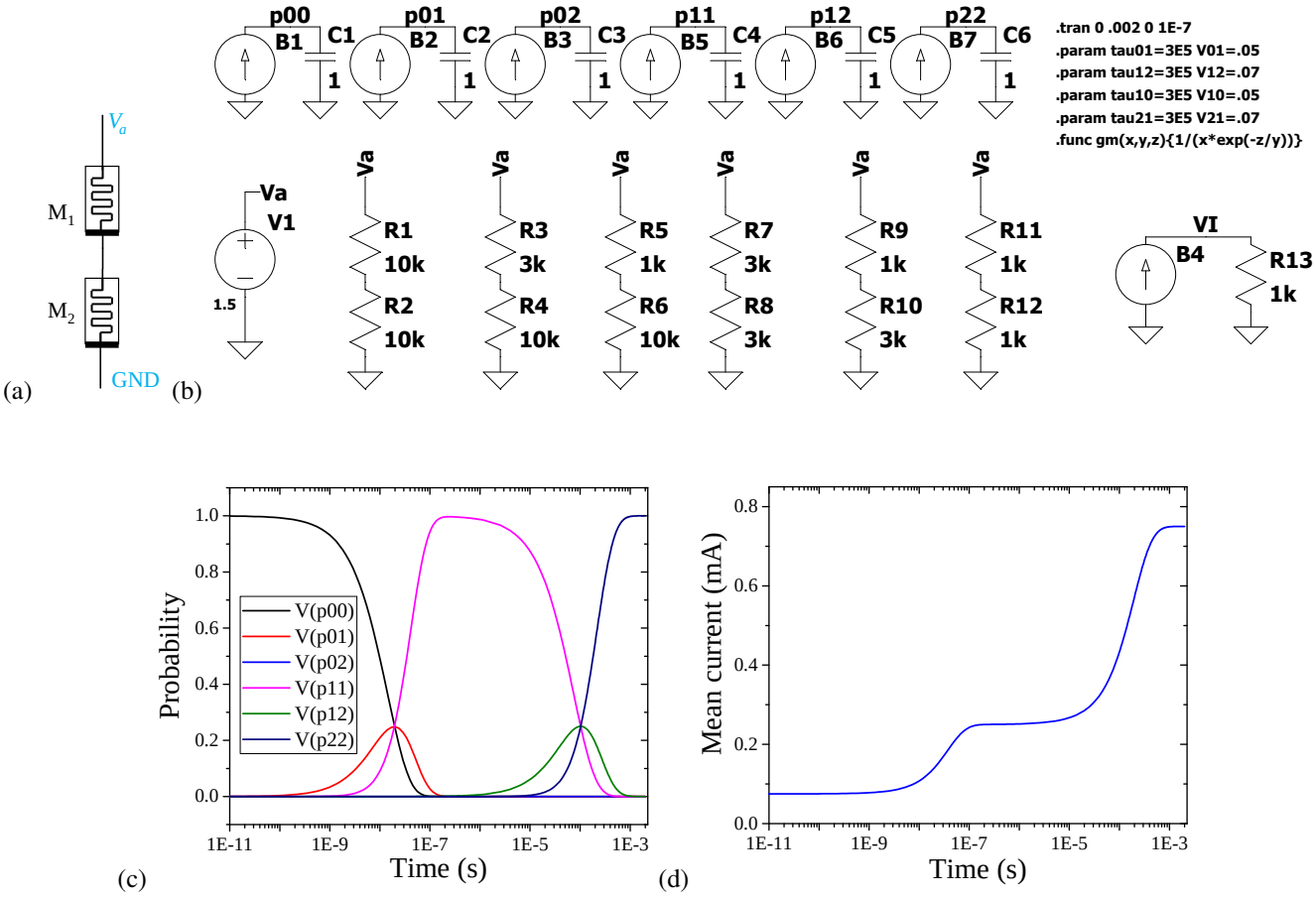

Fig. 6. Dc-driven network of two three-state memristors: (a) simulated circuit, (b) schematics of SPICE model, (c) time-evolution of occupation probabilities, and (d) current as a function of time.

5. Summary

In summary, the use of the master equation in probabilistic circuit modeling [24] offers significant benefits compared to the routine Monte Carlo/stochastic simulations. Many circuit characteristics can be found on average in a single run and the master equation can be, in principle, solved analytically, with several analytical solutions already known [24]. In this work, we have shown how to implement the master equation in SPICE. Our examples include simulations of binary and multi-state probabilistic memristors and their circuits subjected to ac- and dc-voltages. We expect that our approach will be useful to a broad range of researchers working in the area of emerging memory devices.

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Appendix A: SPICE Code Examples

```
B1 0 p0 I=-gm(tau01,V01,V(Va))*V(p0)*u(V(Va))+gm(tau10,V10,-V(Va))*V(p1)*u(-V(Va))
B2 0 p1 I=gm(tau01,V01,V(Va))*V(p0)**u(V(Va))-gm(tau10,V10,-V(Va))*V(p1)**u(-V(Va))
C1 p0 0 1 IC=1
C2 p1 0 1 IC=.0
R2 Va 0 1k
R1 Va 0 10k
R3 VI 0 1k
B3 0 VI I=I(R1)*V(p0)+I(R2)*V(p1)
V1 Va 0 SINE(0 1 200 0 0 0 0)
.FUNC gm(x,y,z)1/(x*exp(-z/y))
.param tau01=3E5 V01=.05
.param tau10=3E5 V10=.05
.tran 0 .1 0.05 10E-7
.backanno
.end
```

Table A.1. SPICE code for ac-driven probabilistic binary memristor.

```
B1 0 p0 I=(-gm(tau01,V01,V(Va))*V(p0))*u(V(Va))+(gm(tau10,V10,-V(Va))*V(p1))*u(-V(Va))
B2 0 p1 I=(gm(tau01,V01,V(Va))*V(p0)-gm(tau12,V12,V(Va))*V(p1))*u(V(Va))+(gm(tau21,V21,-V(Va))*V(p2)-gm(tau10,V10,-
+V(Va))*V(p1))*u(-V(Va))
B3 0 p2 I=(gm(tau12,V12,V(Va))*V(p1))*u(V(Va))+(-gm(tau21,V21,-V(Va))*V(p2))*u(-V(Va))
R1 Va 0 10k
R2 Va 0 3k
R3 Va 0 1k
R4 VI 0 1k
C1 p0 0 1 IC=1
C2 p1 0 1 IC=0
C3 p2 0 1 IC=0
B4 0 VI I=I(R1)*V(p0)+I(R2)*V(p1)+I(R3)*V(p2)
V1 Va 0 SINE(0 1.5 200)
.func gm(x,y,z)1/(x*exp(-z/y))
.param tau01=3E5 V01=.05
.param tau12=3E5 V12=.07
.param tau10=3E5 V10=.05
.param tau21=3E5 V21=.07
.tran 0 .1 .09 1E-7
.backanno
.end
```

Table A.2. SPICE code for ac-driven probabilistic three-state memristor.