

Emulation of Three-Pinch-Off Memristor Emulator Based on Highly Non-Linear Charge-Flux Characteristics

Kapil BHARDWAJ, Mayank SRIVASTAVA

Dept. of Electronics and Communication Engineering, NIT Jamshedpur, Jharkhand, India

mayank.ece@nitjsr.ac.in

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Abstract. *The presented work describes an exclusive mathematical model for the multi-pinch-off behavior generated by non-linear memristors, which may be useful in advanced memristive applications. The reported mathematical results are based on the calculation of inflection points present on the memristor charge-flux curve, which has not been studied so far. The consideration of inflection points can be very useful in deciding various aspects of non-linear memristive applications. Based on derived mathematical conditions; a VDTA active element based, three-pinch-off memristor emulator has been developed, without employing any multiplier IC. For the first time, such a compact emulator circuit has been proposed, which uses only two VDTAs and three grounded passive elements, to emulate multi-pinch-off behavior at moderate frequencies. The behavior of the presented emulator is studied by performing simulations under the PSPICE environment for CMOS VDTA. The presented VDTA based three-pinch-off memristor is also implemented using commercially available IC LM13700 and verified.*

Keywords

Three-pinch-off memristor, LM13700, memristor, VDTA

1. Introduction

In 1971, Leon Chua postulated an electrical element with the virtue of having hysteresis in the Current-Voltage ($v-i$) characteristics for transient variations [1]. It finds its applications in various ranges of fields including RRAM (Resistive Random Access Memory) and CNN (Cellular Neural Networks).

The circuits suggested in [2–11] emulate the behavior of a conventional memristor which produces dual lobe $v-i$ characteristics with a single pinch-off point at the origin. In the work depicted in [2], a MOS based realization of a floating memristor is presented. And STDP (Spike Timing-Dependent Plasticity) behavior using the realized memristor has been demonstrated. Similarly, a single OTA based floating memristor emulator has been proposed in

[3]. The developed circuit employs two external MOS transistors, a grounded capacitance, and also requires an analog multiplier IC. Furthermore, the floating memristor emulator given in [4] has been realized using a single CBTA and two grounded capacitors. From the simulation results, it can be observed that the behavior of the emulated memristor is not found to be electronically adjustable. In [5], an emulation configuration of grounded memristor has been reported which uses single CCTA, three resistors, and single grounded capacitance. The floating memristor configuration depicted in [6] employs a large number of active and passive elements including seven active building blocks (3 CCIs and 4 OTAs) and more than five grounded resistances. Moreover, the floating memristor realization circuit reported in [7] is based on a single VDTA and three grounded passive elements along with a MOS based analog multiplier. Moreover, a single multi-output OTA based on grounded memristor is discussed in [8]. It uses two grounded passive elements and an external analog multiplier IC. In [9], both grounded and floating circuit configurations to realize universal mem-element emulators have been discussed. The presented circuits are based on large numbers of active and passive elements along with an external analog multiplier IC. Similarly, the commercial ICs based configuration reported in [10], requires two AD844s and two AD633 ICs to realize a floating memristor emulator. Also, it employs a large number of floating and grounded passive elements. Furthermore, the work shown in [11] depicts the active devices based realization of physical memristor (HP memristor). It employs a large number of operational amplifiers and external MOS transistors along with an external analog multiplier.

Now, in any initial/operating conditions, these conventional memristors [2–11] always produce two lobes with a single pinch-off at the origin, when subjected to pure sinusoidal signals. It is because the memristance/memductance functions, these emulators realize, depends linearly upon the transferred flux value. On the other end, the higher extent of non-linearity in charge-flux characteristics can be very useful in applications such as multi-bit memories, chaotic oscillators, and multi-level logic design. And, interestingly the occurrence of multiple pinch-off points on the $v-i$ contour guarantees the highly non-linear

nature of a memristor subjected to a sinusoidal input. But, surprisingly, in case of any discrepancy in the conventional memristor function or due to the presence of undesired harmonics in the applied sinusoidal signal, conventional memristors may accidentally exhibit multiple pinch-off points on the v - i contour. Like, it can be observed in [12], that the presented physical architecture based on HfOx exhibits extra non-zero pinch-off points in some operating conditions, but in the reported work, this unexpected behavior has not been investigated. And, in [13], the mathematical conditions on the different amplitudes of the multiple harmonics have been derived, which can cause the generation of symmetrical multiple pinch-off points, on the v - i characteristics. The experimental verification of this phenomena is also shown in [14] through the excitation of a commercial memristor IC by multi-harmonic signals. But, the application of multi-harmonic signals does not affect the static characteristics of the conventional memristor and therefore brings no new advantage to any memristive applications. It can be easily understood that multi pinch-off behavior from the pure sinusoidal excitation and under controlled conditions, can only be achieved if the constitutive relationship of the memristor is modified itself. Remarkably, some works can be found in the literature, which has considered unconventional memristor models to find multiple pinch-off v - i contours [15–18]. Like the graphical analysis presented in [15] clearly depicts that some specific charge-flux (q - ϕ) curves can produce symmetrical multiple lobes on the v - i plane for bipolar signals. This analysis describes the effect of different initial operating conditions on the v - i characteristics for piece-wisely linear q - ϕ curves without any mathematical description. Although the analyzed memristor functions cannot be considered for realization purposes, the presented multi-slope q - ϕ curves clearly demonstrate the ability of multi-pinch off memristors to exhibit multi-resistance switching levels.

Moreover, some circuit emulators of fractional-order memristor have been reported recently [16–18] realizing the memductance expression having multiple fractional powered flux terms in it. Interestingly, these emulator circuits produce two/three pinch-off points on the v - i contour, but at the non-symmetric locations. These emulator circuits are based on the derived mathematical models for two/three pinch-off v - i behavior in fractional order memristors. But, in the given mathematical framework, the effect of the curvature of corresponding q - ϕ characteristics and initial conditions has not been provided. Furthermore, the two/three pinch-off behavior generated through these emulator circuits suffers from severe limitations discussed below. The emulator circuits reported in [16–18] produce three-lobe v - i characteristics but with quite different features in opposite quadrants. Due to this non-symmetrical memductance behavior, these memristors are not suitable for bipolar applications. Also, acceptable three-lobe behavior is only possible in the few kilo-Hertz range of operating frequency. This limitation of the operability of these reported fractional-order memristors to low operating frequencies indicates the lack of non-linearity in charge-flux

characteristics, which is highly required in previously discussed applications. Hence, there is no theoretical framework and realization available in the literature for achieving multi-pinch off hysteresis behavior from an integer order memristor subjected to pure sinusoidal signals. Therefore, the objectives of this paper are, to present the systematic mathematical model and a compact emulator circuit for a memristor, whose transient v - i characteristics find three pinch-off points on the symmetrical v - i contour at a sufficiently high range of frequencies (hundreds of kHz) of pure sinusoidal signals.

2. Mathematical Description of Three-Pinch-Off Behavior

Before exploring the three-pinch-off behavior mathematically, it is useful to understand the fundamental cause behind the inability of conventional memristors to produce multiple lobe behavior in standard operating conditions. It has been explained through the discussion presented below. The constitutive relationship of the memristor is defined between the charge (q) and flux (ϕ) associated with the memristor as following;

$$f(q, \phi) = 0 \tag{1}$$

and the memductance of a voltage-controlled memristor can be found from (2) as

$$G_M = dq / d\phi. \tag{2}$$

For conventional memristors, this memductance is related to the flux in a linear relationship given in (3)

$$G_M = a_0 + a_1\phi \tag{3}$$

where the flux ϕ , for the input sinusoidal signal, $v(t) = V_m \sin(\omega t)$ can be written as;

$$\phi = \int_0^t V_m \sin(\omega t) dt = \frac{V_m}{\omega} (1 - \cos(\omega t)). \tag{4}$$

As it is clear from the above equation, the memductance $G_M(t)$ of a conventional memristor varies linearly with applied flux ϕ in a single direction. And this change is reflected as a single loop in the v - i plane (as shown in Fig. 1) with no non-zero intersection. Due to this monotonic variation, conventional memristors are not much

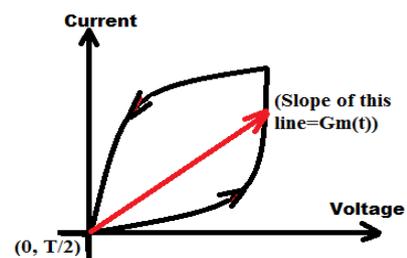


Fig. 1. Dual lobe behavior of a conventional memristor in first quadrant description.

useful in applications like storage, resistance-switching, chaotic oscillators, etc.

Impact of symmetrical cross-over points: Next, we consider a graphical example of three-pinch-off $v-i$ contour and try to understand the nature of the corresponding $q-\phi$ relationship by applying reverse engineering. If we carefully observe the $v-i$ curve given in Fig. 2(a), we will found that the main impact of non-zero cross-over C1 is found as that it changes the direction of memductance variation once (as depicted through arrow-heads), during the period $(0-T/2)$. By using basic concepts, the curve on the $v-i$ plane can be mapped on the $q-\phi$ plane as presented in Fig. 2(b). From the plotted $q-\phi$ curve, it can be observed that it has two inflection points at ϕ_1 and ϕ_2 located at the points of curvature change (with ϕ_0 representing the initial flux value). Due to this type of multi-curvature feature, these memristors are the potential candidates for resistance switching, multi-bit memories, and chaotic oscillators.

Furthermore, in Fig. 2(b), at inflection points, I1 and I2, the following mathematical condition must hold,

$$\frac{d^2q}{d\phi^2} = 0. \tag{5}$$

Now, as equation (5) must be a second-order equation, it implies that memductance of a three-pinch-off memristor must be of the following type

$$G_{M3} = a_0 + a_1\phi + a_2\phi^2 + a_3\phi^3 \tag{6}$$

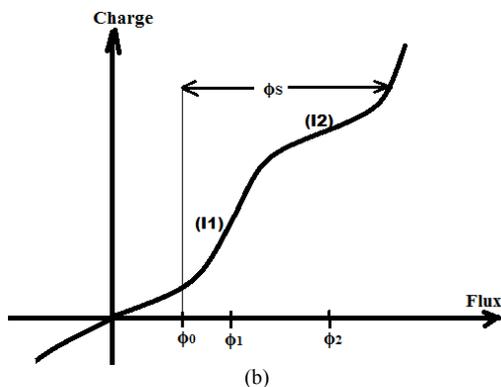
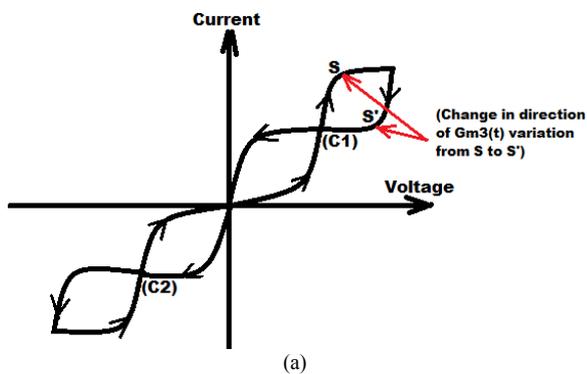


Fig. 2. Characteristics of a three-pinch of behavior: (a) Typical transient $v-i$ contour having symmetrical cross-over points C1 and C2. (b) Static $q-\phi$ characteristics having two inflection points I1 and I2.

where $a_0, a_1, a_2,$ and a_3 are memristor coefficients. By using (6)

$$\frac{d^2q}{d\phi^2} = \frac{dG_{M3}}{d\phi} = a_1 + 2a_2\phi + 3a_3\phi^2. \tag{7}$$

Therefore, equation (5) must be

$$3a_3\phi^2 + 2a_2\phi + a_1 = 0. \tag{8}$$

Now, in order to obtain real and different valued inflection points, the condition can be given as

$$4a_2^2 - 12a_1a_3 > 0. \tag{9}$$

From (8), the flux values ϕ_1 and ϕ_2 at which the inflection occurs (as depicted in Fig. 2(b)) can be calculated as follows

$$\phi_1, \phi_2 = \frac{-2a_2 \pm \sqrt{4a_2^2 - 12a_1a_3}}{6a_3}. \tag{10}$$

Furthermore, for exhibiting three pinch-off points, applied flux, ϕ_s must cover both inflection points (Fig. 2b), for which, the following condition must be satisfied

$$\phi_s > \phi_2 - \phi_0 \tag{11}$$

where the supplied ϕ_s , during the half-cycle period, can be calculated as

$$\phi_s = \frac{2V_m}{\omega}. \tag{12}$$

Now, it must be emphasized that, the conditions given in (9) and (11) only decide the operating region, which consists two inflection points, on the $q-\phi$ curve. But it is important to tell that the presence of two inflection points in the operating region does not always guarantee the occurrence of three pinch-off points on the $v-i$ plane (although converse is always true).

We know, that a crossing on the $v-i$ contour is always occurred when the $v-i$ curve traverses the same point on the $v-i$ plane at two different symmetrical time instants in a half cycle of the applied excitation voltage. For the intersection of the $v-i$ contour, at these two symmetrical time instants, t_{c11} and t_{c12} memristor should exhibit same memductance. For which, these two time instants must be related such that $\omega t_{c12} = (\pi - \omega t_{c11})$, therefore,

$$G_{M3}(\omega t_{c12}) = G_{M3}(\pi - \omega t_{c11}). \tag{13}$$

By using (4), equation (6) can also be written as

$$G_{M3}(\phi) = a_0 + a_1 \left(\frac{V_m}{\omega} (1 - \cos \omega t) \right) + a_2 \left(\frac{V_m}{\omega} (1 - \cos \omega t) \right)^2 + a_3 \left(\frac{V_m}{\omega} (1 - \cos \omega t) \right)^3. \tag{14}$$

On applying condition given in (13), time instant t_{c12} , from (14) can be calculated as

$$t_{c12} = \frac{1}{\omega} \left[\pi - \sin^{-1} \sqrt{\frac{\omega^3}{V_m^3 a_3} \left(a_1 \frac{V_m}{\omega} + 2a_2 \frac{V_m^2}{\omega^2} + 4a_3 \frac{V_m^3}{\omega^3} \right)} \right] \quad (15)$$

and also, the critical value of the $\sin(\omega t)$ at which the pinch-off occurs can be given as

$$v_c(t) = \sin(\omega t_{c12}) = \sqrt{\frac{\omega^3}{V_m^3 a_3} \left(a_1 \frac{V_m}{\omega} + 2a_2 \frac{V_m^2}{\omega^2} + 4a_3 \frac{V_m^3}{\omega^3} \right)}. \quad (16)$$

It can be understood that for the crossover point to occur, t_{c11} should follow the criteria: $0 < t_{c11} < T/4$.

By using (15), we can write,

$$\frac{1}{\omega} \left[\sin^{-1} \sqrt{\frac{\omega^3}{V_m^3 a_3} \left(a_1 \frac{V_m}{\omega} + 2a_2 \frac{V_m^2}{\omega^2} + 4a_3 \frac{V_m^3}{\omega^3} \right)} \right] < T/4. \quad (17)$$

Hence, it can be stated that the coefficient values, peak i/p value, and operating frequency decide the occurrence of symmetrical crossover points. For suitable values of coefficients and operating parameters (satisfying (9), (11), and (17)), the three pinch-off $v-i$ contour can be obtained through the third-order memductance given in (6), which has been plotted in Fig. 3.

Further, it must be emphasized that the investigation of charge-flux characteristics using a mathematical approach is a unique and useful method, which has been followed in the above analysis. It offers the advantage of easier generalization to multiple pinch-off points, which can be directly utilized in these memristor-based multi-level switching applications. Now, coming to the possible application of multi-pinch-off memristors, we know that the most important feature of a memristor is its memory property due to which it can store data [19]. In [20] it has been proved mathematically that the area covered under the transient $v-i$ lobe of a memristor decides the storage property of the memristor. And, for a multiple lobe memristor it can be clearly understood that it will exhibit multiple lobes (more than two) and resultantly, more memory content will be stored due to its different lobe-area components. It can also be explained through Fig. 2, which depicts that three

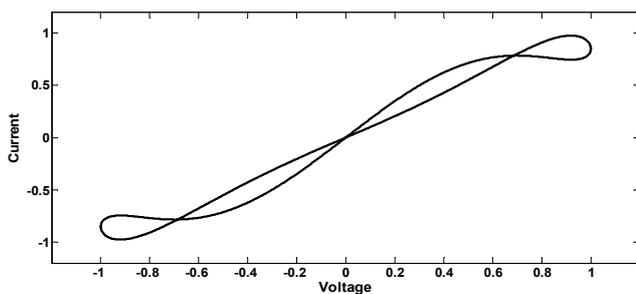


Fig. 3. Transient VI characteristics exhibiting three pinch-off points generated for the angular frequency $\omega = 1$.

pinch-off points on the $v-i$ contour, is the indication of at least two inflection points residing on the static characteristics. Now, these inflection points may be considered as the threshold points splitting the curvature into three levels of conductance values. On the other hand, due to the unavailability of any inflection point, multiple ranges of resistances/conductances are not found in single pinch-off memristors. Hence, the existence of multiple lobes in PHL opens the possibilities for multi-bit memory implementation. The multiple lobe memristors can also find applications in chaotic oscillator implementation. And interestingly, the discussion, given in [21] clearly illustrates the use of specifically three-pinch-off behavior for chaotic applications.

3. Voltage Differencing Transconductance Amplifier (VDTA)

In 2008, the theory of VDTA active element was proposed by Bielek et al. [22] whose CMOS implementation is shown in Fig. 4. It is a circuit idea of five high impedance terminals whose current-voltage relationship is given in (18). The V_{B1} and V_{B2} are the biasing terminals to provide the facility of electronic tuning through voltage.

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (18)$$

where g_{m1} and g_{m2} are the transconductances of the input and output stage of VDTA respectively, which are related to V_{B1} and V_{B2} as

$$g_{m1,2} = k_{1,2}(V_{B1,2} - V_{SS} - V_{th}). \quad (19)$$

VDTA has been used in several analog domain applications such as inductance realization, modern oscillation configurations, and active filtering circuits [23–26].

4. Proposed Configuration of VDTA Based Three-Pinch-Off Memristor Emulator

The proposed VDTA based three-pinch off memristor emulator is shown in Fig. 5. This VDTA based circuit architecture realizes a third-order memductance function consisting of three consecutive high power flux terms (6). But still, the presented emulator is much more compact than those previously reported emulator circuits given in [2–11], which realize only the linear flux dependent functions (shown in (3)). It can be understood from the following comparison.

- The conventional memristor emulators described in [3, 4, 7, 8, 9, 10, 11] which have only a single multiplication term of voltage multiplication in the current

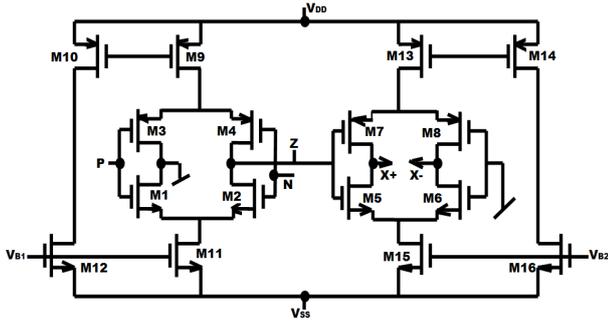


Fig. 4. VDTA implementation using CMOS.

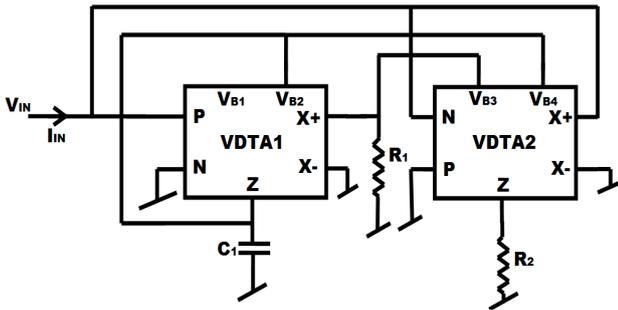


Fig. 5. Designed emulation configuration of three-pinch-off memristor using VDTA.

equation employ one or more voltage multipliers/ ICs. But the proposed three-pinch-off memristor, whose memductance consists of three different terms having voltage multiplication operation, does not employ any external voltage multiplier/IC. This feature can be considered as the most attractive feature of the proposed design.

- Although the emulators reported in [6, 9, 11] realize the linear memductance behavior but these circuits employ an excessive number (three or more) of active elements. On the other end, the proposed emulator shown in Fig. 5, employs only 2 VDTAs. Also, the total number of MOS transistors required to implement our circuit is thirty-two, which is lesser than so many single pinch-off memristors described in [2–11].
- From the perspective of the use of passive elements, the presented emulation circuit requires only two resistances and single capacitance while single pinch-off memristors reported in [6, 9, 10, 11] need more than three resistances. And the emulators reported in [2, 3, 4, 10] require two or more capacitances.
- All the passive elements used in the proposed emulator circuit are grounded, which confirms the suitability of the proposed circuit for monolithic integration. While the conventional memristor emulators reported in [5, 6, 10, 11] employ one or more floating passive elements.

Similarly, the fractional-order memristor emulators given in [16–18] are also based on bulky circuit configurations. These emulators require one or more analog multiplier IC and employ a large number of passive elements,

which are inevitable due to the use of fractional order capacitors. The integer order element realizations are always based on a lesser number of passive elements and are less dependent upon parameter variations.

Now using the terminal relationship of VDTA (given in (18)), input current I_{in} entering in the emulator circuit can be calculated as

$$I_{in} = k_3 k_4 \left(\frac{g_{m1} \phi_{in}}{C_1} + (-V_{SS} - V_{th}) \right) \left(k_2 R_1 \left(\frac{g_{m1} \phi_{in}}{C_1} \right)^2 + k_2 (-V_{SS} - V_{th}) \left(\frac{g_{m1} \phi_{in}}{C_1} \right) R_1 + (-V_{SS} - V_{th}) \right) V_{in} R_2. \quad (20)$$

Expanding (20), the memductance of the realized three-pinch off memristor can be found as

$$G_{M3} = \frac{I_{in}}{V_{in}} = k_2 k_3 k_4 R_1 R_2 \left[\frac{g_{m1} \phi_{in}}{C_1} \right]^3 + 2k_2 k_3 k_4 R_1 R_2 (-V_{SS} - V_{th}) \left[\frac{g_{m1} \phi_{in}}{C_1} \right]^2 + (k_3 k_4 R_2 (-V_{SS} - V_{th}) + k_2 k_4 k_3 R_1 R_2 (-V_{SS} - V_{th})^2) \left[\frac{g_{m1} \phi_{in}}{C_1} \right] + k_3 k_4 R_2 (-V_{SS} - V_{th})^2. \quad (21)$$

5. Simulation Results

The section presents the PSPICE generated simulation results obtained for the presented memristor emulator. For validating the developed memristor emulator, the CMOS based VDTA (shown in Fig. 4) is used with supply voltages as ± 0.9 V. Furthermore, the W/L ratio of CMOS transistors, M3-4, M7-M9, M13-M14 is taken as $13 \mu\text{m}/0.36 \mu\text{m}$ and for the transistors M1-M2, M5-M6, M11-M12, M15-M16, it is chosen as $4 \mu\text{m}/0.36 \mu\text{m}$.

First, we have investigated the effect of operating frequency on the three pinch-off behavior. For which, the passive element values are taken as $R_1 = 55 \text{ k}\Omega$, $R_2 = 5 \text{ k}\Omega$, and $C_1 = 0.5 \text{ nF}$, and biasing voltage is selected as $V_B = 0.05 \text{ V}$. As can be understood from mathematical discussion that three pinch-off v - i contour must exhibit an unusual frequency dependence behavior, which will be different from conventional behavior. In a three-pinch off memristor, on increasing the applied signal frequency middle lobes begin to contract and consequently, the area of external lobes starts to expand. The same phenomena can

be observed from the $v-i$ curves given in Fig. 6 plotted for the proposed VDTA based emulator. It is important to tell that variation in the frequency does not affect the constitutive relationship of memristor between charge and flux, but it does influence the supplied flux value responsible for operating region coverage. Now, on increasing the F_{in} value but without varying the input amplitude, changes the length of the operating region by reducing its upper limit (lower limit is decided by pre-stored values). Due to this, initial transient behavior is always observed as the same, as found in Fig. 6 through commonly touching parts of all three $v-i$ contours. Moreover, it can be easily visualized, that hysteresis is found in the $v-i$ characteristics, only when the transient voltage and current response are different from each other. The presented three-pinch-off memristor emulator validates this property and it also shows no phase difference between current and voltage. It can be verified from the plots presented in Fig. 7 and 8 for $F_{in} = 700$ kHz. In the given plots, zero phase difference can also be observed, which confirms the resistive nature of the realized memristor element.

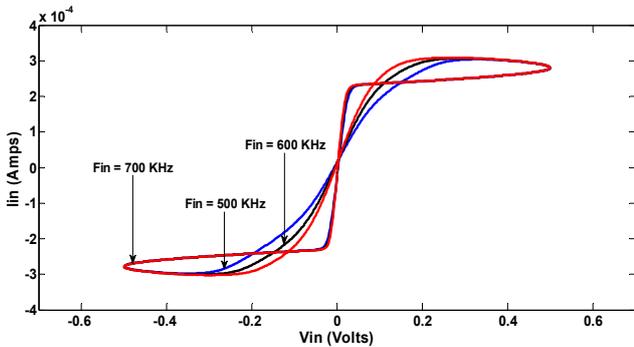


Fig. 6. Three pinch-off behavior generated by presented VDTA based emulator at different operating frequencies.

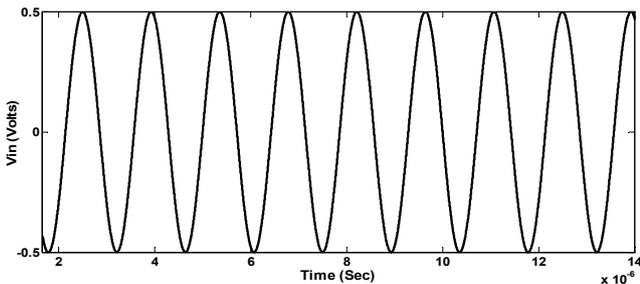


Fig. 7. Applied sinusoidal voltage for frequency $F_{in} = 700$ kHz.

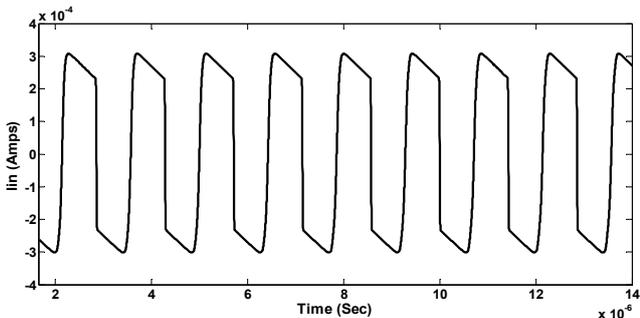


Fig. 8. Generated current response for input voltage shown in Fig. 7.

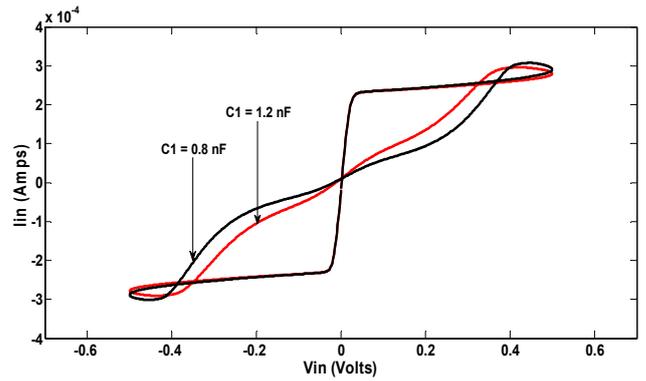


Fig. 9. The behavior of presented emulator circuit for different values of capacitance $C1$.

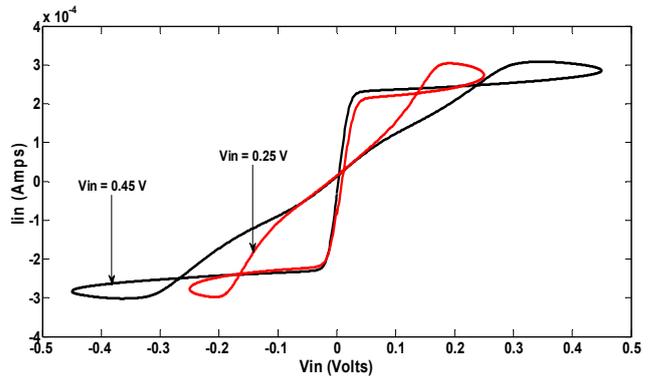


Fig. 10. Effect of different peak valued input voltages on the $v-i$ characteristics of the presented emulator.

For further analyzing the effect of different operating parameters, i/p signal frequency is chosen as 700 kHz, and biasing voltage V_B is kept fixed at 0.05 V. The plots described in Fig. 9 are taken for two different values of capacitance $C1$ keeping all other parameters constant, which verify that realized behavior can be easily controlled using the employed capacitor.

Similarly, as mentioned earlier that, memductance is always a function of applied input voltage, which implies that input signal amplitude can significantly affect the hysteresis behavior. And it can also be witnessed from the $v-i$ plots depicted in Fig. 10 for different peak input values.

Likewise, the depicted plots in Fig. 11 show the effect of biasing voltage variation on memristor behavior. In the $v-i$ plots, a significant change can be observed for different biasing voltages, which demonstrates the electronic tunability feature of the presented emulator.

To find the variation of memristance with time, the simulation has been performed for an operating frequency of 500 kHz, and the corresponding plot is shown in Fig. 12, which illustrates the variation of memristance from 0 to 20.45 k Ω . It can also be observed from Fig. 12, that there is a sharp increase in the resistance at two different instants in a complete cycle of applied sinusoidal voltage. It may be due to the presence of cross-over points in transient $v-i$ characteristics.

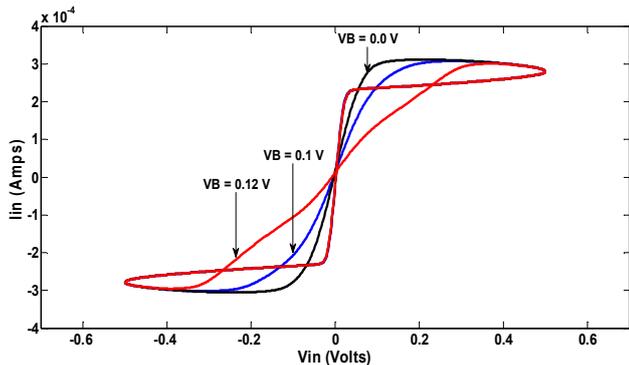


Fig. 11. Tunable behavior of realized three pinch-off memristor for different biasing voltages.

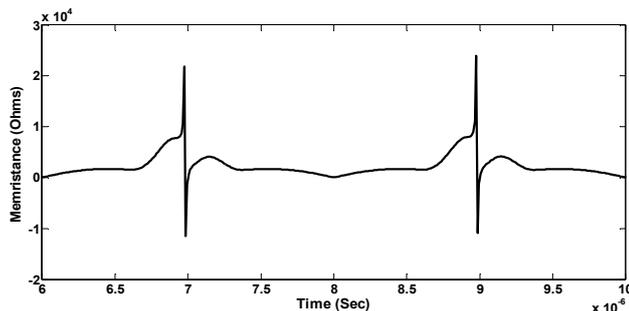


Fig. 12. Variation of memristance to time.

6. Realization of Proposed VDTA Based Three-Pinch-Off Memristor Emulator using IC LM13700

The proposed VDTA based three pinch-off memristor emulator is implemented using IC LM13700.

LM13700 is an IC consisting of two transconductance amplifier stages, whose pin diagram is shown in Fig. 13. By using a single IC LM13700, we can realize the functionality of a VDTA, which is itself based on two transconductance stages. The presented implementation has been verified using the PSPICE model of LM13700, whose performance is close to the hardware IC as claimed by the manufacturer.

Based on two LM13700s, the developed configuration of three pinch-off memristor is shown in Fig. 14. In the

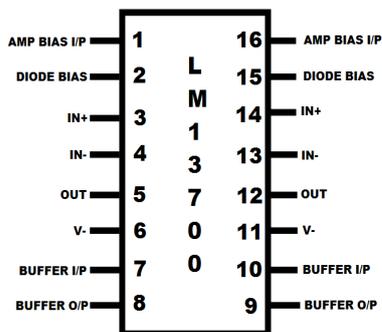


Fig. 13. Pin diagram of IC LM13700.

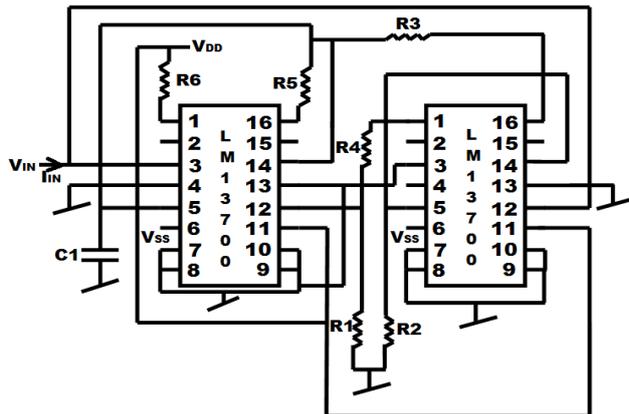


Fig. 14. VDTA based emulator shown in Fig. 7 implemented using LM13700.

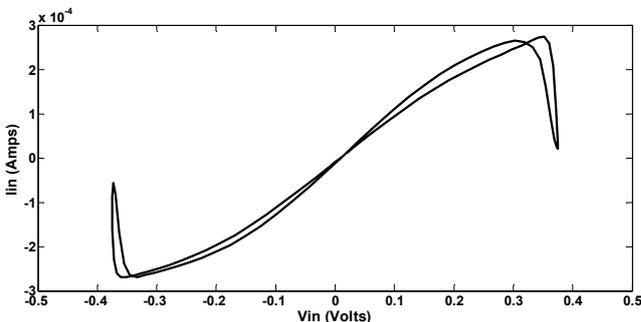


Fig. 15. Three pinch-off behavior commercial IC-based implementation shown in Fig. 14 at C1 = 1nF.

designed circuit, the values employed resistances are selected as $R1 = 50\text{ k}\Omega$, $R2 = 5\text{ k}\Omega$, $R3 = 25\text{ k}\Omega$, $R4 = 30\text{ k}\Omega$, $R5 = 30\text{ k}\Omega$, and $R6 = 25\text{ k}\Omega$. The plot shown in Fig. 15, demonstrates the three-pinch-off behavior obtained for an input signal having peak value as $V_p = 0.375\text{ V}$ at operating frequency $F_{in} = 50\text{ kHz}$.

7. Conclusion

The contribution of the article can be considered as the distinctive mathematical model of the memristive characteristics developed for the first time to explain multi-pinch-off memristive behavior. We have shown, that exhibition of extra non-zero pinch-off points by any memristor is an indication of its highly non-linear nature. Such memristors can be very useful in advanced memristive applications such as chaotic oscillators, multi-bit memory etc. Then, we have presented a VDTA based three-pinch-off emulator, which verifies the derived mathematical results. No such minimal components based emulator can be found in the literature, which offers electronically controllable characteristics with such type of non-linearity. Interestingly, due to realizing a third-order memductance, the developed memristor emulator can be very useful in multi-resistance level switching applications. Also, by varying the memristor coefficients and maintaining the derived condition in (9), we can alter the margins between these resistance levels and the values of switching thresholds

(inflection points). The presented PSPICE generated results show the behavior of the emulator circuit for different parameter variations. Its hardware implementation using LM13700 has also been presented and verified.

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About Authors ...

Kapil BHARDWAJ is currently pursuing Ph.D. from the National Institute of Technology Jamshedpur, Jamshedpur, India. His research interests include analog circuit designing and memristor emulation using new generation ICs.

Mayank SRIVASTAVA is currently working as an Assistant Professor at the National Institute of Technology Jamshedpur, Jamshedpur, India. His research interests include analog circuit designing using modern active building blocks. He has authored and co-authored more than 50 articles in various international journals and conferences.