A 0.5 V 110 nW Sensor for Temperature Monitoring of Perishable Foods

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Abstract. *Real-time monitoring solution is essential for the perishable food to estimate the food quality and to predict its shelf life. In this paper an on-chip temperature sensor which is applicable for UHF RFID passive tag is proposed. MOSFET is used as the sensitive element to the temperature. Since the transistors are biased in sub-threshold region, the power consumption is decreased. To converting proportional-to-absolute-temperature (PTAT) and complimentary-to-absolute-temperature (CTAT) voltages to the digital code, the delay generator and 8-bit ripple counter are utilized. For designing binary counter, a low power and high speed D-flip flap (D-FF) based on gate diffusion input (GDI) technique is employed. The proposed temperature sensor dissipates 110 nW power while the supply voltage is 0.5 V. Simulated in TSMC 0.18 µm CMOS technology, the total chip area is 0.0104 mm^2 and the error is –0.3/0.7°C in the temperature range of –20°C to 10°C.*

Keywords

UHF RFID, on-chip temperature sensor, low power consumption, perishable food, CTAT, PTAT

1. Introduction

Nowadays using of sensor in the RFID tag is developed in order to increase the level of controlling systems. The temperature sensor is one of the RFID sensors that have a variety of various applications such as the temperature control of patients [1], [2] and the perishable foods temperature control [3–5]. The temperature sensors are designed for the various temperatures based on their applications. In these sensors the sensitive element to the temperature can be the resistor [2], BJT transistor [6–9], or MOSFET transistor [5, 10, 11]. Among such sensitive elements to the temperature, MOSFETs have the lowest power consumption and acceptable error. To design the sensor, two signals, which are proportional to absolute temperature and complementary to absolute temperature [5] or dependent and independent on the temperature [6–9], should be created in order to measure the temperature with the comparison of these two signals.

The design of sensor with CMOS technology can be categorized into three groups: the temperature sensor based on analog to digital converter [6–8], the temperature sensor based on delay propagation and time to digital converter [5], [12] and the temperature sensor based on ring oscillator and frequency to digital converter [2, 11, 13]. The temperature sensor based on the analog to digital converter (ADC) dissipates about 80% of its power in ADC block, while it has high chip area. Therefore, despite the high accuracy, it has high power consumption and chip area which makes it unsuitable for using in RFID applications. Usually, temperature sensors based on ring oscillator and delay propagation are utilized for the purpose of having low chip area and power consumption. In the temperature sensor based on the ring oscillator, the signal which is dependent on the temperature is converted into the frequency and then with the help of frequency to digital converter (FDC) the digital data dependent on the temperature is created. In the temperature sensor based on the delay propagation, the signals dependent on the temperature are converted to the delay and then it is changed into the digital data by the time to digital converter (TDC). In general, the sensors based on the delay generator and TDC have lower power consumption and higher accuracy than the sensors based on the ring oscillator and FDC.

In this paper, the RFID passive temperature sensor with very low power dissipation, chip area and error is proposed. The sensitive element to temperature is MOSFET and for converting the PTAT and CTAT voltages to the output digital data, the delay generator and 8-bit counter with 2.5 MHz clock frequency are used. The considered temperature range is –20°C to 10°C which is commonly suitable for controlling the foodstuffs and depraving foods.

In Sec. 2, the designed temperature sensor is proposed. The simulation results are presented in Sec. 3 and finally the conclusion is stated in Sec. 4.

2. Materials and Methods

Figure 1 shows the systematic configuration of the temperature sensor. It includes four parts: the current source,

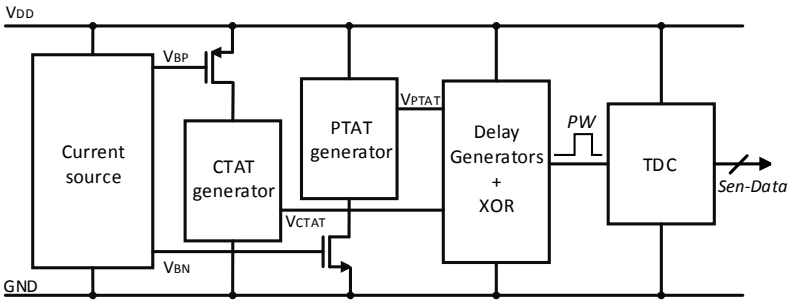

Fig. 1. The block diagram of the proposed temperature sensor of the RFID tag.

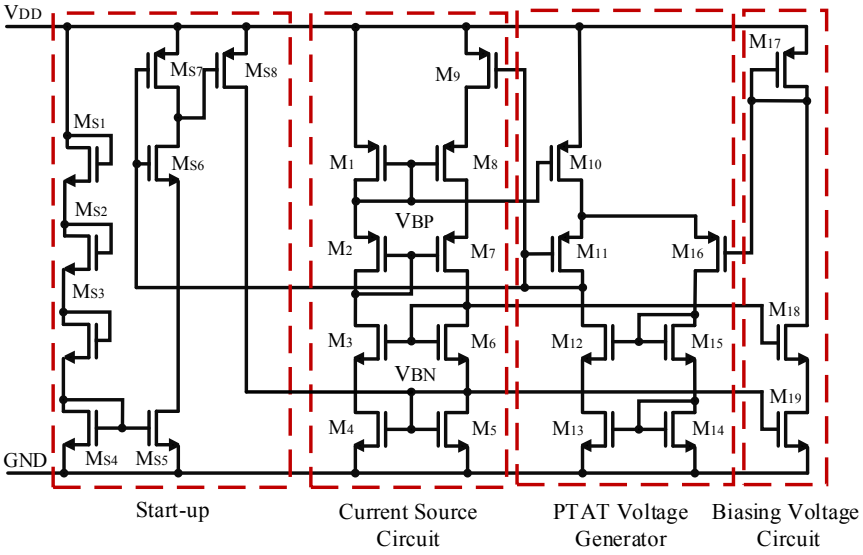

Fig. 2. The current source [15].

the core of sensor, PTAT and CTAT delay generators and the digital part of the sensor. The current source supplies the bias current of the sensor core. First, two signals which are V_{PTAT} and V_{CTAT} are produced in the sensor core by the variation of the temperature. By passing of delay generators the modulated voltage signals to the temperature are converted to the time. The output pulse widths of PTAT and CTAT delay generators are proportional to and inverse of temperature, respectively. In this process, by implementing XOR function on two output pulses the non-linear part of these signals which is dependent to the temperature is eliminated. Finally, the output pulse width is proportional to the voltage difference between V_{PTAT} and V_{CTAT} and also is dependent on the temperature linearly. Then the XOR output is changed into the digital code in the digital part of the sensor by the binary counter which counts the rising edge of clock along the pulse width during one period of sampling. The sampling period independent on the temperature is determined by the reader [14]. Then the digital code is saved in the memory of the tag digital core in order to provide the temperature data for the reader when it is necessary. For reducing the power dissipation, the analog part of the sensor is deactivated after each conversion and the sensor becomes ready for the next conversion.

2.1 The Reference Current Circuit

Figure 2 shows the presented nano-ampere reference current source [15] which supplies the required current for PTAT and CTAT voltage generators. This structure includes the start-up circuit, the current source, PTAT voltage generator and biasing voltage circuit. Unlike M_9 which works in deep triode region, the rest of the transistors work in sub-threshold region. M_9 and M_{17} have the same size and are biased with the equal current. According to [16], the reference current is calculated as

$$I_{REF} = I_{REF0} T^{2-m} \tag{1}$$

where I_{REF0} is independent of the temperature and m is the temperature exponent of the carrier mobility ($\mu = \mu_0 (T_0/T)^m$), which is a process-dependent parameter.

2.2 The Design of the Sensor Core

For designing of the proposed temperature sensor, first two V_{PTAT} and V_{CTAT} signals are produced with sensor core that by comparing these two signals, the temperature is determined. Two different structures of the PTAT voltage

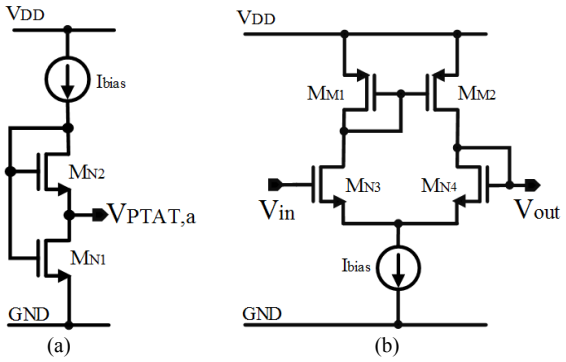

Fig. 3. (a) The classic circuit of PTAT voltage generator [17]; (b) the differential pair PTAT voltage generator [15].

generators are shown in Fig. 3. The classic PTAT voltage generator [14], in which the transistors work in sub-threshold region by employing the low supply voltage, is shown in Fig. 3(a). The PTAT voltage is the voltage difference between V_{gs} of M_{N1} and M_{N2}, which are biased in sub-threshold region. If W/L of M_{N1} is k ($k > 1$) times more than that of M_{N2} and $V_{ds,N1,2} > 4V_T$, $V_{PTAT,a}$ is calculated as

$$V_{PTAT,a} = V_{gs,N1} - V_{gs,N2} = \eta V_T \ln k \tag{2}$$

where η is the sub-threshold slope, V_T is the thermal voltage and V_{gs} is the gate-source voltage of the transistor.

Figure 3(b) shows the PTAT voltage generator presented in [15]. This circuit includes the differential pair with the current mirror circuit. When the MOSFETs work in sub-threshold region, $V_{PTAT,b}$ is achieved as

$$\begin{aligned} V_{PTAT,b} &= V_{out} - V_{in} \\ &= \left(V_{th} + \eta V_T \ln\left(\frac{I_{M_{N4}}}{(W/L)_{M_{N4}} I_0} \right) \right) \\ &\quad - \left(V_{th} + \eta V_T \ln\left(\frac{I_{M_{N3}}}{(W/L)_{M_{N3}} I_0} \right) \right) \\ &= \eta V_T \ln\left(\frac{(W/L)_{M_{N3}} (W/L)_{M_{M2}}}{(W/L)_{M_{N4}} (W/L)_{M_{M1}}} \right) \\ &= \eta V_T \ln k' \end{aligned} \tag{3}$$

where $I_0 (= \mu C_{ox} (\eta - 1) V_T^2)$ is a process-dependent parameter and V_{th} is the threshold voltage. Therefore $V_{PTAT,b}$ is gained with the condition of $k' > 1$. The PTAT voltage generator of Fig. 3(b) has more linear behavior than that of Fig. 3(a). In addition, it is more controllable for adjusting the PTAT voltage, since not only the size of differential pair transistors, but also the size of active load transistors effects on the PTAT voltage value. Figure 4 shows the proposed sensor core. This design consists of the reference current circuit and the PTAT and CTAT voltage generators. In the proposed sensor core the combination of the primary cores presented in Fig. 3, the classic and differential pair voltage generators, is used for generating PTAT voltage.

In order to increase the PTAT voltage level, the sizes of differential pair and active load transistors can be increased, which culminates in decreasing the chip area. Thus three stages of the differential pair are employed to this design for the purpose of ameliorating the voltage level. Knowing that all transistors operate in subthreshold region, V_{PTAT} is achieved as

$$\begin{aligned} V_{PTAT} &= \sum_{i=1}^{4} (V_{gs,P(2i)} - V_{gs,P(2i-1)}) \\ &= \eta V_T \ln \left(\left(\frac{(W/L)_{M_{P2}}}{(W/L)_{M_{P1}}} \right) \cdot \left(\prod_{j=2}^{4} \frac{(W/L)_{M_{P(2j-1)}} (W/L)_{M_{T(4j-4)}}}{(W/L)_{M_{P(2j)}} (W/L)_{M_{T(4j-6)}}} \right) \right) \\ &= \eta V_T \ln k''. \end{aligned} \tag{4}$$

CTAT voltage of the proposed sensor core is produced by two diode-connection MOSFETs, M_{C1} and M_{C2} which work in sub-threshold region. Based on I-V characteristic of MOSFET in sub-threshold region and replacing (1) in it, equation (5) is achieved

$$V_{gs,C1,2} = V_{th} + \eta V_T \ln\left(\frac{\left(I_{REF0} T^{2-m} \right) L}{\mu(T_0)(T_0/T)^m (\eta - 1) C_{ox} W V_T^2} \right) \tag{5}$$

in which the temperature dependence of $V_{gs,C1,2}$ is stated as

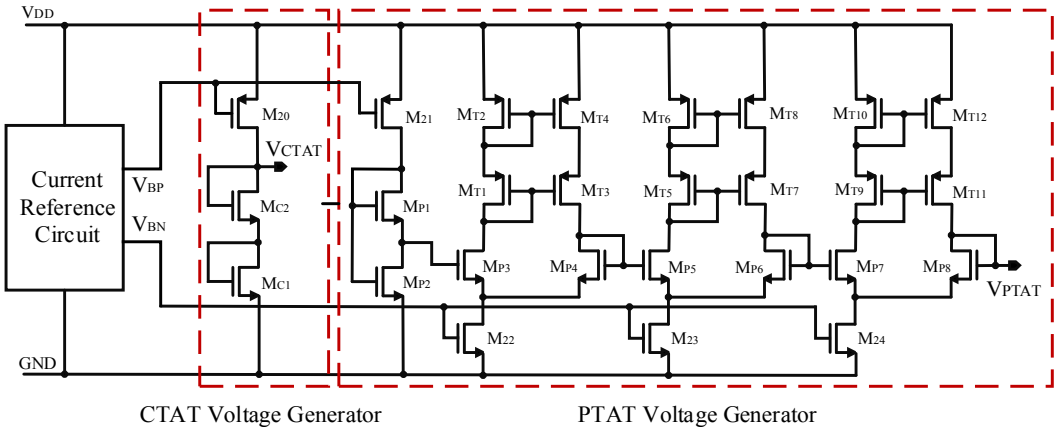

Fig. 4. The core of the proposed temperature sensor.

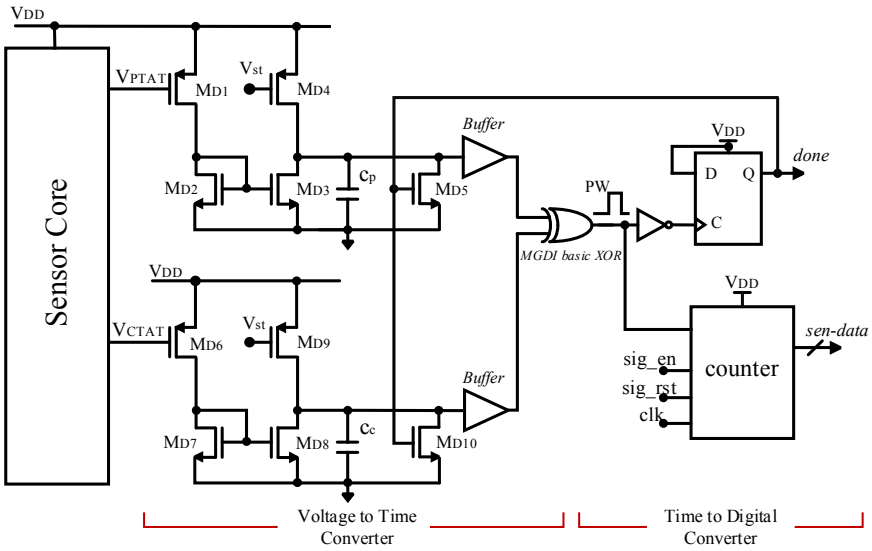

Fig. 5. PTAT and CTAT delay generators schematic.

$$\frac{\partial V_{\mathrm{gs,C1,2}}}{\partial T}=\frac{\partial V_{\mathrm{th}}}{\partial T}+\eta\frac{k}{q}\ln\left(\frac{I_{\mathrm{REF0}}L}{\mu(T_0)T_0^m(\eta-1)C_{\mathrm{ox}}W(k/q)^2}\right). \quad (6)$$

By the appropriate choosing of transistors W/L, $V_{\mathrm{gs,C1,2}}$ has the inverse relation to the temperature. CTAT voltage is gained as

$$V_{\mathrm{CTAT}}=V_{\mathrm{gs,C1}}+V_{\mathrm{gs,C2}}$$
$$=2V_{\mathrm{th}}+\eta V_{\mathrm{T}}\ln\left(\frac{\left(I_{\mathrm{REF0}}T^{2-m}\right)^2L_{\mathrm{C1}}L_{\mathrm{C2}}}{\mu^2(T_0)(T_0/T)^{2m}(\eta-1)^2C_{\mathrm{ox}}^2W_{\mathrm{C1}}W_{\mathrm{C2}}V_{\mathrm{T}}^4}\right). \quad (7)$$

2.3 The Design of the Delay Generator

Figure 5 shows the simple schematic of the PTAT and CTAT delay generators and its connection to the sensor core and digital part. The modulated temperature signals V_{PTAT} and V_{CTAT} are changed into time domain from the voltage domain by the delay generators. In the CTAT (PTAT) delay generator M_{D1} (M_{D6}) transistor and $M_{\mathrm{D2,3}}$ ($M_{\mathrm{D7,8}}$) the current mirror, transfer V_{PTAT}, the modulated temperature signal, to the C_{P} (C_{C}) and then the buffer changes the it to the time, like single_slope ADC.

At the start of each conversion, V_{st} is employed and activates M_{D4} (M_{D9}), so C_{P} (C_{C}) can charge to V_{DD} at the pre-charge process. The measurement process initiates by the rising edge of V_{st} signal which comes from the tag digital core. I_{PTAT} and I_{CTAT} discharge C_{C} and C_{P}, respectively. XOR gate is employed to the buffer outputs of these two PTAT and CTAT delay generators to produce the temperature dependent pulse. The pulse width of XOR output is dependent on pulse width of modulated temperature signals which are produced from PTAT and CTAT delay generators. The time delay of the XOR output pulse width is calculated as

$$t_{\mathrm{d\text{-}PW}}(T)\approx\frac{C_{\mathrm{P}}\Delta V}{I_{\mathrm{CTAT}}(T)}-\frac{C_{\mathrm{C}}\Delta V}{I_{\mathrm{PTAT}}(T)} \quad (8)$$

where $\Delta V\,(=V_{\mathrm{DD}}-V_{\mathrm{th}})$ is the voltage difference between V_{DD} and threshold voltage of inverter transistors at the input of buffer. The value of $I_{\mathrm{CTAT}}(T)$ and $I_{\mathrm{PTAT}}(T)$ are calculated as (9) and (10), respectively

$$I_{\mathrm{PTAT}}(T)\approx I_{\mathrm{PTAT}}(T_0)\left[1+k_{\mathrm{P}}(T-T_0)\right], \quad (9)$$

$$I_{\mathrm{CTAT}}(T)\approx I_{\mathrm{CTAT}}(T_0)\left[1-k_{\mathrm{C}}(T-T_0)\right] \quad (10)$$

where T is the instantaneous temperature, T_0 is the reference temperature, k_{P} and k_{C} are the temperature coefficient of I_{PTAT} and I_{CTAT}, respectively. By using (9) and (10) in (8) and considering only the first and second term and ignoring the rest of the terms, the XOR output pulse width is calculated as (11):

$$t_{\mathrm{d\text{-}PW}}(T)\approx\left[\frac{C_{\mathrm{P}}\Delta V}{I_{\mathrm{CTAT}}(T_0)}-\frac{C_{\mathrm{C}}\Delta V}{I_{\mathrm{PTAT}}(T_0)}\right]+\left[\frac{C_{\mathrm{P}}\Delta Vk_{\mathrm{C}}}{I_{\mathrm{CTAT}}(T_0)}+\frac{C_{\mathrm{C}}\Delta Vk_{\mathrm{P}}}{I_{\mathrm{PTAT}}(T_0)}\right](T-T_0). \quad (11)$$

As it is clear from (11), if the output pulse width of each delay generator has the non-linear relation to the temperature, after implementing XOR, the non-linear parts are eliminated and the output pulse width of the XOR has the linear relationship to the temperature. Then by quantizing the pulse width with ripple counter the digital temperature data is achieved from the same conversion. At the end of each conversion, when the edge of XOR pulse signal falls the done signal is triggered and makes C_{P} and C_{C} completely discharged. By sending of this signal, the end of conversion is determined and the sensor becomes ready for the next conversion.

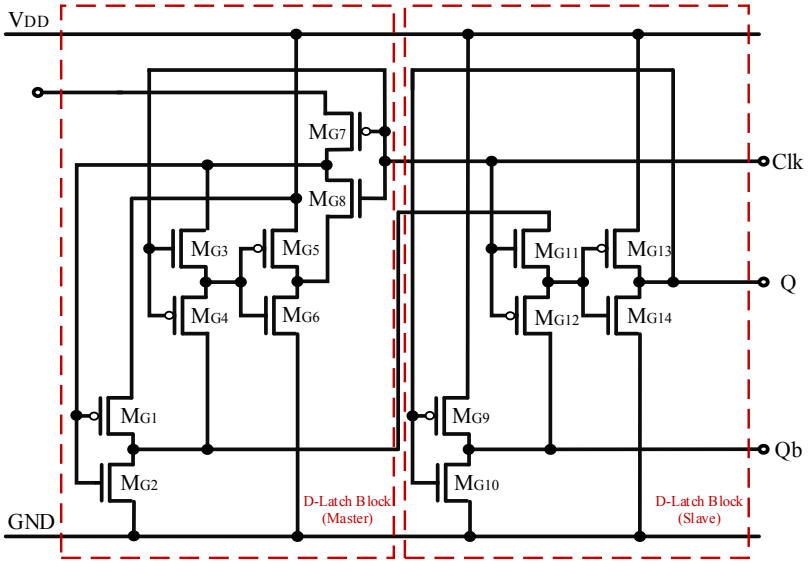

Fig. 6. The configuration of D-FF with GDI cell.

Sensor Core				Delay Generator		D-Flip Flop	
Transistor	W/L (µm/µm)	Transistor	W/L (µm/µm)	Transistor	W/L (µm/µm)	Transistor	W/L (µm/µm)
M_{20}	12/0.18	$M_{T1,5,9}$	1/0.18	$M_{D1,6}$	80/0.18	$M_{G1,5,9,13}$	3/0.18
$M_{21\text{-}24}$	16/0.18	$M_{T2,6,10}$	2/0.18	$M_{D2,3,7,8}$	0.22/20	$M_{G2,6,10,14}$	7/0.18
$M_{P1,3,5,7}$	5.5/0.18	$M_{T3,7,11}$	3/0.18	$M_{D4,5,9,10}$	0.22/0.18	$M_{G4,7,12}$	3/0.18
$M_{P2,4,6,8}$	0.5/0.18	$M_{T4,8,12}$	6/0.18			$M_{G3,8,11}$	7/0.18
$M_{C1,2}$	0.5/0.18						

Tab. 1. Transistors sizes of the proposed temperature sensor.

2.4 The Design of Ripple D-FF Counter with the GDI Technique

Figure 6 shows the novel structure of the 14-transistor D-Flip Flap (DFF) with Gate Diffusion Input (GDI) technique. GDI technique is recently developed and is efficiently replaced instead of CMOS and SOI technology in the design of logic circuits. Using this technique in the DFF structure decreases more delay, number of transistors and chip area in comparison with 18-transistor CMOS cell. GDI technique in the DFF design dissipates lower power, since it reduces the sub-threshold leakage current and the components of gate leakage current. Generally employing this technique in the ripple counter not only improves the power consumption and chip area, but also increases the speed of counter in the digital circuits of the sensor.

3. Simulation Results

The proposed temperature sensor is designed in 0.18µm CMOS technology. In this design the values of C_P and C_C are considered 1 pF. Table 1 presents the size of transistors used in this design. Figure 7 shows the output signals of the sensor core, V_{PTAT} and V_{CTAT}, in the temperature range of –20°C to 10°C.

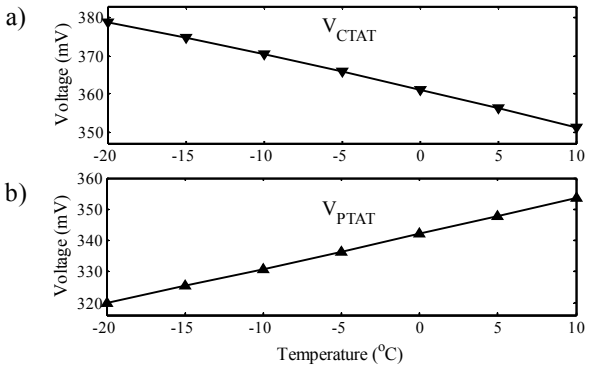

Fig. 7. The simulation results of (a) V_{CTAT}, (b) V_{PTAT} in the temperature range of –20°C to 10°C.

The output of V_{PTAT} and V_{CTAT} delay generators and also the XOR output pulse are shown in Fig. 8 at the temperature of 10°C.

Based on (11), by decreasing the temperature the pulse width is increased which is shown in Fig. 9(a). In addition, Fig. 9(b) shows the output quantized code of 8-bit binary ripple counter with 2.5 MHz clock frequency for the temperature range of –20°C to 10°C.

The linearity of the sensor is effected by the PTAT and CTAT modulated temperature signals and their delay

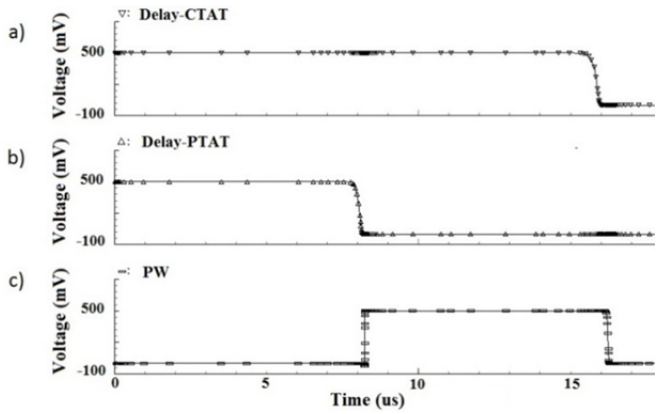

Fig. 8. (a) The PTAT delay generator output, (b) the CTAT delay generator output, (c) the output pulse of the XOR.

Reference	This Work	[2]	[5]	[9]	[12]	[18]	[10]
Architecture Type	TDC	FDC	TDC	TDC	TDC	FDC	TDC
Process [µm]	0.18	0.35	0.18	0.18	0.35	0.18	0.18
Supply voltage [V]	0.5	2.1	0.5 to 1	0.6 to 1	-	1	0.65
Power Consumption [µW]	0.11	0.11	0.119	0.9	10	0.22	1.3
Temperature Range [°C]	–20 to 10	35 to 45	–10 to 30	–20 to 30	0 to 100	0 to 100	−15 to 65
Error [°C]	–0.3/0.7	±0.1	–0.8/+1	±0.8	–0.7/+0.9	–1.6/+3	−0.3/+0.27
Area [mm^2]	0.0104	-	0.0416	-	0.175	0.05	0.11

Tab. 2. The comparison of the proposed sensor with other schemes.

generators. The process variation and mismatch of the sensor core transistors $M_{C1,C2}$ and $M_{P1\text{-}P8}$, the current mirror transistors $M_{T1\text{-}T12}$ and the used capacitors in the delay generators are the most important factors in the existence of the proposed temperature sensor error. Figure 10 shows the Monte Carlo simulation results of the sensor error for 100 runs that the mean and standard deviation are 0.18°C and 0.33°C, respectively. According to Monte Carlo simulation, the measured error of the samples varies in the range of –0.3°C to 0.7°C in the temperature range of –20°C to 10°C.

The comparison of the results of the proposed temperature sensor with some recently designed sensors is presented in Tab. 2. In comparison with the other sensors, the proposed sensor has the lowest chip area and power dissipation as its transistors work in sub-threshold region.

The layout of the proposed sensor, which occupies 0.0104 mm^2 area, is shown in Fig. 11.

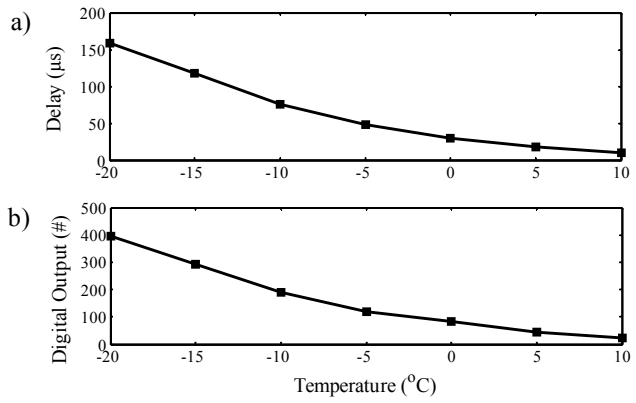

Fig. 9. (a) The pulse width of the XOR output. (b) The output of counter at the temperature range of –20°C to 10°C.

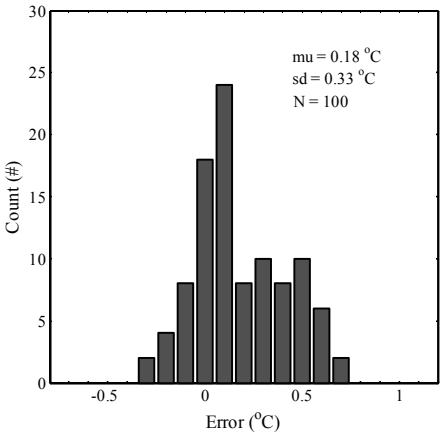

Fig. 10. The simulated error of the samples at the temperature range of –20°C to 10°C using 100 runs.

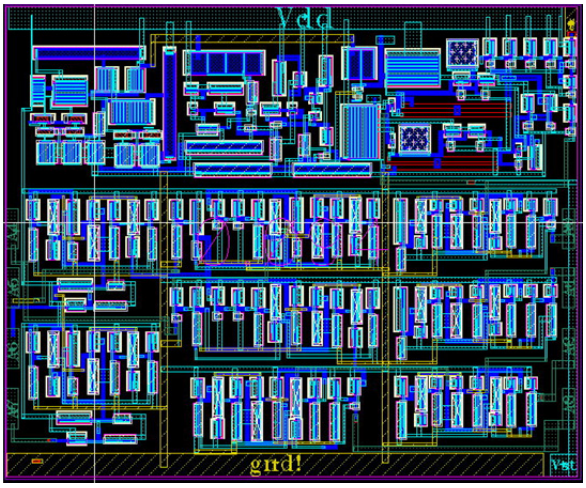

Fig. 11. The layout of the proposed temperature sensor.

4. Conclusion

A low power CMOS sensor is designed for temperature control of the perishable foods at the temperature range of –20°C to 10°C. The sensor core transistors work in sub-threshold region. D-FF based on GDI technique is employed to the counter instead of conventional D-FF to reduce the power dissipation. Considering 0.5 V supply voltage and 10°C temperature, the power dissipation of the sensor core, delay generator and digital part is only 110 nW. This sensor which has low power dissipation and low chip area is suitable for RFID tag applications. Using the Cadence software, the temperature sensor is simulated in 0.18µm CMOS technology.

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