# A Self-Start-Up Sub-Threshold DC/DC Boost Converter Using Bootstrap Driver for Self-Powered Sensor Nodes

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Abstract. In this paper, a fully autonomous and integrated sub-threshold DC-DC converter is presented for energy harvesting from ambient sources to self-powered IoT nodes. The proposed converter and its clock generator are designed by exploiting body biasing technique for low power operation and operate in sub-threshold regime. This bulk driven technique can dynamically enhance the on-current during conducting state and decrease reverse current during the non-conducting state. A bootstrap driver with dynamic body bias is employed to drive the phase generator at the output of the ring oscillator to decrease the settling time of the charge pump. This further improves the driving capacity of the clock along with extended rail to rail output voltage swing. Also, a novel cross clock scheme is proposed to improve the output voltage's transient response and conversion efficiency of a converter by reducing reverse current loss. The proposed circuit is implemented in CMOS 0.18 µm process. The proposed design requires very low start-up voltage of 400 mV and exhibits output voltage of 1.98 V, settling time of 33 µs, and pumping efficiency of 99% with a total power dissipation limited to just  $1.5 \mu W$ .

# **Keywords**

Bootstrap driver, body biasing, charge transfer switches (CTS), DC-DC converter, internet of things (IOT)

# 1. Introduction

Nowadays, a large number of wireless sensor nodes (WSNs) are connected in a network to realize smart systems such as the Internet of things (IoT), smart homes, and intelligent grid. However, due to their widespread and existence in large number, these systems require low maintenance, low area, and seamless operation without replacement of the battery. Micro energy harvesting has been recently emerging as a promising solution to power up such systems [1]. However, the harvester's output voltage is a few hundred mill volts (e.g., the output voltage of an amorphous single photovoltaic cell is between 0.3 V and 0.6 V) [2]. Usually, such low voltage is not sufficient enough to power these circuits. Consequently,

a power management unit (PMU) with the DC-DC boost converter is strongly required to raise the voltage level proportionate to the desired voltage level. The DC-DC converter in self-powered devices needs operating voltage higher than the MOS device's threshold voltage to achieve high conversion efficiency. Several start-up mechanisms have been implemented in the literature to trigger the converter in such a low voltage range. The boost converter in [3] recharges the auxiliary battery for one time. The converter in [4] employs a mechanical vibrator that is triggered by kinetic energy (KE) in motion to power up the portable IoT node. The work in [5] uses a transformer-based start-up circuit, which requires a very large turning ratio. Post-fabrication threshold voltage tuning is developed in [6] to enable the low voltage operation. However, all these start-up mechanisms utilize external excitation.

Self-start-up on-chip DC-DC converters realized with inductors have also been investigated [7]. A combination of low threshold voltage MOSFETs and switched inductor used in [8] was designed to operate in the low input voltage range. However, it suffers from low-quality factor integration, high cost, and inefficient chip usage. On the other side, integrated inductor less dc/dc converters also referred to as a charge pump (CP), can provide the best integration solution to make compact self-powered IoT devices. The first fully integrated inductor less DC-DC converter was developed by Dickson in 1976 [9]. It was simply implemented with chain of NMOS diode-connected MOSFETs that operate in cut-off or saturation region. The steady-state output voltage of the NMOS diode-connected MOSFET CP can be defined as:

$$V_{\text{out}} = (V_{\text{IN}} - V_{\text{th}}) + N \left( \frac{V_{\phi}}{1 + \alpha_{\text{p}}} - V_{\text{th}} \right) - N \frac{I_{\text{L}}}{f_{\phi(1 + \alpha_{\text{p}})C^{\text{k}}}} \quad (1)$$

where  $V_{IN}$  is the supply voltage,  $V_{th}$  is the threshold voltage, N is the number of stages,  $\alpha_p$  is the ratio of pumping capacitance ( $C^k$ ) to top parasitic capacitance, and  $V_{\phi}$  is the clock amplitude. From the above equation, it can be seen that  $C^k$ ,  $V_{\phi}$ , and  $V_{th}$  limit the voltage gain and efficiency. Thereafter, to improve the efficiency and voltage gain in [9], many control techniques have been investigated [10]. Although charge transfer switches (CTSs) are turned off, non-negligible reverse saturation current flows through the CTSs, which degrades conversion efficiency. A linear charge pump (LCP) with improved conversion efficiency using a gate-controlled switch technique was presented in [11]. However, CTSs in LCP cannot be completely turned on/off when the supply voltage is lower than the MOSFET's threshold voltage. A latched CP (also referred to as cross-coupled charge pump) using a simple two-phase complementary scheme was presented in [12] and same was introduced in [13]. This two branch structure using latch configuration generates the differential doubled output voltage with the near-zero voltage drop across each CTS. Also, this structure reduces the ripple voltage and improves efficiency. Successively, the works in [14] improve the conversion efficiency using hybrid structure. The stage, which is connected to supply, employs three latched cells connected in parallel so that the power extraction can be done optimally from power sources. The next stage, which is connected to load, works typically as a conventional charge pump to boost the pumping efficiency at the target level. Incompetent with prior works, latched CPs have several advantages. However, they do not work well for low voltage applications. To make IoT devices operate at low voltages, some interesting solutions have been provided in the literature. The converter presented in [3] can operate with low supply voltage using Carbon Nano-tube FETs (i.e., CNFETs) that offer devices with a low threshold voltage. Another high efficiency switched converter in [15], which offers low threshold voltage, was implemented in 65nm node. On the other side, to make them less dependent on the threshold voltage of the MOS device in various charge pump topologies, bulk biasing techniques [15] using proper bias of the MOSFETs' well (i.e., p-well for NMOS and n-well for PMOS in the triple-well process) are used. One of the high-performance latch based CPs was proposed in [16] where gates and bulks dynamically adjust the bulk voltage to enable the circuit operates at minimum operating voltages. However, the requirement of an extra complex circuit at the last stage of CP is a major drawback of it. The forward body biasing for latch based CP was proposed in [17]. In this method, all MOSFETs are forward biased, thus resulting in higher on-current. In this biasing scheme, the enhanced on-current is higher than bulk leakage current that allows the low voltage operation of the CP. Nevertheless, the high inverse saturation current through NMOS transistor during the non-conducting phase of switches decreases the end-to-end conversion efficiency of the CP.

This work aims to implement a simple self start-up low voltage DC-DC boost converter with compact size, high conversion efficiency, and low settling time. The proposed converter and its clock generator, which operate in sub-threshold, are designed by expoliting body biasing technique using auxiliary transistor for low power operation with no external start-up circuit. This bulk driven technique can dynamically enhance the on-current in conducting state and decrease reverse current in the non-conducting state. Working in low supply voltage has a benefit of low power dissipation, but CPs suffer from poor conversion efficiency due to reverse current loss. To address this issue, a novel cross clock scheme is proposed to improve the output voltage's transient response and conversion efficiency of a converter by reducing reverse current loss. Also, a bootstrap driver with dynamic body bias is employed to drive the phase generator at the output of the ring oscillator in order to decrease the settling time of the charge pump. This further improves the driving capacity of the clock along with extended rail to rail output voltage swing. The remainder of this paper's workflow is as follows: Section 2 presents the implementation of the proposed DC-DC booster converter. Section 3 discusses the functionality of the implemented prototype, which is validated using postlayout simulations. Finally, the conclusion is given in Sec. 4.

# 2. Proposed Bootstrap Based DC/DC Boost Converter

#### 2.1 Four Stage Latched Charge Pump

The basic block diagram of the DC-DC boost converter and the proposed DC-DC boost converter using bootstrap driver are depicted in Fig. 1. A latch based charge pump is exploited in the proposed boost converter to achieve low ripple voltage and better charge transferability than preceded charge pump topologies [9–11]. Nevertheless, to improve the performance metrics of the latched CP in the low voltage range, a few modifications are essential; one of the possible solutions to allow the CP for low voltage operation is bulk biasing technique. So, a latched CP using body biasing with auxiliary transistor technique is designed to implement the proposed self-start-up DC-DC boost converter, as depicted in Fig. 2. As shown in Fig. 2, body biasing, which effectively turns on/off CTSs in the sub-threshold regime, is applied to both PMOS CTS and NMOS CTS in CP. As a result, the sub leakage current decreases and transient characteristics of CTS are improved. And also, to achieve high conversion efficiency with a low input voltage, a dc/dc boost converter with high conversion ratio is needed; however, a large pumping capacitance in circuit is also required. Thus, the proposed converter can provide high conversion ratio with small pumping capacitance.

On the other side, the undesired charge flows between the input node and output of CP due to improper timing clock transitions by switching clocks, so the end to end efficiency deteriorates significantly. To address this problem up to some extent, non-overlapping clocks can be used in dual-phase clock scheme circuit, but the undesired charge still exists in this case as well, and also generating perfect non-overlapping clocks is not possible in reality. Successively, several control schemes using an auxiliary circuit for CTSs were developed in [18]. In this paper, without using any auxiliary circuit and non-overlapping clocks, a novel cross clock scheme is proposed to improve the output voltage's transient response and conversion efficiency. CLK and CLKB, which are two cross clocks generated from the clock generator, have amplitudes that are same as the amplitude of the supply voltage.



Fig. 1. a) Basic architecture of the boost converter. b) Proposed architecture of the boost converter.



Fig. 2. Four stage charge pump with bootstrap clock generator.

The operation of the first stage is as follows. When the clock signal CLK is low, and CLKB is high, voltages at nodes P and Q are  $V_{IN}$  and  $2V_{IN}$ , respectively, so  $N_{2-CP}$ ,  $N_{b2}$ ,  $P_{1-CP}$ ,  $P_{b1}$  are turned ON and charge transfers consequently from the input node to node Q. Also, applied body biasing technique improves the conductance of N<sub>2-CP</sub> and P<sub>1-CP</sub> while ensuring proper forward biasing of substrate junction diodes even for low input voltages, thus resulting in high oncurrent. On the other hand, charge transfer switches (i.e.,  $N_{1-CP}$  and  $P_{2-CP}$ ) and their respective auxiliary transistors are turned off so that reverse current is prevented at the later stages. Hence, the output of the first stage, when the clock signal CLK is low and CLKB is high, is 2V<sub>IN</sub> in the first half cycle. During the other half cycle, voltages at nodes P and Q are  $2V_{IN}$  and  $V_{IN}$ , respectively, so  $N_{b1}$ ,  $N_{1-CP}$ ,  $P_{2-CP}$ ,  $P_{b2}$ are turned ON, and charge transfer switches  $N_{2-CP}$ ,  $P_{1-CP}$ are turned OFF. Consequently, the output voltage of the first stage is  $2V_{\rm IN}$  in the second half cycle. Therefore, the output voltage always remains as  $2V_{IN}$  during the complete full cycle. The same operation is applicable to the next stages of the charge pump. Sizing of the charge transfer switch is discussed in the next section.

#### 2.2 Sizing of CTS

Body of the CTSs (i.e.,  $N_{2-CP}$  and  $P_{2-CP}$ ) in Fig. 3 are biased by single transistor at each CTS. As CLK is high, and CLKBis low,  $N_{2-CP}$  turned on, and the node voltage of 'g' is charged to a higher level.  $N_{b2}$  are also turn on during this time interval which shorts the  $p, q, b_2$ . The relation among the  $p, q, b_2$  is given by

$$V_{b2} = V_q \le V_p. \tag{2}$$



Fig. 3. NMOS-CTS and PMOS-CTS.

On the other hand,  $N_{2-CP}$ ,  $N_{b2}$  are turned off when CLK is low, and CLKB is high.  $V_{b2}$  is mainly determined by the capacitance model of  $N_{2-CP}$ ,  $N_{b2}$ that can be expressed as

$$V_{b2} = V_g \frac{C_{gb(N_{2-CP})} + C_{gb(N_{b2})}}{C_{T}} + V_q \frac{C_{sb(N_{2-CP})} + C_{db(N_{b2})}}{C_{T}} + V_p \frac{C_{db(N_{2-CP})}}{C_{T}}$$
(3)

where  $C_{\rm sb}$ ,  $C_{\rm gb}$ ,  $C_{\rm db}$  are  $N_{2-\rm CP}$ 's source-body, gate-body, drain-body capacitance, respectively, while  $C_{\rm gb}(N_{b2})$  is gatebody capacitance of  $N_{b2}$ ,  $C_{\rm db}(N_{b2})$  is drain-body capacitance of  $N_{b2}$ . Source-body capacitance of  $N_{b2}$  is ignored because of source and body shorted and  $C_{\rm T}$  is  $C_{\rm s} + C_{\rm gb}(N_{2-\rm CP}) + C_{\rm db}(N_{2-\rm CP}) + C_{\rm db}(N_{b2}) + C_{\rm gb}(N_{b2})$ ,  $C_{\rm s}$  is stray capacitances inculding the  $N_{2-\rm CP}$ ,  $N_{b2}$ 's substrate capacitance. As  $N_{2-\rm CP}$  is turned on then  $V_q < V_p \le V_g$  and consider  $C_{\rm sb}(N_{2-\rm CP}) + C_{\rm db}(N_{b2})$  is negliable compared to  $C_{\rm T}$ , then (3) can be simplified as

$$V_{b2} = V_p \left( \frac{C_{\text{gb}(N_{2-\text{CP}})} + C_{\text{gb}(N_{b2})} + C_{\text{db}(N_{2-\text{CP}})}}{C_{\text{T}}} \right).$$
(4)

Let

$$\alpha = \frac{C_{\rm sb(N_{2-CP})} + C_{\rm db(N_{b2})} + C_{\rm s}}{C_{\rm gb(N_{2-CP})} + C_{\rm gb(N_{b2})} + C_{\rm db(N_{b2})}}.$$
 (5)

We get  $V_{b2}$  in (6)

$$V_{b2} = \frac{1}{1+\alpha} V_p. \tag{6}$$

 $C_{\rm gb(N_{2-CP})}$  is much larger than  $C_{\rm db(N_{b2})}$ ,  $C_{\rm s}$ ,  $C_{\rm sb(N_{2-CP})}$ . As a result, we can  $\alpha << 1$  by choosing the moderate size of  $N_{b2}$ , 10% of  $N_{2-CP}$  is acceptable such that these capacitors have smallest values. And the relation among the  $p, q, b_2$ when CLK is low, and CLKB is high are expressed in (7)

$$V_{b2} = V_q > V_p. \tag{7}$$

From (2) and (7), it can conclude that  $V_{b2}$  follows closely to the lower one between  $V_p$  and  $V_q$  which makes sure that the bulk-source and bulk-drain PN junction is not turned on and suppress the junction leakage current. Moreover, when  $N_{2-CP}$  is turn-on in CLK is high, and CLKB is low,  $N_{2-CP}$ 's body and the source are short, which prevents  $N_{2-CP}$  from body effect. And analysis of charge transfer switch  $P_{2-CP}$  is analogous to NMOS-CTS.

#### 2.3 Clock Generator

Figure 1(b) shows the block diagram of the proposed dual-phase clock generator that can generate cross couple clocks with 50% duty cycle. It consists of a five-stage stack ring oscillator, followed by the bootstrap driver, phase generator, and buffers. The clock generator circuits, which were proposed for low voltage applications in the literature [19], pose several challenges. While implementing a clock generator for low voltage (LV) applications, one of the primary challenges is to design ring oscillator that can produce out of phase-clocks with well-output current driving capability. The ring oscillator must be operated in the weak inversion region or sub-threshold region for LV applications. However, when the harvester output voltage is less than the MOS threshold voltage that has a typical threshold voltage of 0.5 V in 0.18 µm CMOS process, the device must work in the weak inversion region, thereby allowing a small amount of current. Consequently, MOS devices exhibit poor drivability and low electrical characteristics. Hence, oscillator's performance deteriorates.

A bulk biasing technique is exploited to improve device drivability and electrical properties in sub-threshold circuits by adjusting the threshold voltage. The relationship between the threshold voltage and source bulk voltage [20] is given by

$$V_{\rm th} = V_{\rm th0} + \gamma (\sqrt{2 |\phi_{\rm F}| + V_{\rm SB}} - \sqrt{|2\phi_{\rm F}|})$$
(8)

where  $\gamma$  is the substrate bias coefficient (body effect parameter,  $V_{\text{th0}}$  is the threshold voltage for zero substrate bias



Fig. 4. Stacked ring oscillatorand bootstrap driver using DBB technique.

(i.e.  $V_{SB} = 0$ ),  $\phi_F$  is substrate Fermi potential,  $V_{SB}$  is the substrate-body voltage. It is observed from the equation that as bulk source voltage  $(V_{SB})$  increases, the threshold voltage of the transistor increases, and consequently reverse saturation current of the OFF device decreases, which usually exists in reverse body biasing (RBB). Similarly, as V<sub>SB</sub> increases, the transistor's threshold voltage decreases, and consequently conductance of ON device increases, which generally occurs in forward body biasing (FBB). On the other hand, to obtain both of the benefits discussed above, dynamic body biasing (DBB), a combination of FBB and RBB, is used. Therefore, DBB based ring oscillator (RO), which is depicted in Fig. 4, is exploited in this work. To obtain target frequency, a chain of five stages stacked inverter is utilized, and the size of the inverter is kept small [14] to lower the threshold voltage  $(V_{\rm th})$ . Moreover, the stacked inverters in RO reduce power consumption since the leakage current represents an essential part of the circuit's total consumption when the circuit operates at low voltages. The current leakage can be reduced by means of the stacking effect of transistors [21]. To improve the speed of the CMOS sub-threshold circuits in which drivability is challenging task, several bootstrap drivers have been investigated [22,23]. In the proposed work, a bootstrap technique is incorporated between ring oscillator and phase generator to enhance the load drivability and rail to rail clock output swing of clock generator without increasing overall circuit's power much. Figure 4 depicts the bootstrap driver using dynamic body biasing where  $C_{B1}$  and  $C_{B2}$  are two bootstrap capacitors, N<sub>B1</sub>, N<sub>B2</sub>, N<sub>B3</sub> are NMOS transistors, and  $P_{B1}$ ,  $P_{B2}$ ,  $P_{B3}$  are PMOS Transistors. As shown in Fig. 4, the combination of bootstrap capacitors and DBB technique makes the input signals to overcome the shortage of gate overdrive problems for low voltage operation where input voltages are less than MOS device's threshold voltage. The bootstrap capacitors  $C_{B1}/C_{B2}$  with pre-charge charge transistors and the driver transistors using DBB can resolve the issue that is related to a shortage of gate overdrive voltage. Consequently, the driving speed of the clock generator becomes better. The output of the bootstrap driver is fed to Phase generator, which can produce dual-phase cross clock signal. Figure 6 shows the schematic of the phase generator [24] that is composed by transmission gate, inverter, and buffer. Usually, phase

generator circuit is used to produce non-overlapping clocks. It is implemented by using a dual-branch chain of dual input inverters [17] or by using a chain of at least eight NAND and NOT gates [25]. Thus, significant power drop occurs when the dc/dc boost converter is used for low-power applications. A phase generator circuit, designed in this work with a count of 8 transistors, consumes less power, which is a tremendous advantage for self-powered IoT nodes. In the last stage, large sized progressive buffers are employed to eliminate the undesired glitches in the final clock signal.

## 3. Results and Discussions

To verify the benefits of the proposed solution, a fourstage latched charge pump with and without bootstrap driver with 400 mV supply voltage using auxiliary body biasing is implemented and simulated using UMC180 nm triple-well CMOS process.

Figure 5 illustrates the layout of the proposed DC-DC converter with an area of 193  $\mu$ m × 91  $\mu$ m in which the pumping capacitors occupy the major active area. Each pumping capacitor of the charge pump is chosen as 1 pF, and the capacitors in the bootstrap driver are chosen as 103 fF. For all simulations, the switching frequency is set to 4 MHz



Fig. 6. Two-phase generator using DBB technique with large size buffers.



Fig. 5. Layout of the proposed architecture of the boost converter.

The proposed CP with dynamic bulk biasing is investigated at the supply voltages of 320 mV and 400 mV regarding output voltage, settling time  $(T_s)$ , power dissipation, voltage conversion efficiency (VCE), voltage ripple  $(V_{\gamma})$ , and rampup current  $(I_r)$ . Table 1 describes the simulated results for 1 pF load capacitance. Figure 7 shows output voltage transient response of the converter with bootstrap driver under the different supply voltages (i.e., 0.3 V, 0.32 V, 0.36 V, 0.4 V, and 0.44 V) at no-load condition. As shown in the figure, when the supply voltage increases, the response speed increases (i.e., start-up time reduces from 395 µs at 300 mV to about 10 µs at 440 mV). Also, the steady-state output voltage magnitude increases from 1.47 V to 2.18 V. Figure 8 depicts the proposed circuit's output voltage transient response with and without bootstrap driver and its corresponding cross clocks with a 50% duty cycle. Figure 9 illustrates the output transient response using non-overlapping clocks scheme with a 49% duty cycle at a supply voltage of 0.4 V. It can be observed from Fig. 8 and Fig. 9 that cross clocks scheme achieve the output voltage of 1.98 V and 1.91 V with a settling time of 33 µs and 60 µs with bootstrap and without bootstrap driver case. Simultaneously, non-overlapping clock scheme achieves the output voltage of 1.94 V and 1.88 V with settling time of 84 µs and 128 µs with and without bootstrap driver, respectively. However, the proposed circuit with the cross-clock scheme has better steady output voltage level and settling time than the non-overlapping clock scheme. Figure 10 compares pumping efficiency of the proposed design

Parameters	Power supply			
	$V_{\rm IN} = 320 \rm mV$	$V_{\rm IN} = 400  {\rm mV}$		
$V_{\rm OUT}$ [V]	1.58	1.98		
$T_{\rm s}$ [µs]	206	33		
Power [µW]	140.7	1.34		
V <sub>ripple</sub> [mV]	3.8	4.5		
Vripple/VOUT	0.24	0.22		
<i>I</i> <sub>r</sub> [μA]	0.007	0.06		
VCE [%]	98.7	99		
G i d i d i d Vout				

 $C_{\text{out}}$  is the output capacitance,  $I_{\text{r}} = C_{\text{out}} \frac{v_{\text{out}}}{T_{\text{s}}}$ 

**Tab. 1.** Simulation results of the proposed converter at 320 mV and 400 mV supply.



Fig. 7. Transient responce of the output voltage for various supply voltages (300 mV, 320 mV, 360 mV, 400 mV, 440 mV).

with and without a bootstrap driver at various supply voltages. The achieved pumping efficiencies are more than 99% and 97% of the ideal value for the supply voltages ranging from 300 mV to 470 mV in with and without bootstrap driver cases, respectively. Therefore, the proposed converter with the bootstrap driver has much higher pumping efficiency than without bootstrap driver.



Fig. 8. Transient responce of the output voltage with and without bootsrap driver using cross-clock scheme at 400 mV.



Fig. 9. Transient responce of the output voltage with and without bootstrap driver using non-overlapping clock scheme at 400 mV.



Fig. 10. Pumping efficiency with and without bootstrap driver for different supply voltages.

Figure 11 illustrates the dependency of the proposed circuit's start-up time with and without bootstrap driver on the supply voltage. It is noticed from Fig. 11 that as the input voltage increases, the settling time require to settle the output decreases. It can be observed that less start-up time is achieved in with bootstrap driver's case than without a bootstrap driver's case. Figure 12 illustrates settling time under various load capacitances. As load capacitance increases from 1 pF to 10 pF, circuits with and without bootstrap driver require settling times range from 33 µs to 101 µs and 57 µs to 132 µs, respectively. The output versus various load currents of the designed circuiput voltage is plot with and without bootstrap driver for a supply voltage of 400 mV, as shown in Fig. 13. When the load current ranges from 10 nA to 200 nA, the output voltage varies from 1.96 V to 1.32 V and 1.89 V to 0.9 V in with and without bootstrap driver cases, respectively. It can be observed that as load current increases, the output voltage decreases due to decreased load resistance. The designed charge pump with the bootstrap technique performs better compared to without bootstrap technique at different load currents. Table 2 describes the effect of the load capacitor on the proposed CP for 0.4 V supply voltage. It can be observed that the high value of  $C_{\rm L}$  increases start-up time  $(T_s)$  and decreases the ripple. The simulation transients under dynamic conditions are shown in Fig. 14 and Fig. 15. It can be observed that there is no significant change voltage drop till 72 nA and 51 nA in with and without bootstrap driver cases. So, the proposed converter can cope up with the load transients as well. As illustrated in Fig. 16, efficiency is better at high loads compared to low loads.

<i>C</i> <sub>L</sub> [pF]	V <sub>out</sub> [V]	$V_{\gamma} [mV]$	$T_{\rm r}[\mu s]$	$I_{L(m)}$ [nA]
1	1.98	4.5	33	72
5	1.97	2.2	79	77
10	1.97	0.9	101	79
20	1.97	0.3	209	81

 $I_{L(m)}$  [nA] is maximum steady-state current that can be provided without significant voltage degradation.

**Tab. 2.** The effect of the load capacitor on the proposed CP for 0.4 V supply.



Fig. 11. Settling time with and without bootstrap driver for various supply voltages.

The incorporation of a bootstrap circuit results in achieving better efficiency than without a bootstrap circuit at both low and high loads. Therefore, the maximum efficiencies achieved are 33.6% and 29.4% with and without bootstrap circuits, respectively. Figure 17 illustrates transient output voltage response over various bulk topologies. It is concluded that the CP using dynamic body biasing with auxiliary transistor has better transient response than existing topologies.



Fig. 12. Settling time with and without bootstrap driver for various load capacitances.



Fig. 13. Output voltage with and without bootstrap driver for various load currents.



Fig. 14. Transient response of the output voltage with bootstrap driver for various load currents.



Fig. 15. Transient response of the output voltage without bootstrap driver for various load currents.



Fig. 16. Power conversion efficiencywith and without bootstrap driver for various load currents.



Fig. 17. Transient responce of the output voltage for various body biasing topologies.

Table 3 presents corner analysis outcomes for various temperatures at the supply voltage of 400 mV. The corner slow-slow (SS) at 0°C is the worst corner, where the voltage conversion efficiency and settling time are equal 79.76% and 246  $\mu$ s, respectively. Post-layout Monte Carlo simulations further evaluate the robustness of the boost converter against process variations. Figure 18 illustrates Monte Carlo simulations for voltage conversion efficiency over 1000 iterations at the worst corner under the supply voltage of 400 mV and clock frequency of 4 MHz.



Fig. 18. Monte Carlo simulation result for voltage conversion efficiency at the worst-case corner (SS at 0°C).

Parameter	Corner	Temperature [°C]		
1 al aniciel		0	27	75
Settling Time [µs]	SS	248	130.6	60
	TT	80	33	19
	FF	26	18	9.2
Power [µW]	SS	0.367	0.721	3.83
	TT	0.714	1.3	6.05
	FF	1.1	1.939	8.2
%VCE	SS	79.76	93.08	96.9
	TT	97.7	99	98.12
	FF	99.11	99.1	98.38

**Tab. 3.** Corner and temperature simulation results of the proposed converter.

As shown in Fig. 18, it has a mean of 78.58 and normalized standard deviation of 2.8m. Moreover, Monte Carlo simulation power consumption, shown in Fig. 19, results in the average power consumption of 1.3  $\mu$ W, and standard deviation of 214.4 nW. Figure 20 illustrates total power consumption of the proposed DC-DC converter. Finally, Table 4 depicts the performance comparison of the designed charge pump with state-of-the-art designs. In order to make a fair comparison, figure of merit (FOM) is estimated using (9)

$$FOM = \frac{P[\mu m] \times VCE\% / V_{\rm IN} \times CR}{N \times V_{\rm min}}.$$
 (9)

This FOM includes several performance metrics such as CMOS process node ( $P[\mu m]$ ), voltage conversion efficiency at that supply voltage ( $VCE\%/V_{IN}$ ), conversion ratio (CR), no of stages (N), and minimum start-up voltage ( $V_{min}$ ). The proposed design in [16] has better FOM than the proposed converter but uses external auxiliary capacitors and complex clocking scheme. The charge pump in [26], which is implemented in 65 nm node, offers a lower value of threshold voltage for MOSFETs than that of the proposed design. However, without going to lower technology, the proposed circuit, which is implemented in 180 nm, offers almost the same performance as achieved by charge pump in [26]. Also, in comparision with prior works, the proposed circuit has a high conversion ratio, low power consumption, and low settling time.

Parameters	<b>2014</b> [16]	<b>2018</b> [17] <sup>a</sup>	<b>2020</b> [26] <sup>a</sup>	This Work <sup>a</sup>	
Technology node [nm]	180	180	65	180	180
Topology	Latched CP	Latched CP	Latched CP	Latched CP	Latched CP
Number of stages	6	4	4	4	4
min V <sub>IN</sub> [mV]	320	400	400	320	400
Settling time $(T_s)$ [µs]	100	30	33.5	206	33
Clock frequency [Hz]	450k	4M	4M	4M	4M
VCE [%]	89	95.7	99	98.7	99
Conversion ratio	8.87	4.7	4.95	4.93	4.95
Load capacitor [pF]	50.7p	1p	160p	1p	1p
Chip area [mm <sup>2</sup> ]	1.37	0.018	0.021	0.017	0.017
FOM	2.31	1.24	0.49	2.13	1.36

<sup>a</sup> post-layout simulations; NA: not available

Tab. 4. Performance comparison of the proposed charge pump with state-of-the-art designs.



**Fig. 19.** Monte Carlo simulation result for power consumption at the TT corner (27°C).



Fig. 20. Power consumption of the proposed DC-DC converter.

## 4. Conclusion

In this paper, a self-start-up sub-threshold boost converter has been designed and implemented in a CMOS  $0.18 \ \mu m$  process. A bootstrap technique is incorporated between ring oscillator and phase generator to enhance the load drivability and rail to rail clock output swing of the clock generator. Consequently, novel cross clocks are generated from the clock generator, which reduces reverse currents in the charge pump. Body biasing has been used to reduce the switching loss and leakage current and also makes the design suitable for low voltage applications. Simulation results verify that better output voltage transient response, lower settling time and higher conversion efficiency can be achieved by the proposed circuit compared to conventional circuits.

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