Transmitter IQ Imbalance Mitigation and PA Linearization in Software Defined Radios

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Abstract. *Radio frequency (RF) power amplifiers (PA) are efficiently linearized by adaptive digital predistortion (DPD). However, performance of DPD is severely degraded in presence of transmitter's frequency-selective in-phase/quadrature (I/Q) imbalance. We propose the DPD/IQ method that compensates the effects of transmitter's I/Q imbalance and PA nonlinearity and is dedicated for implementation in low-cost software defined radio (SDR) cellular base stations. The advantage of DPD/IQ is low complexity in terms of reduced number of DPD coefficients which provides significant savings of FPGA resources. The performance of DPD/IQ has been evaluated after the method has been implemented in SDR board. Measured results clearly demonstrate efficient compensation of PA and transceiver impairments enabling transmission of wide bandwidth waveforms and realization of sophisticated modulation schemes. Improvement in image rejection ratio of 10–15 dB is achieved. Considering compensation of PA nonlinearities, the ACPR at PA output is decreased by 15 dBc.*

Keywords

Frequency dependent I/Q imbalance, digital predistortion, memory polynomial, power amplifier, PA linearization

1. Introduction

Nonlinearity and memory effects of radio frequency (RF) power amplifiers (PA) produce high out-of-band emissions and degrade bit error rate of transmitted signals. Popular solution to decrease distortions is to back off PA output power. This approach yields significantly lower PA power efficiency and substantial reduction in base station (BS) coverage. More acceptable approach is utilization of digital predistortion (DPD), based on complex valued memory polynomials (MP) [1], [2]. Other DPD approaches, such as the segmentation approach, consist of dividing the signal amplitude range into segments and applying a specific nonlinear function to each of them [3].

Modern modulation schemes exhibit high peak-to-average power ratio (PAPR), and when combined with nonlinear PA characteristics, they increase unwanted emissions at PA output [4]. Emissions can be reduced when DPD operation is supported by crest factor reduction (CFR) techniques [5]. RF transmitter imperfections degrade the symmetry between in-phase/quadrature (I/Q) modulator paths [6], [7], which not only deteriorates in-band signal characteristics but it is also detrimental to DPD operation [8]. In the case of the imperfect analogue-to-digital (A/D) converter systems, the signal quality improvement achieved by DPD is significantly degraded [9]. In order to fulfill strict Long Term Evolution (LTE) regulations, transceiver transmit paths, which already employ inevitable CFR and DPD, should implement some of I/Q imbalance (IQI) mitigation methods.

The paper presents a novel DPD/IQ method for combined RF transmitter IQI mitigation and PA linearization. It is particularly created for implementation in low-cost software defined radio (SDR) BS. The DPD/IQ advantage is low complexity in terms of reduced number of complex valued coefficients. Steps for efficient distortion mitigation are thoroughly described starting from mathematical model to complete realization in a SDR board which is incorporated in field-programmable radio frequency (FPRF) LTE BS. The results which are provided in the paper are obtained by measuring the transmitted BS signals. Adjacent channel power ratio (ACPR) and error vector magnitude (EVM) are used to assess the DPD/IQ performance.

The paper is organized as follows. Related work is given in the following section. In Sec. 3, the DPD/IQ method is described. In Sec. 4, the simulation setup is presented followed by simulation results. The measured results of DPD/IQ evaluation in SDR based BS are presented in Sec. 5. Section 6 is dedicated for discussion. The conclusion is drawn in the last section.

2. Related Work

Complex-valued signal $x(t)$, exposed to the source of frequency-independent I/Q imbalance, results to the signal $y(t)$ [10]:

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$$y(t) = \nu_1 x(t) + \nu_2 x^*(t), \tag{1}$$

$$\nu_1 = \cos\frac{\varphi}{2} + \mathrm{j}\,\varepsilon \sin\frac{\varphi}{2}, \tag{2}$$

$$\nu_2 = \varepsilon \cos\frac{\varphi}{2} - \mathrm{j}\sin\frac{\varphi}{2}.$$

The parameters ε and φ from (2) represent the amplitude and phase imbalance terms. The impact of static IQI on signal quality can be measured by image rejection ratio (IRR), defined as the ratio of the desired signal power and power of the image signal:

$$IRR = 20\log_{10}\left|\frac{\nu_1}{\nu_2}\right|. \tag{3}$$

For wideband signals, IQI manifests frequency-dependent behavior caused by analogue components in I and Q modulator paths [11]:

$$Y(f) = \mathrm{H}_1(f)X(f) + \mathrm{H}_2(f)X^*(-f), \tag{4}$$

where $X(f)$ and $Y(f)$ are the fast Fourier transforms (FFT) of $x(t)$ and $y(t)$ respectively. The complex-valued functions $H_1(f)$ and $H_2(f)$ depend on the gain and phase mismatches. In this case, IRR can be defined as [11]:

$$IRR = 20\log_{10}\left|\frac{H_1(f)}{H_2(f)}\right|. \tag{5}$$

Distortions related to IQI and PA nonlinearity can be minimized independently. The authors [12] propose a serial structure of two processing blocks, where the first block cancels PA nonlinearity and the second block is used for IQI mitigation. However, as reported in [13], this approach requires additional hardware in form of RF feedback loop to separately compensate different distortion sources. Simultaneous compensation is achieved in either time or frequency domain. Time domain techniques are presented in [13–15], while the frequency domain techniques are presented in [16], [17]. The Volterra-series DPD from [14] has shown an excellent performance in frequency-dependent IQI compensation, but it does not address PA nonlinearity. The joint digital pre-distortion presented in [18] compensates impairments of RF vector signal generators (VSG) including IQ imbalance, local oscillator (LO) leakage and power amplifier nonlinearities. The DPD employs a parallel structure consisting of non-conjugate and conjugate Parallel Hammerstein (PH) blocks. The method presented in [13] simultaneously suppresses PA and I/Q impairments of direct conversion radio transmitters. In [15] the frequency-dependent nonlinear I/Q impairments are modeled by nonlinear I/Q model, followed by a linear time invariant (LTI) system. The PA is represented by a LTI Wiener model, followed by a memoryless nonlinear model. The methods presented in [13], [15] have increased complexity compared to the methods in which distortion sources are separately compensated. The reason of increased complexity resides in uncompensated I/Q imbalance source, positioned in front of nonlinear PA, which requires extended DPD memory length [19].

The model presented in [20] employs of serial connection of a MP block, dedicated for PA nonlinearity mitigation and second block which removes the modulator's nonlinear IQI. The second block is formed as parallel connection of direct and conjugated value MPs. Ref. [21] proposes DPD Volterra model that compensates static IQI sources and PA impairments exciting a dynamic multiple-input multiple-output (MIMO) system.

It is worth mentioning that all methods found in literature are validated using laboratory test equipment. In test setups modulated waveforms are created by MATLAB software, then up-converted to RF by VSG. In our test setup VSG is not used. Instead, one of the novelties of this paper is that results are derived after the DPD/IQ has been implemented in SDR board which is a part of FPRF LTE BS.

3. DPD/IQ Method

The DPD/IQ adopts complex-valued MP models and indirect learning architecture (ILA) composed of predistorter and postdistorter blocks. We propose novel architecture in which predistorter and postdistorter blocks are divided into MP-based non-conjugate and linear conjugate sub-blocks, as presented in Fig. 1. The predistorter MP non-conjugate part (named with DPD in Fig. 1) takes at input signal $xd(n)$ and it is dedicated to minimization of PA and transmitter nonlinearity effects. Linear conjugate part, denoted as I/Q corrector in Fig. 1, takes at input the complex-conjugated signal $xd^*(t)$ and is introduced to suppress the effects of transmitter's I/Q imbalance. Compared to methods presented in [13], [18] the novelty of DPD/IQ resides in linearity of complex conjugate I/Q corrector block which is realized by FIR filter.

The DPD/IQ postdistorter output signal $y(n)$ is defined as:

$$y(n) = \sum_{i_1=0}^{N_1}\sum_{j_1=0}^{M_1} g_{i_1 j_1}\cdot x(n-i_1)\cdot e(n-i_1)^{j_1} + \sum_{i_2=0}^{N_2} h_{i_2}\cdot x^*(n-i_2). \tag{6}$$

The parameter N_1 in (6) represents the DPD memory length and M_1 is the nonlinearity order. I/Q corrector block is modeled by FIR filter with length N_2. Equation (6) is an extended version of MP model [1], [2].

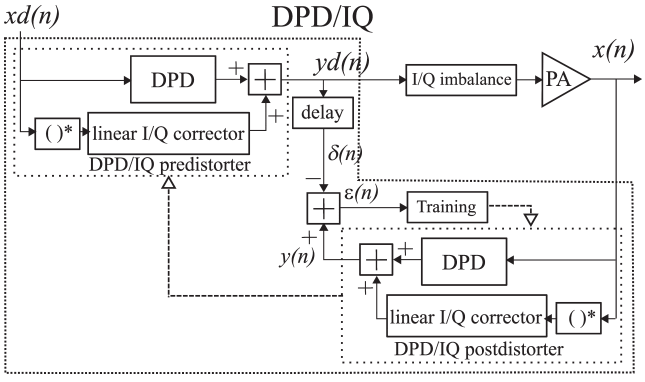

Fig. 1. ILA for I/Q image rejection and PA linearization.

The complex valued DPD/IQ coefficients from (6) are:

$$\begin{aligned} &g_{i_1 j_1} = a_{i_1 j_1} + \mathrm{j} b_{i_1 j_1}; \text{for } i_1 = 0,1,\ldots, N_1;\ j_1 = 0,1,...,M_1; \\ &h_{i_2} = c_{i_2} + \mathrm{j} d_{i_2}; \text{for } i_2 = 0,1,\ldots, N_2. \end{aligned} \tag{7}$$

The envelope signal $e(n)$ is defined by (8). Real and imaginary parts of the signal $x(n)$ are denoted with $x_\mathrm{I}(n)$ and $x_\mathrm{Q}(n)$:

$$e(n) = x_\mathrm{I}(n)^2 + x_\mathrm{Q}(n)^2. \tag{8}$$

The coefficients are determined using recursive least squares (RLS) algorithm which error function $\varepsilon(n)$ is defined by (9) [1]:

$$\varepsilon(n) = \sqrt{\left(\delta_\mathrm{I}(n) - y_\mathrm{I}(n)\right)^2 + \left(\delta_\mathrm{Q}(n) - y_\mathrm{Q}(n)\right)^2} \tag{9}$$

where $\delta_\mathrm{I}(n)$ and $\delta_\mathrm{Q}(n)$ are real and imaginary parts of delayed signal $\delta(n)$ used for compensation of digital loop delay. The signal $y(n)$ consists of real $y_\mathrm{I}(n)$ and imaginary $y_\mathrm{Q}(n)$ components. The RLS cost function $C(n)$ is defined as [2]:

$$C(n) = \sum_{m=0}^{n} \lambda^{n-m} \varepsilon(m)^2 \tag{10}$$

where λ is the RLS "forgetting factor". In order to minimize $C(n)$, the following system of linear equations is formed:

$$\frac{\partial C(n)}{\partial a_{i_1 j_1}} = 0;\ \frac{\partial C(n)}{\partial b_{i_1 j_1}} = 0;\frac{\partial C(n)}{\partial c_{i_2}} = 0;\ \frac{\partial C(n)}{\partial d_{i_2}} = 0. \tag{11}$$

In order to express (11) in a matrix form, the real and imaginary parts of DPD/IQ coefficients are stored in the vector $\mathbf{s}(n)$:

$$\begin{aligned} &\mathbf{s}(n) = \left[s_i\right] = \left[s_k \quad s_{k+K} \quad s_{l+2K} \quad s_{l+2K+L}\right]^\mathrm{T}_{2(K+L)} = \\ &\left[a_{i_1 j_1} \quad b_{i_1 j_1} \quad c_{i_2} \quad d_{i_2}\right]^\mathrm{T}_{2(K+L)} \\ &\text{for } k = i_1 + j_1 \cdot (N_1 + 1); l = i_2 \end{aligned} \tag{12}$$

where $K = (N_1 + 1)(M_1 + 1)$ and $L = (N_2 + 1)$. Delayed signals $\delta_\mathrm{I}(n)$ and $\delta_\mathrm{Q}(n)$ are stored in the vector $\boldsymbol{\delta}(n)$:

$$\begin{aligned} &\boldsymbol{\delta}(n) = \left[\delta_i\right]_{2(K+L)} = \\ &\left[\delta_0 \quad \delta_1 \quad \delta_2 \quad ... \quad \delta_{2(K+L)-1}\right]_{2(K+L)} = \\ &= \left[\delta_I(n) \quad \delta_Q(n) \quad 0 \quad ... \quad 0\right]_{2(K+L)}. \end{aligned} \tag{13}$$

The signals $x_\mathrm{I}(n)$ and $x_\mathrm{Q}(n)$ and their previous values are stored in matrices **Ie** and **Qe** given by (14).

$$\begin{aligned} &\mathbf{Ie} = \left[ie_{ij}\right]_{(N+1)\times(M_1+1)} = \\ &\left[x_\mathrm{I}(n-i)\cdot e(n-i)^j\right]_{(N+1)\times(M_1+1)}, \\ &\mathbf{Qe} = \left[qe_{ij}\right]_{(N+1)\times(M_1+1)} = \\ &\left[x_\mathrm{Q}(n-i)\cdot e(n-i)^j\right]_{(N+1)\times(M_1+1)} \\ &i = 0,1,...,N;\ \ j = 0,1,...,M_1 \end{aligned} \tag{14}$$

where the parameter N in (14) represents the maximum of N_1 and N_2.

The matrix $\mathbf{X}(n)$ is created from the elements of matrices **Ie** and **Qe**:

$$\begin{aligned} \mathbf{X}(n) &= \begin{bmatrix} x_{k,0} & x_{k,1} & 0 & ... & 0 \\ x_{k+K,0} & x_{k+K,1} & 0 & ... & 0 \\ x_{l+2K,0} & x_{l+2K,1} & 0 & ... & 0 \\ x_{l+2K+L,0} & x_{l+2K+L,1} & 0 & ... & 0 \end{bmatrix}_{[2(K+L)]^2} \\ &= \begin{bmatrix} ie_{i_1 j_1} & qe_{i_1 j_1} & 0 & ... & 0 \\ -qe_{i_1 j_1} & ie_{i_1 j_1} & 0 & ... & 0 \\ ie_{i_2 0} & -qe_{i_2 0} & 0 & ... & 0 \\ qe_{i_2 0} & ie_{i_2 0} & 0 & ... & 0 \end{bmatrix}_{[2(K+L)]^2}. \end{aligned} \tag{15}$$

Following RLS algorithm, after every training step, the elements of matrix $\mathbf{R}(n)$ and vector $\mathbf{r}(n)$ are calculated according to (16) and (17). The $\mathbf{R}(n)$ and $\mathbf{r}(n)$ have dimensions $2(K+L) \times 2(K+L)$ and $2(K+L) \times 1$, respectively. The system of equations in the matrix form is expressed by (18). The model coefficients, which are stored in $\mathbf{s}(n)$, are found by solving (18):

$$\mathbf{R}(n) = \lambda \mathbf{R}(n-1) + \mathbf{X}(n) \times \mathbf{X}(n)^\mathrm{T}, \tag{16}$$

$$\mathbf{r}(n) = \lambda \cdot \mathbf{r}(n-1) + \mathbf{X}(n) \times \boldsymbol{\delta}(n)^\mathrm{T}, \tag{17}$$

$$\mathbf{R}(n) \times \mathbf{s}(n) = \mathbf{r}(n). \tag{18}$$

4. The Simulation of DPD/IQ

The DPD/IQ has been simulated using mixed mode simulation library in which analogue and digital blocks are modeled in PSpice and SystemC, respectively. The diagram of simulation setup is given in Fig. 2. The DPD/IQ is modeled in SystemC and the model consists of predistorter and postdistorter parts. Beside DPD/IQ block, several modules are modeled in SystemC: the digital modulator, the CFR block, I/Q imbalance block, Inverse Sync filter, ADC and DAC. The transmitter operates in baseband (BB). In different test cases the ten-tone and 5MHz LTE low intermediate frequency (low-IF) waveforms are generated by digital modulator at rate of 61.44 MS/s.

The CFR is applied to reduce the PAPR of the signal at modulator output. The CFR module is based on Peak Windowing (PW) algorithm, which is described in details

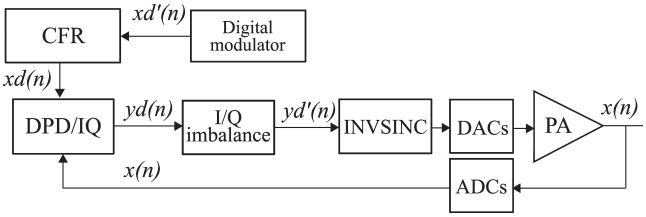

Fig. 2. Transmitter architecture block diagram, used for simulation of DPD/IQ.

in [23]. As the result of CFR employment, the PAPR of input waveforms is reduced to 8 dB. The model of DPD/IQ block is designed based on the equations described in Sec. 3. The DPD/IQ postdistorter implements (6). The non-conjugate MP part is simulated with memory length of $N_1 = 4$ and nonlinearity order $M_1 = 2$. The I/Q corrector length is $N_2 = 4$. In every training step postdistorter block calculates new elements of matrices $\mathbf{R}(n)$ and $\mathbf{r}(n)$ according to (16) and (17), respectively. The system of linear equations, expressed by (18), is solved by LU decomposition method. The result is the vector $\mathbf{s}(n)$ which contains new DPD/IQ coefficients. After signal is processed by CFR and pre-distorter, the IQI is inserted into signals. For this purpose, two IQI sources have been created which are described in the following subsections. The digital to analogue conversion (DAC) roll-off is compensated by Inverse SINC filter. For PA, we used different models – the memory polynomial model and the Hammerstein model. The Hammerstein model is derived as memory-less nonlinearity modeled in SystemC, followed by analogue 7th order ladder LC Pi filter. The filter is designed with 30 MHz cut-off frequency, in-band amplitude ripple less than 0.1 dB and the stop band attenuation greater than 90 dB. The LC filter is the only analogue circuit in simulation setup; the other circuits are described as digital blocks. In simulations the arithmetical precision of 18 bits is adopted and the number of points for FFT is set to 2^{16}. The results presented in the following subsections correspond to the Hammerstein PA model. The simulations proved efficiency of DPD/IQ in image rejection as it is documented in the following test cases.

4.1 Case 1: I/Q Imbalance Model Realized of IIR Filters and Ten-tone Input Waveform

In the test case 1 positive-band ten-tone signal is applied in which the frequencies of tones range from 1 to 10 MHz. The IQI source is modeled by third-order low-pass infinite impulse response (IIR) filters processing separately I and Q components. The filters have Butterworth transfer characteristic. The filter processing I component has 10 MHz cut-off frequency; the cut-off frequency of the filter applied for Q component processing is 9.7 MHz. Gain imbalance of 3% and a phase imbalance of around 3° are introduced at 10.0 MHz.

Figure 3 depicts the power spectral densities of DPD/IQ input $xd(n)$ and the IQI source output $yd'(n)$ when DPD/IQ is bypassed.

Spectral components of PA output signal are depicted in Fig. 4 in cases when DPD/IQ block is bypassed and when DPD/IQ is applied. Results which are presented in Figs. 3 and 4 correspond to the 14-bit ADC/DAC resolution.

In further simulations the impact of ADC/DAC resolution on DPD/IQ performance is analyzed. The resolution, denoted with parameter R, is changed from $R = 10$ to $R = 18$, with a step of $\Delta R = 2$. The amplitudes of tones at negative frequencies are determined and IRR values calculated. The IRR results, derived with or without DPD/IQ, are presented in Fig. 5. When DPD/IQ is not used, IQI distortions reflect to IRR value of approximately 30 dB. When DPD/IQ is utilized, the IRR is improved to 60 dB. Frequency images are efficiently suppressed if R is greater than or equal to 12.

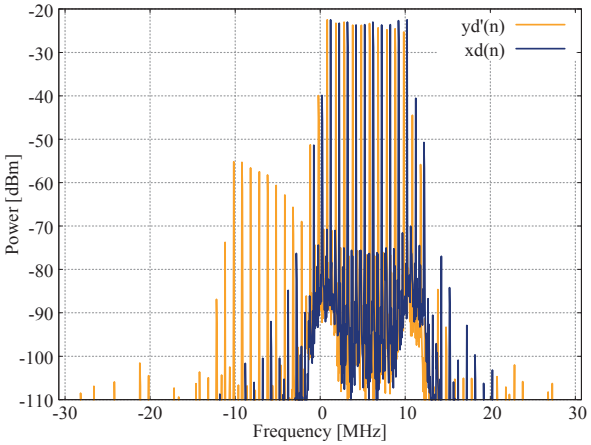

Fig. 3. Spectra of $xd(n)$ and $yd'(n)$ when DPD/IQ is bypassed.

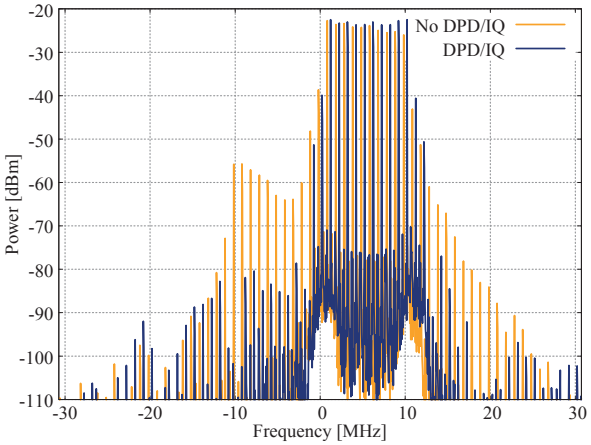

Fig. 4. Spectra of PA output signals when DPD/IQ is bypassed and when DPD/IQ is utilized.

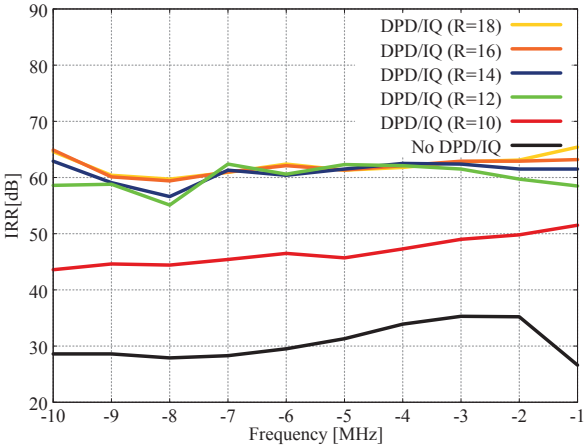

Fig. 5. IRR obtained at negative frequencies for different ADC/DAC resolution values R.

4.2 Case 2: I/Q Imbalance Model Based on Measured Transceiver Characteristics

In the test case 2, the ten-tone waveform is used. The IQI source model has been created based on data obtained from calibration process of a SDR transceiver chip.

The chip is first tuned to operate at central frequency of 3.5 GHz [22]. Then, I/Q gain and phase correction values are determined at BB frequencies in the range from –30 MHz to 30 MHz, with a step of 5 MHz. After that, gain and phase imbalance values are calculated and used as input parameters of IQI model, developed on the bases of (4). The gain and phase imbalance terms manifest frequency dependent behavior (Fig. 6). Spectral densities of signals $xd(n)$ and $yd'(n)$ are depicted in Fig. 7 in the case when DPD/IQ is bypassed.

Figure 8 presents power spectral densities of the PA output signal without DPD/IQ and with DPD/IQ.

The simulation is repeated for different ADC/DAC resolution values. The IRR, as a function of BB frequency and value R, is given in Fig. 9. When DPD/IQ is not applied, the IRR is deteriorated as a result of incomplete suppression of the image frequency and it is approximately

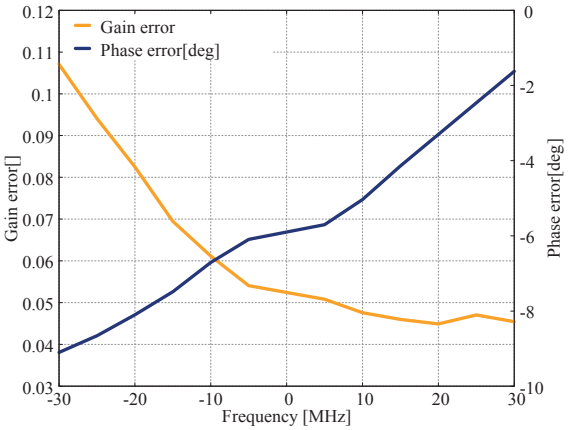

Fig. 6. Gain and phase imbalance of a transceiver chip as a function of BB frequency.

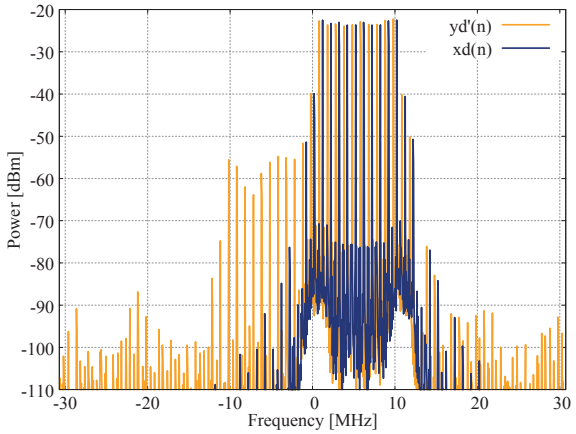

Fig. 7. The spectra of $xd(n)$ and $yd'(n)$ in case when DPD/IQ is bypassed.

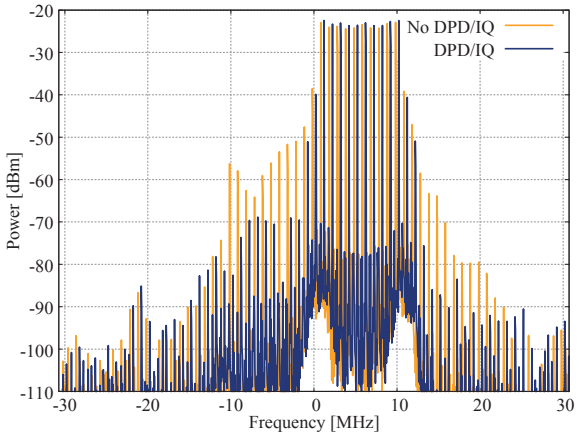

Fig. 8. The PA output spectra in cases with and without DPD/IQ.

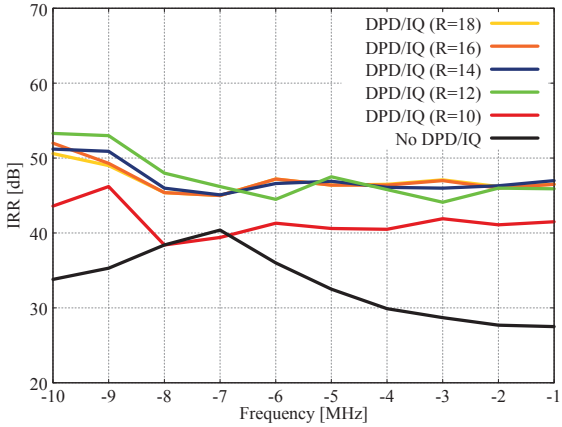

Fig. 9. IRR at negative frequencies for different ADC/DAC resolutions. The used waveform is ten-tone.

equal to 35 dB. The utilization of DPD/IQ improves the IRR by approximately 15 dB. The resulting IRR reaches 50 dB.

4.3 Case 3: I/Q Imbalance Model Based on Measured Transceiver Characteristics and 5MHz Low-IF Input Waveform

In test case 3 the 5 MHz LTE low-IF waveform is applied. The same IQI model is used as it is used in the test case 2. Power spectral densities of $xd(n)$ and $yd'(n)$ are depicted in Fig. 10 in the case when DPD/IQ is not applied.

Figure 11 depicts $x(n)$ spectra with and without DPD/IQ usage. In the case of uncompensated PA, the ACPR values for lower and upper adjacent channels are –30.67 dBc and –39.22 dBc, respectively. When ADC/DAC resolution is R = 12, DPD/IQ achieves –53.5 dBc and –58.27 dBc.

Further simulations are conducted to assess the impact of ADC/DAC resolution on DPD/IQ performance. The ACPR values, obtained for PA output signal and different R values are given in Tab. 1. The adjacent and alternate channels are obtained at offsets of 5 MHz and 10 MHz from the central baseband frequency of 2.5 MHz. Results

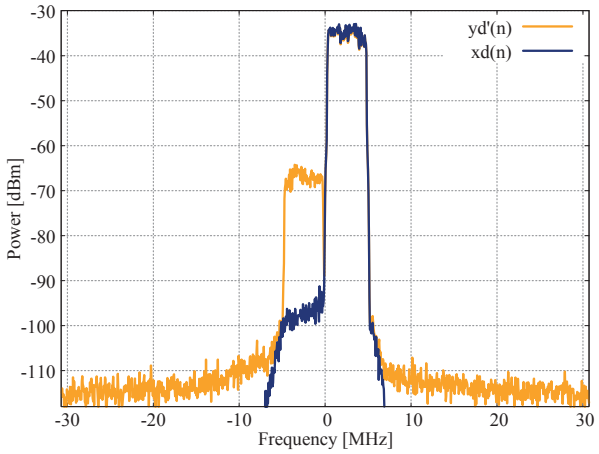

Fig. 10. *xd*(*n*) and *yd'*(*n*) spectra in the case when DPD/IQ is not applied.

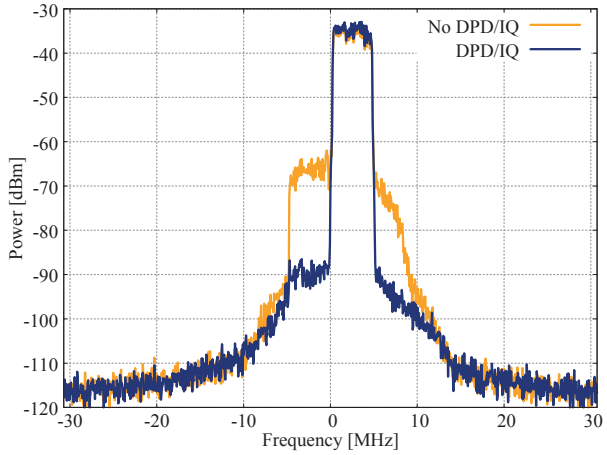

Fig. 11. The spectra of PA output when DPD/IQ block is bypassed and in the case when DPD/IQ is applied.

	ADC/DAC resolution *R*	ACPR [dBc]			
		Lower alternate	Lower adjacent	Upper adjacent	Upper alternate
DPD off	14	–62.18	–30.67	–39.22	–65.87
DPD/IQ on	10	–47.37	–48.37	–51.03	–51.91
	12	–59.07	–53.53	–58.27	–63.39
	14	–66.47	–54.74	–59.3	–69.2
	16	–67.74	–54.94	–59.45	–70.55
	18	–67.8	–54.97	–59.49	–70.77

Tab. 1. The ACPR values in case of 5 MHz low-IF LTE waveform for different DAC/ADC resolutions.

confirm that the distortions are efficiently reduced if ADC/DAC resolution is greater than or equal to 12 bits.

5. The Implementation in SDR Board

The measurement setup consists of BS, Spectrum Analyzer and Windows based PC which is running Vector Signal Analyzer (VSA) software for modulation analyses. The BS consists of a Linux based PC, equipped by SDR board [22] and PAs. The SDR board is inserted in peripheral component interconnect express (PCIe) slot of the PC. The BB digital modem is implemented by Linux PC software. It generates waveforms at rate of 30.72 MS/s and sends them to the SDR board through PCIe.

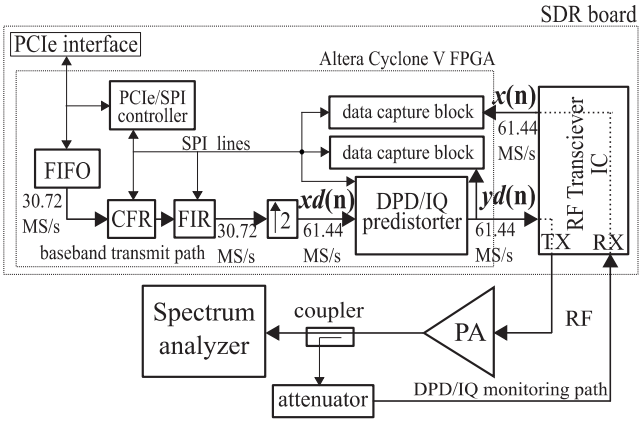

Fig. 12. The block diagram of one transmit path used for the realization of DPD/IQ.

The DPD/IQ is implemented in SDR board which incorporates two transceiver ICs and an Altera Cyclone V FPGA chip [22]. The 12-bit DACs and ADCs are incorporated in transceiver ICs. Frequency conversion from BB to RF is performed by transmitter chains. Down conversion from RF to BB is implemented by receive chains. BS performs 2×2 MIMO operations. Only components which belong to one transmit path are shown in Fig. 12. The transmit path consists of CFR, FIR, interpolation block and DPD/IQ predistorter blocks. The CFR is based on Peak Windowing technique and it is described in details in [23]. Additional FIR filter is used to eliminate spectrum regrowth produced by BB modem and CFR [23].

The CFR and FIR have provision for Serial Peripheral Interface (SPI) in order to change their configuration. The PCIe/SPI controller provides the connection between PCIe and SPI ports of these digital circuits (Fig. 12). The DPD/IQ predistorter has parameters $N_1 = N_2 = N = 4$, $M_1 = 2$. An oversampling of factor one is used before predistorter block, yielding a data rate of 61.44 MS/s. The data rate is constrained by maximum data throughput at the interface between FPGA and transceiver IC which is equal to 61.44 MS/s.

Predistorter operations can be divided into two parts. In the first part, delayed versions of the signals $xd_I(n)$ and $xd_Q(n)$, which represent the I and Q components of predistorter input signal, are multiplied with envelope $ed(n)$. The envelope is determined as a sum of squares of $xd_I(n)$ and $xd_Q(n)$. Obtained values are stored in the matrices **ID** and **QD** which have dimension $(N + 1) \times (M_1 + 1)$ (19):

$$\mathbf{ID} = \left[id_{ij} \right] = \left[xd_1(n-i) \cdot ed(n-i)^j \right],$$
$$\mathbf{QD} = \left[qd_{ij} \right] = \left[xd_Q(n-i) \cdot ed(n-i)^j \right]. \quad (19)$$

The part of predistorter circuit, which takes at its inputs $xd_I(n)$ and $xd_Q(n)$ and calculates the elements of matrices **ID** and **QD**, is given in Fig. 13. The number of 18×18bit multipliers, utilized by this structure, is $2(M_1 + 1)$.

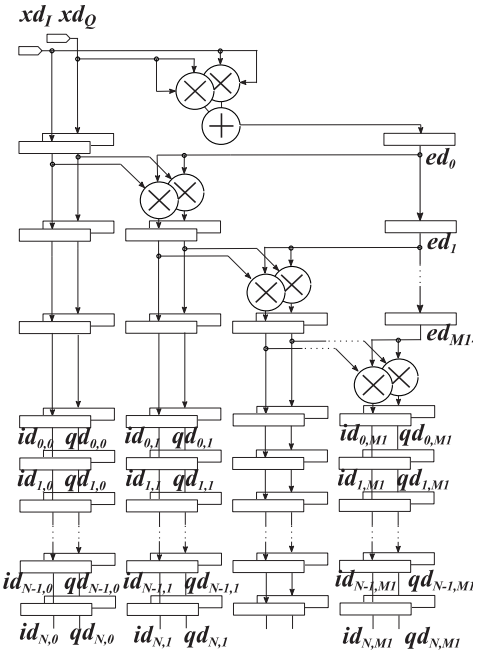

Fig. 13. The part of DPD/IQ architecture which calculates elements of matrices **ID** and **QD.**

The circuit operates at clock frequency which is equal to data processing rate of 61.44 MS/s. The rest of predistorter circuit calculates the predistorter output signals yd_{I} and yd_{Q} according to (20–21). The complex valued coefficients (7) are shared between the predistorter and postdistorter. The real and imaginary parts of complex-valued coefficients, denoted with a_{ij}, b_{ij}, c_i and d_i in (7), are used in (20–21):

$$yd_{\mathrm{I}} = \sum_{i=0}^{N}\left(c_i \cdot id_{i0} + d_i \cdot qd_{i0} + \sum_{j=0}^{M_1}\left(a_{ij} \cdot id_{ij} - b_{ij} \cdot qd_{ij} \right) \right), \quad (20)$$

$$yd_{\mathrm{Q}} = \sum_{i=0}^{N}\left(d_i \cdot id_{i0} - c_i \cdot qd_{i0} + \sum_{j=0}^{M_1}\left(a_{ij} \cdot qd_{ij} + b_{ij} \cdot id_{ij} \right) \right). \quad (21)$$

The number of multiplication operations in (20–21) is $4(N_1+1)\times(M_1+2)$. The operations in (20–21) use 18-bit arithmetic precision and they are optimized by multiplexing input data. The circuit operates at clock frequency of 122.88 MHz which is two times greater than the data processing rate. The number of multipliers is reduced two times compared to the number of multiplication operations and it is equal to $2(N_1+1)\times(M_1+2)$. The total number of multipliers used for implementation of DPD/IQ predistorter is equal to $2(N_1+1)\times(M_1+2)+2(M_1+1)$.

The predistorted signal is converted into an analogue signal by transceiver IC DAC and it is up-converted to RF. Frequency down conversion from RF to BB is implemented by IC receive chain, which is allocated as DPD/IQ monitoring path in Fig. 12. Table 2 gives the information about FPGA resources occupied by digital blocks which belong to one transmit path.

The software application is developed in C/C++ which runs on CPU core and completes several functions. First, it is used for transceiver IC calibration and control.

Resources	Adaptive logic module	Adaptive look-up tables	Dedicated logic registers	DSP block	Block memory bits
CFR	2322	2445	3947	14	3401
Post-CFR FIR	1519	1546	2768	10	1920
Interpolation block	1083	1745	1887	0	240
DPD/IQ predistorter	3817	3180	7560	46	0

Tab. 2. The utilized Altera Cyclone V FPGA resources.

Then, it implements graphical display presenting important DPD/IQ signals. Finally, the postdistorter operations are executed by the same application. Beside the predistorter, additional circuits are created in FPGA to support the training process. The circuits include data capture RAM blocks which store I/Q samples of two signals: the $yd(n)$, which is obtained at the output of predistorter block, and the $x(n)$ which is obtained at the output of monitoring path (depicted in Fig. 12). Data streams of signals $x(n)$ and $yd(n)$ consist of 16384 consecutive I/Q samples. Data is periodically read from capture blocks and sent from FPGA to PC. Based on information received from SDR board, software application calculates new coefficients. Specifically, the application executes the operations given by (16) and (17). In every training step, new elements of matrices $\mathbf{R}(n)$ and $\mathbf{r}(n)$ are calculated and the system of linear equations, given by (18), is solved. The result is the vector $\mathbf{s}(n)$ which contains new DPD/IQ coefficients. At the end of each training cycle, the coefficients are sent to FPGA over PCIe/SPI and programmed into the registers dedicated to predistorter coefficients. The PA and I/Q imbalance impairments change slowly with temperature drift and component aging. Additionally, the number of mathematical operations is reduced because of reduced coefficients set. The postdistorter operations are realized as low-priority background tasks, which are repeated after time interval of several seconds.

In the measurements the transceiver IC central frequency is tuned to LTE Band 13 frequency of 751 MHz. Moderate output power broadband PA is used [24]. The PA supply voltage is intentionally decreased from nominal 5 V to 3.6 V, reducing the PA 1 dB compression point to 6 dBm. In the measurements, static I/Q calibration procedure of the transceiver IC is intentionally bypassed in order to assess the DPD/IQ performance in the presence of static I/Q imbalance. The PA output is over coupler and attenuator circuits fed to the transceiver receive input for the realization of DPD/IQ monitoring path.

5.1 Test Case 1: The 10 MHz and 20 MHz LTE Test Model 3.1

In the test case 1 the 10 MHz and 20 MHz E-TM 3.1 LTE are applied. The PAPR of original waveforms are 10.6 dB and 10.4 dB, respectively.

When CFR is employed, the PAPR is reduced down to 8 dB, creating EVM of 2%. After the linearization process

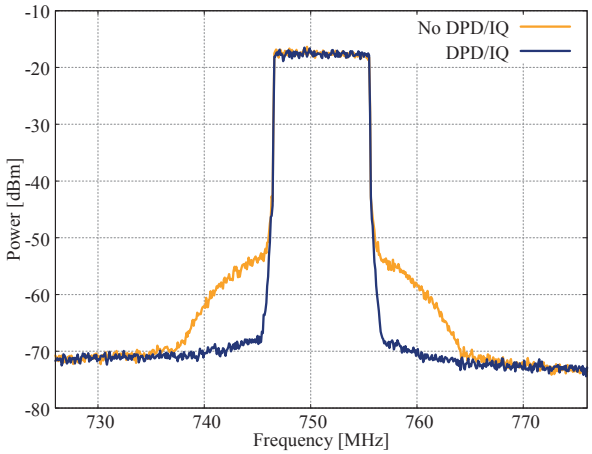

Fig. 14. The spectra of PA output signals when 10 MHz LTE Test Model 3.1 is applied. Signals are obtained in cases with and without using the DPD/IQ.

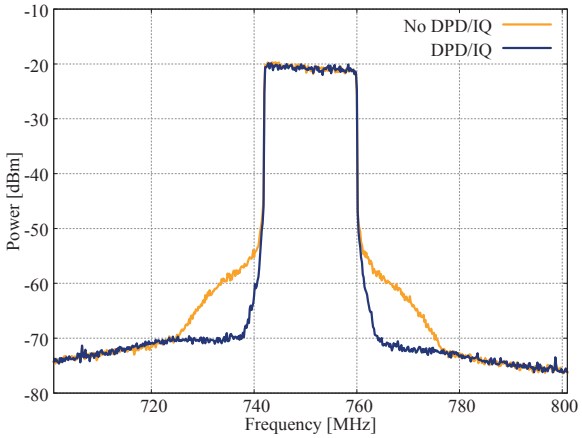

Fig. 15. The spectra of PA output signals when 20 MHz LTE Test Model 3.1 is applied. Signals are obtained in cases with and without using the DPD/IQ.

	10 MHz LTE		20 MHz LTE	
	No DPD	**DPD/IQ**	**No DPD**	**DPD/IQ**
Channel power [dBm]	6.79	6.72	6.73	6.74
ACPR [dBc]	–40.4	–51.8	–39.7	–48.6
EVM [%]	3.2	2.2	3.6	2.2
PAPR [dB]	10.32	8.3	10.6	8.3

Tab. 3. The measured ACPR, EVM and PAPR for 10 MHz and 20 MHz LTE signals.

is done, the PA output power is preserved at the same level of P_out = 6.7 dBm as before any DPD/IQ processing is performed. The comparison of spectra of PA output signal, in cases with and without DPD/IQ, is given in Figs. 14 and 15 for 10 MHz and 20 MHz E-TM 3.1 LTE waveforms, respectively. The results in terms of ACPR, EVM and PAPR are given in Tab. 3.

5.2 Test Case 2: Asymmetrical Ten-tone Signal

In order to evaluate the performance of DPD/IQ in IQI mitigation, asymmetrical positive-band ten-tone input

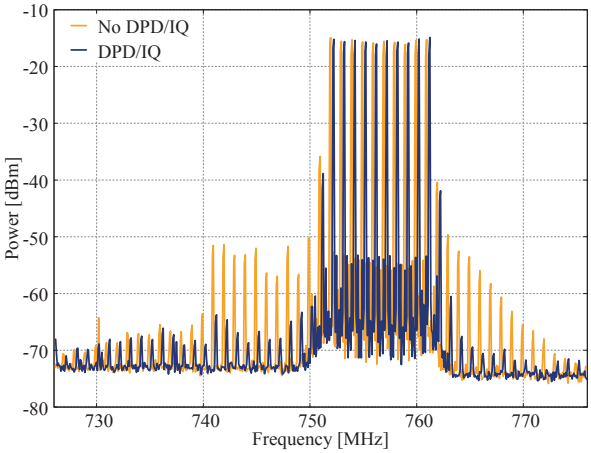

Fig. 16. The spectra of signals obtained at PA output when ten-tone is applied.

f [MHz]		–10	–9	–8	–7	–6
IRR[dB]	**DPD off**	37.2	37.1	38.3	38.5	37.6
	DPD/IQ on	48.9	50.4	52	52.8	51.6
f [MHz]		–5	–4	–3	–2	–1
IRR[dB]	**DPD off**	41.3	42	37.5	41.4	37
	DPD/IQ on	52.6	53.5	49.8	48.5	47.8

Tab. 4. IRR at negative frequencies for ten-tone waveform.

waveform is used. The output power of ten tone test signal is equal to 3.5 dBm. The input waveform is modified by CFR block. The PAPR of the waveform is decreased by 2 dB. Figure 16 illustrates the results of DPD/IQ operation by showing power spectral densities of PA output with and without using DPD/IQ. The IRR values, measured at negative BB frequencies, are given in Tab. 4. After DPD/IQ is employed, the IRR is increased to 50 dB.

5.3 Test Case 3: The 5 MHz LTE Low-IF Signal

In test case 3 the 5 MHz LTE low-IF is used. The power spectral densities of PA output signals are given in Fig. 17. Three cases are considered: when DPD is bypassed,

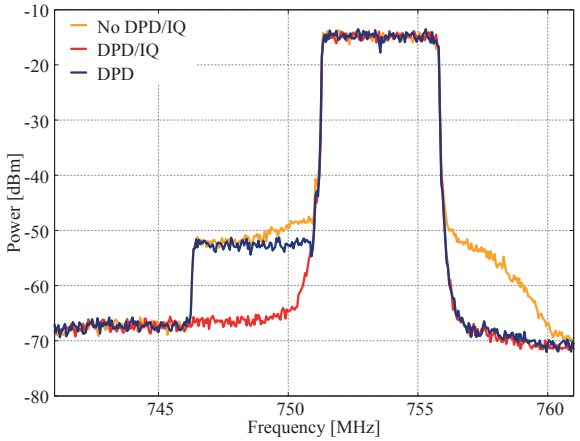

Fig. 17. Spectra of signals obtained at PA output when 5 MHz low-IF LTE waveforms is applied.

Condition	Main channel power [dBm]	Lower adjacent ACPR [dBc]	Upper adjacent ACPR [dBc]
No DPD	6.46	–36.38	–42.11
DPD [23]	6.5	–37.57	–54.76
Proposed DPD/IQ	6.45	–50.92	–54.44

Tab. 5. The ACPR in case when 5 MHz low-IF LTE waveform is transmitted.

when DPD is used without I/Q corrector (the model is described in [23]), and in the third case, when DPD with I/Q corrector is applied. When DPD is used without I/Q corrector, PA output exhibits strong IQI images. The utilization of DPD/IQ gives very good suppression of IQI images. The ACPR results are given in Tab. 5. In lower adjacent channel DPD/IQ reduces the ACPR by 14.5 dBc. In upper adjacent channel the ACPR is reduced by 12.2 dBc. The main channel power is preserved at the same level as before DPD/IQ is applied.

6. Discussion

The DPD/IQ provides low complexity in terms of reduced number of complex-valued coefficients. This is accomplished by several methods, first, by choosing even order terms only form for the envelope function realization (8). Discrimination of even order terms speeds up the execution of postdistorter operations by eight times as compared to the speed of the full MP [25]. Despite reduced number of coefficients, the odd order only MP model achieves similar linearization performance as a full order MP [25].

The proposed model is similar to the one proposed by Refs. [13], [18]. References [13], [18] present functions which are optimized to ensure orthogonality; the present work uses more conventional MP basis function. Another difference is in complex conjugated DPD/IQ part, which in Refs. [13], [18] is realized by nonlinear PH models, while in the proposed model it is implemented by linear FIR. In DPD/IQ, the nonlinearities of the PA and I/Q modulator are compensated by non-conjugate DPD block, defined by MP parameters $M_1 = 2$ and $N_1 = 4$ (6). Linear I/Q corrector, implemented as a FIR filter, is applied specifically for IQI mitigation. The utilization of FIR block for I/Q corrector additionally reduces the number of complex valued coefficients. Besides, the realization in FPGA is simplified by choosing the FIR length N_2 to be equal to the memory length N_1. The number of complex-valued coefficients is $(N_1 + 1)\times(M_1 + 2) = 20$. For comparison, the numbers of complex valued coefficients of the models presented in [20] and [13] are 34 and 41, respectively. Decreased number of coefficients enables savings of FPGA resources, which makes DPD/IQ more suitable for realization in SDR FPGA than methods presented in [13], [18]. It is worth mentioning that beside predistorter, the other digital blocks are also required in transmitter paths, such as CFR and post-CFR FIR filters. For implementation of these digital blocks significant amount of FPGA resources is also required [23].

Simulation and measurement results demonstrate DPD/IQ capability of efficient PA linearization without sacrificing PA output power. The DPD/IQ, supported by CFR, enables efficient operation in the region near PA 1 dB compression point. As the result of CFR employment, the PAPR of LTE waveforms is reduced to 8 dB. In cases of LTE test model 3.1 10 MHz and 20 MHz, in-band signal distortion is created and EVM is increased to 2%. The advantage of DPD/IQ utilization is that transceiver's static I/Q calibration procedure is not required and can be omitted.

In simulations we analyzed the impact of ADC/DAC resolution on DPD/IQ performance. The resolution value $R = 12$ has been adopted because it yields the IRR greater or equal than 50 dB. As a consequence of this, the SDR board is chosen with 12-bit internal ADCs and DACs [22]. As far as IQI is concerned, the challenging test cases were those that apply 5 MHz LTE low-IF and ten-tone waveforms. In different test cases the IQI effects are observed and analyzed for negative image frequencies. Also, the method gives satisfactory results if IQI is present at positive frequencies. The measurement results, which are presented in Tab. 4, confirm the accuracy of the simulation results, which are given in Fig. 9. When asymmetrical ten-tone signal is used as input waveform, the DPD/IQ achieves the IRR value that is equal to 50 dB (Tab. 4). The output of uncompensated PA contains significant IQI images (Fig. 17). The amount of IQI increases with transmitter's LO frequency (Fig. 6) [22]. The MP DPD from [23] can compensate PA nonlinearity but cannot be used for IQI mitigation (Fig. 17). The linearization is achieved by DPD/IQ, which effectively reduces the PA nonlinearity, memory and IQI effects. In case of 5 MHz LTE low-IF waveform, the ACPR of PA output signal is decreased by 14.5 dBc. The obtained results are comparable with the results found in [13], [15]. The PA/IQ PD method from [13] yields 15–20 dBc improvement in ACPR compared to the uncompensated case. In [16] the compensation of I/Q imbalance improves the IRR over 45 dB. When ten-tone waveform is applied, the DPD yields increase in IRR by 10–15 dB [16].

Model		Ref. [13]	Ref. [27]	Ref. [28]	Proposed
Memory order		3	3	3	4
Nonlinearity order		9	9	9	7
Number of complex-valued coefficients		80	184	212	25
Waveform bandwidth [MHz]		50			10
Sample rate [MS/s]		400			61.44
Modulated P_out [dBm]		43			28
ACPR [dBc]	**DPD off**	–34.54			–34
	DPD on	–52.40	–52.81	–53.76	–49.0

Tab. 6. Performance comparison of different methods.

The DPD/IQ has been used for linearization of PAs with advanced architecture [26] and power added efficiency of 35%. In this case the broadband PA [24] is used as pre-driver. However, the DPD/IQ nonlinearity order is increased to efficiently compensate PA nonlinearities. DPD/IQ is employed with parameters $N_1 = 4$ and $M_1 = 3$. Because the even order terms form is chosen for the envelope realization, $M_1 = 3$ corresponds to full MP nonlinearity order equal to value of 7. The number of complex valued coefficients is increased to 25 and the number of 18×18 multipliers is 58. For input waveform LTE 10 MHz Test model 3.1, central frequency of 2140 MHz and selected PAPR value equal to 8 dB, the ACPR of PA output signal is reduced from starting point of –34 dBc down to –49 dBc. The output power is preserved at the same level of 28 dBm as before DPD/IQ was applied. The PAPR is reduced down to 8 dB and EVM is equal to 2%. The following methods for the joint compensation of I/Q imbalance and PA nonlinearity are found in literature and used for comparison with the proposed method: the PA/IQ PD model [13], the conjugated generalized MP model [27] and the three-input nonlinear model from [28]. The results for these methods, given in Tab. 6, are taken from [28].

When comparing the obtained results with the results from literature test-bed conditions cannot be neglected, such as the number of bits of the waveforms, the DPD/IQ data rate and DAC/ADC resolution. In the literature the results are obtained using laboratory equipment that relies on high-performance VSG and where all pre-distorter operations are realized by MATLAB software. The methods which results are given in Tab. 6 have much larger complexity in terms of number of coefficients, and therefore, are not adapted for use in FPGA. In our case, performance of DPD/IQ is assessed after it is implemented in low-cost SDR board which is part of RF BS. The resolutions of waveforms and ADC/DACs, located in transceiver IC, are limited to 12 bits. Also, the DPD/IQ data rate is 61.44 MS/s.

7. Conclusion

In this paper the effects of I/Q imbalance and PA nonlinearity in wireless transmitters is considered. The low complexity method is proposed for impairments mitigation. The DPD/IQ yields linearization results comparable to conventional DPD solutions while reducing the number of complex-valued coefficients. The IQI images are suppressed almost down to the noise floor without sacrificing the PA output power. Low complexity feature enables implementation in SDR boards which are suitable for realization of low-cost LTE base stations. The results which are presented in the paper are obtained after the predistorter has been implemented in a SDR-based BS. The DPD/IQ performance was analyzed using LTE type of waveforms and multi-tone signals. In case of 5 MHz LTE low-IF the ACPR is improved for 15 dBc; in case of ten-tone waveform the IRR improvement of 10–15 dB is achieved. When 10 MHz and 20 MHz LTE signals are transmitted, the improvement in ACPR is greater than 15 dBc. The development of a method that jointly compensates I/Q impairments, PA nonlinearity and crosstalk effects which appear in multi-branch and multi-frequency MIMO wireless transmitters is envisaged for future work.

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