# Low Voltage High Performance CMOS Current Mode Four-Quadrant Analog Multiplier Circuit

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**Abstract.** *This paper describes a new CMOS current-mode four-quadrant analog multiplier circuit. The proposed design is based on a high performance squarer cell, whose main core is realized by the up–down topology trans-linear loop using flipped voltage followers (FVF).*

*The simulation results are verified by TSPICE simulator based on the BSIM3v3 transistor model for TSMC 0.18 µm CMOS process available from level 49 MOSIS at 25°C with ±0.75 V supply voltage. The proposed multiplier offers improved characteristics compared to the multipliers previously exposed in the literature. It has a wide dynamic range. The total harmonic distortion is about 0.42% at 100 kHz with peak-to-peak input current of 40 µA. The −3 dB bandwidth is more than 850 MHz and maximum power consumption is of approximately 105 µW.*

## Keywords

Multiplier, four-quadrant, CMOS, current-mode, trans-linear loop, low voltage

## 1.    Introduction

Signal processing circuits are present in all the equipment used in our life, such as telecommunications, television, transport or medical equipment [1–4]. The analog approach of these circuits is highly recommended in the manufacturing sector due to their low power and high-speed operation, allowing real-time signal processing.

Analog multiplier circuit is a block widely used in analog signal processing systems, for example in adaptive filters, modulators, automatic gain control, image processing, artificial neural networks, fuzzy integrated systems , squaring and square rooting of signals [5–8]. It usually has two input ports and one output port. Under ideal conditions, the output of this circuit $Z$ is defined as the linear product of two input signals $X$ and $Y$, which translates to $Z = K \, X \, Y$, where $K$ is a constant with an appropriate dimension [9].

Current mode multipliers have received considerable attention due to their good characteristics of dynamic range, accuracy, bandwidth, power consumption [10–12]. For this reason, many researches have been carried out with the aim of improving their performance using different techniques. The first group of circuits was made based on the trans-linear principle (TL) using loop transistors operating either in weak inversion [13], [14] or in strong inversion [15], [16]. The second group deals with the structure based on active circuits such as Current Conveyor (CC) [17–19], Operational Amplifier (OA) [20], Operational Trans-conductance Amplifier (OTA) [5], [21] and voltage differencing gain amplifier (VDGA) [22].

This paper presents a new CMOS current-mode four-quadrant multiplier circuit. It is implemented by using two squarer circuits. The circuit is simulated using TSPICE simulator by level 49 parameters (BSIM3v3) in 0.18 µm standard CMOS technology with ± 0.75 V supply voltage. The simulation results present ± 20 µA dynamic range with THD less than 0.8% at 1 MHz, 850 MHz bandwidth and a maximum power consumption about 0.105 mW.

## 2.    Circuit Description

### 2.1  Proposed Current Mode Squarer Circuit

The proposed CMOS current-mode squarer circuit is shown in Fig. 1. The main core of this circuit consists of up–down topology trans-linear loop formed by four NMOS transistors (M1, M2, M3, and M4). The transistors (M1, M5) and (M2, M6) formed flipped voltage followers (FVF) which keep the voltage of sources of transistors M1 and M2 constant regardless of the input and output currents.

Consequently, the path formed by the transistors M5 and M12 limits the minimum supply voltage of circuit.

$$\left(V_{\text{DD}} - V_{\text{SS}}\right)_{\text{min}} = V_{\text{GS5}_{\text{min}}} + V_{\text{SG12}_{\text{min}}} + V_{\text{TH}} \qquad (1)$$

where $V_{\text{GS}}$ is the gate-source voltage, $V_{\text{DD}}$ is the positive voltage supply, $V_{\text{SS}}$ is the negative voltage supply and $V_{\text{TH}}$ is the threshold voltage of transistor.
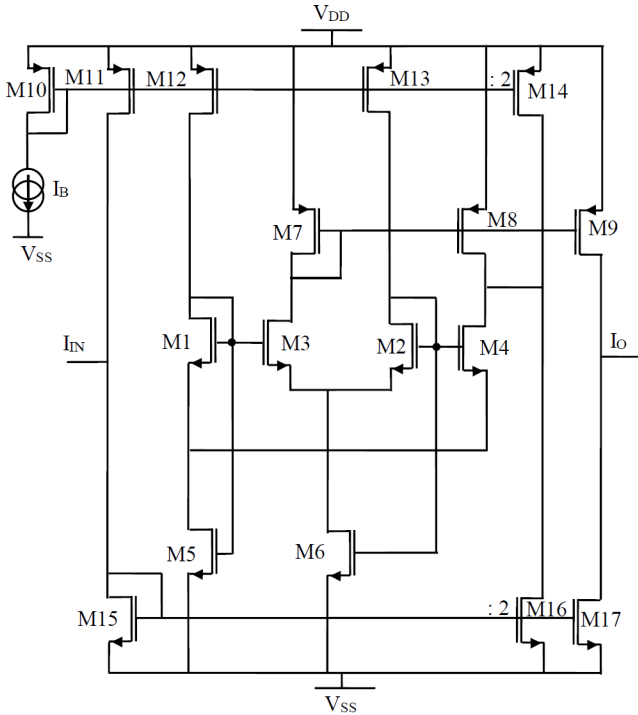
**Fig. 1.** Proposed current squaring circuit.

Since all transistors operate in the saturation region $V_{DS} \geq V_{GS} - V_{TH}$, the drain-source current equation can be expressed as:

$$I_{DS} = \frac{k_n}{2} \frac{\left(V_{GS} - V_{TH}\right)^2}{1 + \theta\left(V_{GS} - V_{TH}\right)} \qquad (2)$$

where $k_n = \mu_{n0} C_{ox} W/L$ is the trans-conductance parameter, $C_{ox}$ is the oxide gate capacitance in unit area, $\mu_{n0}$ is the low field mobility, $W/L$ is the ratio of width to length and $\theta$ is the mobility attenuation factor.

If the mobility attenuation factor is not taken into account, the drain-source current expression of transistor becomes:

$$I_{DS} = \frac{k_n}{2}\left(V_{GS} - V_{TH}\right)^2 . \qquad (3)$$

From (3), the gate-source voltage $V_{GS}$ expression can be written as:

$$V_{GS} = V_{TH} + \sqrt{2\frac{I_{DS}}{k_n}} . \qquad (4)$$

Applying Kirchhoff's voltage law (KVL), the relationship between the gate-source voltages of trans-linear loop is given by:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} . \qquad (5)$$

Assuming that all transistors have the same trans-conductance value, the following expression is given using (4) and (5).

$$\sqrt{I_{DS1}} + \sqrt{I_{DS2}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} . \qquad (6)$$

Given that the drain-source currents of transistors M1 and M2 are traversed by the bias current $I_B$ and the drain-source currents of transistors M14 and M16 are respectively equal to twice the currents of transistors M10 and M15, the drain-source currents of transistors M3 and M4 can be expressed as follows:

$$I_{DS3} = I_O + I_B + I_{IN} , \qquad (7)$$

$$I_{DS4} = I_O + I_B - I_{IN} . \qquad (8)$$

By replacing (7) and (8) into (6), we obtained:

$$2\sqrt{I_B} = \sqrt{I_O + I_B + I_{IN}} + \sqrt{I_O + I_B - I_{IN}} . \qquad (9)$$

By taking the square from both sides of (9), we get:

$$4I_B = 2I_O + 2I_B + 2\sqrt{I_O^2 + I_B^2 + 2I_O I_B - I_{IN}^2} . \qquad (10)$$

By squaring (10), the output current of the squarer circuit is given by:

$$I_O = \frac{I_{IN}^2}{4I_B} . \qquad (11)$$

On the other hand, if the mobility attenuation factor is taken into account, the gate-source voltage expression of transistor is given by:

$$V_{GS} = V_{TH} + \frac{\theta I_{DS}}{k_n} + \sqrt{\left(\frac{\theta I_{DS}}{2k_n}\right)^2 + 2\frac{I_{DS}}{k_n}} . \qquad (12)$$

Knowing that the mobility attenuation factor is low, such $\theta^2/k_n^2 I_{DS}^2 << 2/k_n I_{DS}$, the gate-source voltage expression has become:

$$V_{GS} \approx V_{TH} + \frac{\theta I_{DS}}{k_n} + \sqrt{2\frac{I_{DS}}{k_n}} . \qquad (13)$$

Assuming that all transistors have the same trans-conductance value and the same mobility attenuation factor $\theta$, equation (14) is given using (13) and (5).

$$\frac{\theta}{k_n}\left(I_{DS1} + I_{DS2}\right) + \sqrt{\frac{2}{k_n}}\left(\sqrt{I_{DS1}} + \sqrt{I_{DS2}}\right)$$
$$= \frac{\theta}{k_n}\left(I_{DS3} + I_{DS4}\right) + \sqrt{\frac{2}{k_n}}\left(\sqrt{I_{DS3}} + \sqrt{I_{DS4}}\right) . \qquad (14)$$

Knowing that the drain-source currents of transistors M1 and M2 are equal to the bias current $I_B$ and by using (7) and (8), equation (14) becomes:

$$2\sqrt{I_B}\left[\sqrt{\frac{2I_B}{k_n}}\,\theta + 1\right] = \sqrt{\frac{2}{k_n}}\,\theta I_O$$
$$+ \sqrt{I_O + I_B - I_{IN}} + \sqrt{I_O + I_B + I_{IN}} . \qquad (15)$$

By taking the square twice on both sides of (15), we get:

$$I_O = \frac{I_{IN}^2}{4I_B} + 2\frac{\theta}{\sqrt{k_n}}I_B\sqrt{I_B}. \tag{16}$$

By comparing (11) and (16), we notice the presence of an undesirable effect caused by reduced mobility under the form $2\left(\theta/\sqrt{k_n}\right)I_B\sqrt{I_B}$.

## 2.2  Proposed Multiplier Circuit

The working principle of a current mode four-quadrant multiplier circuit based on the squared difference identity is given by:

$$I_{OUT} = \left(I_X + I_Y\right)^2 - \left(I_X - I_Y\right)^2 = 4I_X I_Y. \tag{17}$$

Based on (17), the block diagram of the multiplier circuit can be realized by two squarer circuits, a current subtractor and a current adder, as presented in Fig. 2.

The summation and subtraction of input current signals $I_X + I_Y$ and $I_X - I_Y$ respectively are made using an additional input stage composed of simple current mirrors as shown in Fig. 3.

The proposed current mode multiplier circuit is shown in Fig. 4. It consists of two squarer circuits composed by two up-down topology trans-linear loops formed by M1–M4 and M18–M21. Assuming that the input currents are respectively $(I_X + I_Y)$ and $(I_X - I_Y)$, the output current of two squarer circuits are given by:

$$I_{O1} = \frac{\left(I_X + I_Y\right)^2}{4I_B}, \tag{18}$$

$$I_{O2} = \frac{\left(I_X - I_Y\right)^2}{4I_B}. \tag{19}$$

The output current of the second squarer circuit is reversed by the current inverter circuit consisting of transistors M26, M33, M34, M35, M36 and M37.

The output current of multiplier circuit can be written as:

$$I_{OUT} = I_{O1} - I_{O2} = \frac{I_X I_Y}{I_B}. \tag{20}$$

## 2.3  Mismatch Analysis

In this section, the mismatch analyzes for the proposed multiplier circuit are performed. It includes the input current mismatch, the mobility parameter mismatch and the trans-conductance parameter mismatch of transistors.
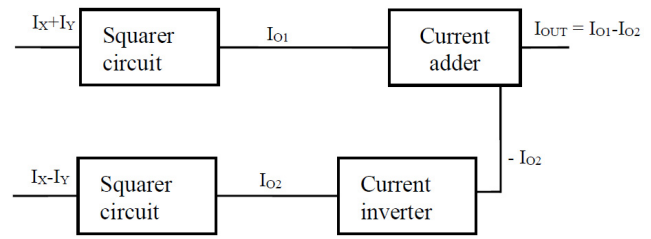


**Fig. 2.**  Block diagram of the proposed current-mode multiplier.
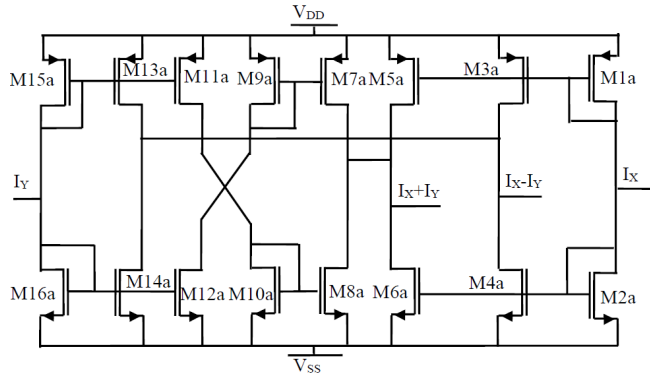


**Fig. 3.**  Summation and subtraction current circuit.

### 2.3.1  Input Current Mismatch

The proposed multiplier circuit requires two well-matched input signals $I_X$ and $I_Y$. It is reported that the mismatch in the input signals leads to a second harmonic distortion condition at the output of the multiplier circuit.

All input currents can be defined as follows in terms of possible mismatches ($i = 1, 2$):

$$\hat{I}_{Xi} = \left(1 + \Delta_{Xi}\right)\hat{I}_X, \tag{21}$$

$$\hat{I}_{Yi} = \left(1 + \Delta_{Yi}\right)\hat{I}_Y. \tag{22}$$

The mean values of input currents are $\hat{I}_X$ and $\hat{I}_Y$. The mismatch percentages of $\hat{I}_{Xi}$ and $\hat{I}_{Yi}$ are $\Delta_{Xi}$ and $\Delta_{Yi}$, respectively.

By considering $\Delta_{Xi}^2$, $\Delta_{Yi}^2$ and $\Delta_{Xi}\Delta_{Yi}$ less than 1, the output currents of squarer circuits are given by:

$$I_{O1}' = \frac{\left(\hat{I}_X + \hat{I}_Y\right)^2}{4 I_B} \\ + \frac{\Delta_{X1}\hat{I}_X^2 - \left(\Delta_{X1} + \Delta_{Y1}\right)\hat{I}_X\hat{I}_Y + \Delta_{Y1}\hat{I}_Y^2}{2 I_B}, \tag{23}$$

$$I_{O2}' = \frac{\left(\hat{I}_X - \hat{I}_Y\right)^2}{4 I_B} \\ + \frac{\Delta_{X2}\hat{I}_X^2 - \left(\Delta_{X2} + \Delta_{Y2}\right)\hat{I}_X\hat{I}_Y + \Delta_{Y2}\hat{I}_Y^2}{2 I_B}. \tag{24}$$
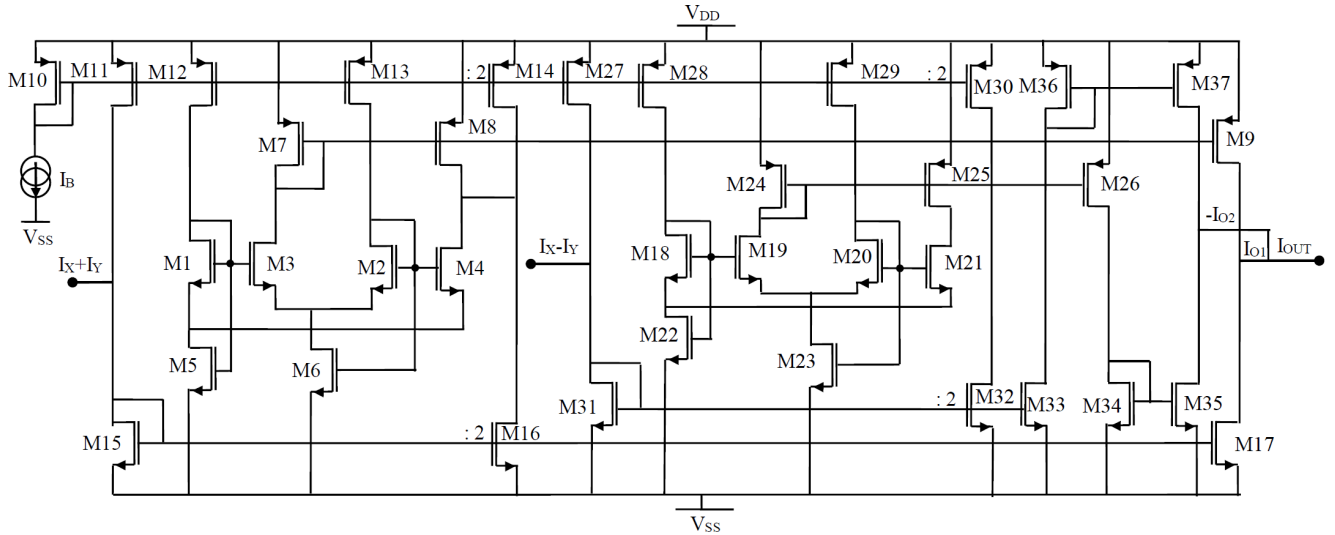
**Fig. 4.** Proposed current-mode multiplier.

The output current of multiplier circuit can be written as:

$$I'_{OUT} = I'_{O1} - I'_{O2}$$
$$= \frac{\hat{I}_X \hat{I}_Y}{I_B} + \frac{\delta_X \hat{I}_X^2 - (\Delta_X + \Delta_Y)\hat{I}_X\hat{I}_Y + \delta_Y \hat{I}_Y^2}{2 I_B} \quad (25)$$

where

$$\begin{cases} \delta_X = \Delta_{X1} - \Delta_{X2} \\ \delta_Y = \Delta_{Y1} - \Delta_{Y2} \end{cases} \begin{cases} \Delta_X = \Delta_{X1} + \Delta_{X2} \\ \Delta_Y = \Delta_{Y1} + \Delta_{Y2} \end{cases}.$$

In (25), if one of the inputs $\hat{I}_X$ is assumed constant and the other is sinusoidal in the form of $\hat{I}_Y = \hat{i}_m \sin(\omega t)$, the second harmonic distortion from the input signal offsets can be calculated as follows:

$$HD_2 = \frac{1}{2} \frac{\delta_X}{(\Delta_X + \Delta_Y)\hat{I}_X + 2\hat{I}_X} \hat{i}_m. \quad (26)$$

According to (26), it should be noted that the mismatch ratio increases and the second harmonic distortion also increases.

However, it remains roughly stable and does not significantly change the distortion of the third harmonic, as it does not show up in manual calculations.

### 2.3.2 Mobility Parameter Mismatch

If we assumed that the mobility parameter of the proposed multiplier circuit is not perfectly adapted, the output currents of the squarer circuits can be written as:

$$I'_{O1} = \frac{(I_X + I_Y)^2}{4I_B} + 2\frac{\Delta\theta}{\sqrt{k_n}} I_B\sqrt{I_B}, \quad (27)$$

$$I'_{O2} = \frac{(I_X - I_Y)^2}{4I_B} + 2\frac{\Delta\theta}{\sqrt{k_n}} I_B\sqrt{I_B}. \quad (28)$$

The output current of the proposed multiplier circuit can be written as:

$$I'_{OUT} = I'_{O1} - I'_{O2}. \quad (29)$$

Using (27), (28) and (29), the output current is given by:

$$I'_{OUT} = \frac{I_X I_Y}{I_B}. \quad (30)$$

The absolute error is given by:

$$I_{error} = |I_{OUT} - I'_{OUT}| = 0. \quad (31)$$

We can see from (31) that the proposed multiplier is insensitive to mismatch in carrier mobility parameter.

### 2.3.3 Transconductance Parameter Mismatch

If we assume that the transconductance parameter of the transistor does not fully match, the output currents of the squarer circuits can be written:

$$I'_{O1} = \frac{(I_X + I_Y)^2}{4I_B} + 2\frac{\theta\Delta k_n}{k_n\sqrt{k_n}} I_B\sqrt{I_B}, \quad (32)$$

$$I'_{O2} = \frac{(I_X - I_Y)^2}{4I_B} + 2\frac{\theta\Delta k_n}{k_n\sqrt{k_n}} I_B\sqrt{I_B}. \quad (33)$$

Combining (29), (32), and (33), we get:

$$I'_{OUT} = I'_{O1} - I'_{O2} = \frac{I_X I_Y}{I_B}. \quad (34)$$

The absolute error is given by

$$I_{error} = |I_{OUT} - I'_{OUT}| = 0. \quad (35)$$

This means that the proposed circuit is insensitive to mismatch in trans-conductance parameter.

## 2.4  Simulation Results

The simulation results of the proposed circuits are verified using Tanner TSPICE simulator with 0.18 μm CMOS parameter technology under a supply voltage of ±0.75 V and a bias current $I_B$ of 10 μA. The aspect ratios of the transistors are shown in Tab. 1.

Figure 5 shows the transient analysis characteristic of the proposed squarer circuit where the input signal has a triangular form with 40 μA peak-to-peak amplitude and 1 MHz of frequency as shown in the top graph. The output current is presented in the middle graph. The bottom graph of figure shows the value of the measured error, which is swept between 22.3 nA and –21.4 nA.

Figure 6 shows the transient analysis characteristic of the proposed squarer circuit where the input current is the sum of two sinusoidal currents $I_X$ and $I_Y$ with a 1 MHz frequency and amplitudes 20 μA and 10 μA, respectively.

The DC transfer characteristic of the proposed four-quadrant analog multiplier is shown in Fig. 7. The input current $I_X$ varied between –20 μA to 20 μA, when the current $I_Y$ has the same disparity from –20 μA to 20 μA with step size 4 μA.

| Transistors | W(μm)/L(μm) |
|---|---|
| M1, M2, M3, M4, M18, M19, M20, M21 | 5.2/0.18 |
| M7, M8, M9, M24, M25, M26, M36, M37 | 5/0.18 |
| M10, M11, M12, M13, M27 | 10/0.18 |
| M14, M30 | 20/0.18 |
| M15, M17, M31, M33 | 0.27/0.18 |
| M16, M32 | 0.5/0.18 |
| M5, M22, M34, M35 | 1/0.18 |
| M6, M23 | 3.5/0.18 |
| M28, M29 | 10/0.18 |

Tab. 1.  Transistor aspect ratios of the proposed multiplier circuit.
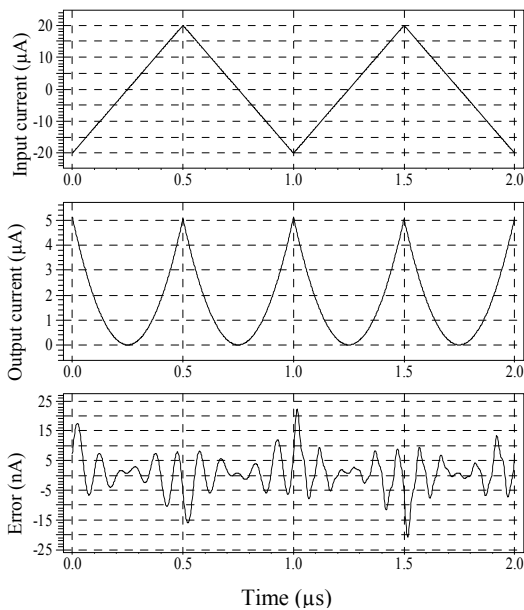
Fig. 5.  Transient analysis characteristic of the squaring circuit with triangular form input signal.
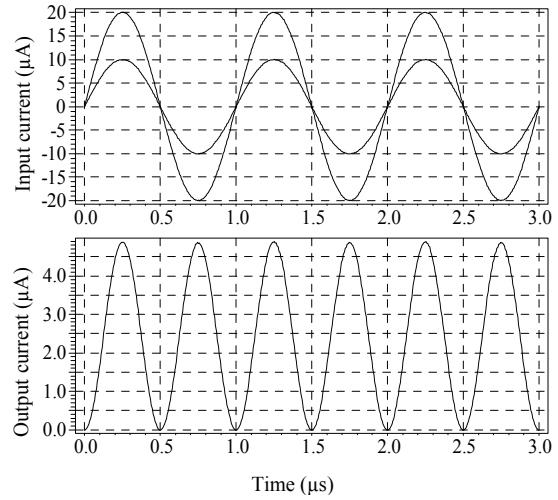
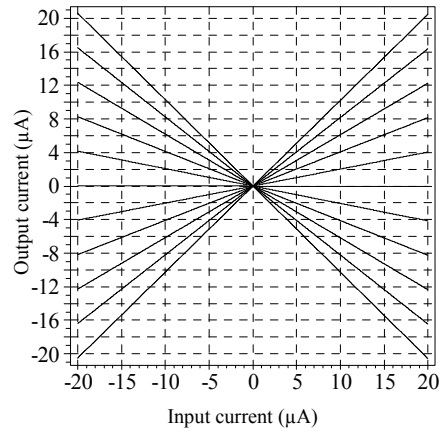Fig. 6.  Transient analysis characteristic of the squarer circuit with sinusoidal form input current.

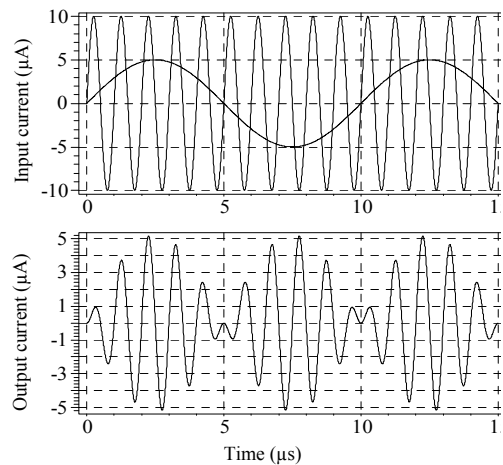Fig. 7.  DC simulation result of the multiplier circuit.

Fig. 8.  Simulation result of analog amplitude as modulator.

The application of multiplier used as a modulator is shown in Fig. 8. The input current signals $I_X$ and $I_Y$ are set to 1 MHz and 100 kHz with peak-to-peak amplitude of 10 μA and 5 μA, respectively. The variations of total harmonic distortion (THD) with respect to the peak-to-peak amplitude of the input signal $I_X$ when $I_Y$ amplitude equal to 10 μA at 100 kHz and 1 MHz are shown in Fig. 9. In the

worst case, when $I$x is equal to 40 µA peak-to-peak amplitude at 1 MHz, the total harmonic distortion is obtained 0.8%.

The variation of temperature as a function of relative error is shown in Fig. 10. The simulation results are obtained using a transient signal input current $I_X$, with an amplitude of 10 µA and a frequency of 1 MHz, and a constant current $I_Y$ equal to 10 µA. The maximum error is reported at 75°C as 1.18 %. The output at 25°C is considered as the ideal value with zero relative error, so that the outputs obtained at other temperatures are calculated based on the reference value.

The frequency response of the multiplier is checked using an AC input current $I_X$ with an amplitude equal to 10 µA and a constant current $I_Y$ equal to 10 µA. The simulation result obtained is shown in Fig. 11, where the low frequency gain is −120 and the bandwidth obtained is 850 MHz. The power consumption of the circuit is 105 µW.

Monte Carlo analysis is performed for 100 samples by applying a ±5% Gaussian distribution for temperature effect to analyze bandwidth and gain variations, as shown in Fig. 12. These simulations are performed using an AC
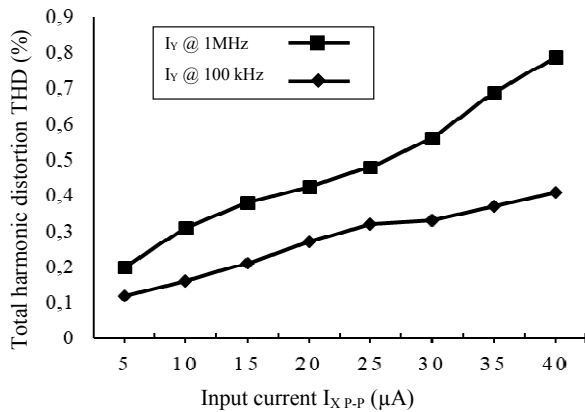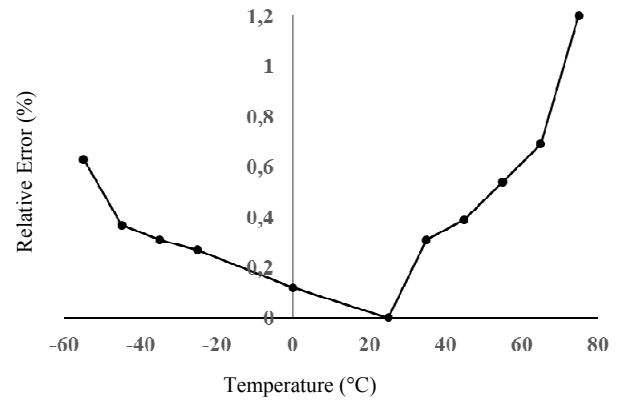


**Fig. 10.** Relative error variation with different temperatures
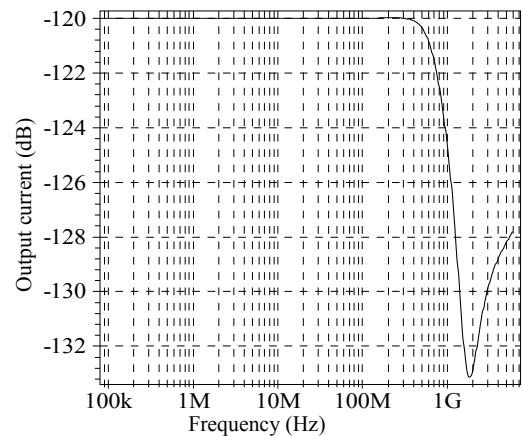


**Fig. 11.** Frequency response of the multiplier.

input current $I_X$ with 10 µA DC component and a constant current $I_Y$ equal to 10 µA. The mean values of bandwidth and gain are 848 MHz and −120.38, respectively.

The proposed multiplier is compared to recently published work as presented in Tab. 2. Simulation results from the proposed multiplier indicate better performance in terms of supply voltage, bandwidth, high accuracy and power consumption.



**Fig. 9.** Relation between THD and input current $I_X$.



(a)



(b)

**Fig. 12.** Monte-Carlo analysis results about (a) bandwidth, and (b) gain of the multiplier.

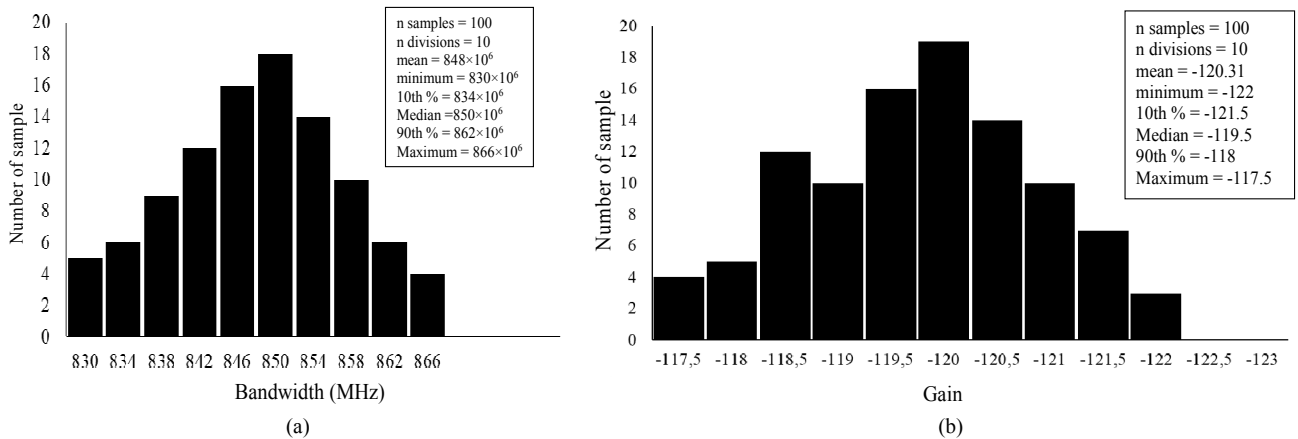| Ref | Year | Power supply (V) | Power consumption (μW) | –3 dB bandwidth (MHz) | Nonlinearity (%) | THD (%) | Technology (μm) |
|---|---|---|---|---|---|---|---|
| [1] | 2013 | 1.2 | 75 | 59.7 | 0.9 | N/A | 0.18 |
| [8] | 2020 | 1.8 | 61.9 | 736 | 0.93 | 0.98 (20 μA, 1 MHz) | 0.18 |
| [11] | 2009 | 3.3 | 340 | 41.8 | 1.1 | 0.97 (20 μA, 1 MHz) | 0.35 |
| [15] | 2009 | 3.3 | 240 | 44.9 | 1.15 | 0.76 (20 μA, 1 MHz) | 0.35 |
| [23] | 2016 | 2.8 | 0.521 | 137 | 1.12 | 1.45 (20 μA, 1 MHz) | 0.35 |
| [24] | 2019 | 0.8 | 92 | 623 | 0.69 | 0.97 (20 μA, 1 MHz) | 0.18 |
| [25] | 2017 | 1 | 0.508 | 33.52 | 2.9 | 2.05 (0.1 μA, 100 kHz) | 0.18 |
| [26] | 2018 | 0.8 | 770 | 34.1 | 2 | 0.67 (50 nA, 0.1 MHz) | 0.18 |
| [27] | 2021 | ± 1 | 700 | 260 | N/A | 0.49 (±150 μA, 1 MHz) | 0.5 |
| [28] | 2014 | 1.5 | 700 | 230 | 1.8 | N/A | 0.18 |
| [29] | 2012 | ± 0.75 | 2.3 | 2.8 | 0.3 | 0.7 (20 nA, 1 kHz) | 0.35 |
| [30] | 2017 | 1.8 | 144 | 62 | 1.5 | 1 (10 μA, 10 kHz) | 0.18 |
| [31] | 2005 | 2 | 5.5 | 0.2 | 5 | 0.9 (150 nA, 0.2 MHz) | 0.35 |
| [32] | 2000 | 5 | N/A | N/A | N/A | 2(50 μA, 10 kHz) | 2.4 |
| [33] | 2001 | 3.3 | 600 | 3 | N/A | 1.5 (20 μA, 10 kHz) | 2.4 |
| [34] | 2014 | 1 | 90 | N/A | N/A | N/A | 0.18 |
| This work | ----- | ±0.75 | 105 | 850 | 0.85 | 0.42 (20 μA, 1 MHz) | 0.18 |

**Tab. 2.** Comparison between the proposed multiplier and others reported in the literature.

# 3.  Conclusion

This work presents a new CMOS current mode analog four-quadrant multiplier. The proposed circuit is designed by using two low voltage squarer circuits based on the up-down topology trans-linear loop and the flipped voltage followers (FVF).

The simulation results have verified by TSPICE using TSMC 0.18 μm CMOS process available from MOSIS at 25°C with ±0.75 V supply voltage. The circuit is characterized by a low power consumption 105 μW, a wide bandwidth about 850 MHz and a low nonlinearity error of 0.85%.

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