A 2 V, 32.13 nA, fully MOSFET Voltage Limiter for Low Power Applications

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Abstract. *This paper presents a fully MOSFET DC voltage limiter with low current consumption. In the proposed voltage reference structure to reduce power consumption, transistors are biased in the sub-threshold region. To generate complementary to absolute temperature (CTAT) voltage in the voltage reference circuit, only a PMOS transistor is used, in which its drain, gate, and source terminals are connected together and acts as a diode that reduces the layout area occupation. To further reduce power consumption, a part of the rectifier output voltage is compared with the reference voltage by the sampling circuit. Also, four stage inverters are used as buffers to provide the I-V limiting characteristic closer to the ideal situation. The use of series pass-gate transistors in the first inverter also reduces power consumption as much as possible.*

The results of post-layout simulation based on 0.18μm CMOS technology depict that the suggested voltage reference circuit has a reference voltage equivalent to 0.579 V with a TC of 37.2 ppm/°C in the temperature range of –50°C to 50°C. LR and PSRR attained 0.008%/V and 45 dB, respectively. The output voltage and current consumption of the limiter circuit are 2 V and 32.13 nA, respectively. The total layout area of the proposed limiter is 3249 μm^2.

Keywords

Limiter, voltage reference, temperature coefficient, low power, voltage sampler, OPA, buffer

1. Introduction

Nowadays low voltage and low power consumption concepts are the most significant procedures in the design of electronic circuits and peripheral systems. Radio Frequency Identification (RFID) as an innovative technology in the management of existing systems, use a passive structure to minimize the power consumption and costs of tag creation [1], [2]. In fact, a passive RFID tag receives its energy from electromagnetic waves transmitted from the reader. At close distances, the power received by the tag from the reader increases and can interfere with the operation of the circuits in the tag chip. Therefore, using a limiter circuit to protect the tag chip is inevitable. To reduce power consumption, the limiter deviation current should be low when the tag and the reader are spaced apart [3], [5]. In [6], [7], used limiters are based on the voltage division structure, where large changes in the limiter voltage can be observed with variations in temperature and fabrication process, and the current consumption in the range of microampere has caused these structures to be used rarely.

In the limiter configuration typically the voltage reference block can be utilized for the comparison, to create a stable voltage. Voltage references over the past decade have been designed to generate voltage with a temperature coefficient (TC) of almost zero from the sum of the effects of positive and negative temperature coefficient signals using MOS transistors that operate in the weak or strong inversion region. The desire to reduce construction costs also encouraged designers to develop fully MOSFET voltage references [8–11].

In recent papers, the reference voltage is derived from the unequal threshold voltage of different NMOS or PMOS transistors [12], [13]. Therefore, it should be noted that using this technique increases the cost of bandgap reference (BGR) fabrication and the amount of power consumption is undesirable. To be able to attain a reduction in the temperature coefficient of the reference voltage, in [14], [15], the thermal voltage is introduced to generate the proportional to absolute temperature (PTAT) voltage and the complementary to absolute temperature (CTAT) property of the threshold voltage coefficients. However, due to existence of the resistors in these circuits, the design in the nanoampere current range is problematic, since in this regard, a voltage drop of several hundred millivolts and large resistors are required.

The proposed DC voltage limiter uses OPA, voltage reference, voltage sampler and buffer blocks. Diverse blocks used in the proposed circuit are designed with MOSFET transistors only. In the voltage reference part, a MOSFET transistor in which source, drain and gate terminals are connected together is used as a PN junction to provide the CTAT voltage. To achieve the desired reference voltage, two identical MOSFET transistors are used to reduce the CTAT voltage level. The PTAT voltage is provided by a cascade circuit stage and a differential stage

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circuit. The proposed voltage reference has a small layout area, low power consumption and high power supply rejection ratio (PSRR). Very low power consumption is achievable by considering that all transistors operate in sub-threshold region. The use of inverters in four stages at the OPA output helps to divert the current as much as possible and limiting the output voltage as soon as the input voltage increases.

The general architecture and structure of the DC voltage limiter along with the proposed voltage reference are investigated comprehensively in Sec. 2. Section 3 represents the post-layout simulation outcomes by the proposed voltage reference and voltage limiter. Finally, the paper is concluded in Sec. 4.

2. Proposed DC Voltage Limiter

The main designers' concerns for wireless and portable applications such as the Internet of Things (IoT) and RFID systems is providing the supply for the receiver. One of the most important parts of providing proper power supply for the circuits is the power management unit (PMU). Figure 1 indicates the various sections of the PMU. According to Fig. 1, first RF waves are received by the antenna, these waves are converted to electrical signal by the antenna and then to DC voltage by the rectifier. In some cases, voltage multiplier circuits are used as rectifiers to provide the voltage level with the suitable value [16]. Since this voltage level depends on the input power, which is itself a function of the distance from the transmitter, as the distance decreases, the power attained by the receiver increases significantly. Therefore, to prevent damage to the circuit, a DC voltage limiter and an RF clamp are essential to be settled in the power supply circuit. The limiter block prevents voltage increments and possible damage to the circuit when the transmitter and receiver are near to each other. In the next step, the voltage regulator also eliminates the ripples of the rectifier output signal and the voltage obtained with DC to DC converter is changed to different voltage level to supply other circuit blocks [17].

In this paper, a complete structure of a low power DC voltage limiter circuit will be presented. In the proposed DC limiter circuit, the voltage sampled from the rectifier output (V_{samp}) by OPA is compared to the reference voltage (V_{ref}). If the rectifier output voltage (V_{rec}) is greater than V_{Lim}, then $V_{samp} > V_{ref}$ and the OPA output becomes high. In this case, after passing through the buffer, the gate of M_{Pass} transistor becomes high and prevents the increment of V_{rec} voltage by providing a deflection path for the current.

2.1 Proposed Voltage Reference Circuit

The proposed voltage reference is observable according to Fig. 2. In this circuit, a PMOS transistor in which its three terminals, gate, source, and drain terminals are connected together and which performs as a diode is used as the CTAT voltage generator. In such a structure, due to the connection of the body to ground and the connection of source, drain and gate to non-zero and positive voltage, the resulting diodes are in direct bias state. In case of providing a sufficient voltage difference, a diode voltage drop will be obtained from this connection. V_D is the CTAT voltage generated by M_{C1}, which is equal to the gate-source voltage of two NMOS transistors, M_{c2} and M_{p1}. Since M_{c2} and M_{p1} have the identical current in the same dimensions, the V_{CTAT} created on the M_{c2} diode junction transistor is $V_D/2$. The PTAT voltage is obtained by a self-cascade stage and a stage of a differential circuit, which is added to the V_{CTAT} to produce a reference voltage with a low temperature coefficient. Since PTAT and CTAT voltage generator transistors operate in sub-threshold region, low power consumption can be seen.

If $|V_{DS}|$ of a MOSFET is larger than $4V_T$, the sub-threshold I_D current is almost independent of V_{DS} and can be obtained as (1):

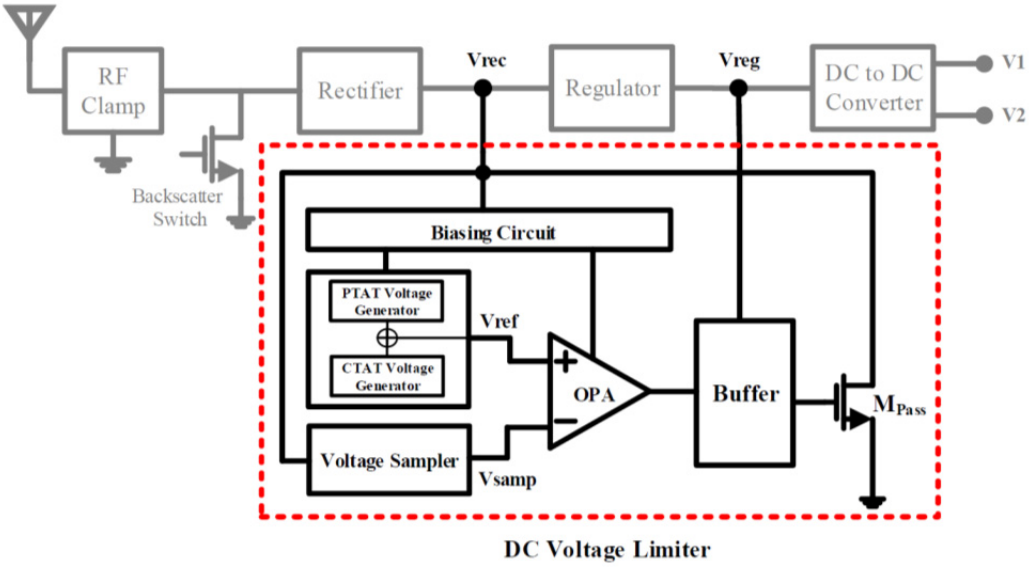

Fig. 1. Block diagram of PMU and the proposed DC voltage limiter.

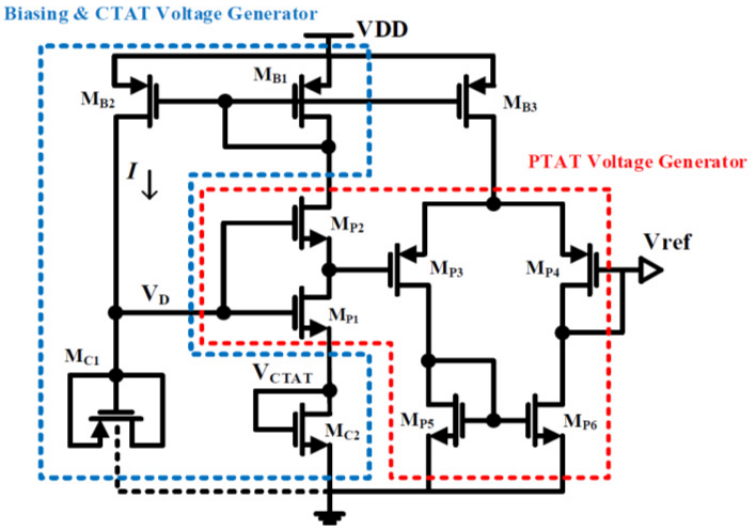

Fig. 2. Schematic of the proposed voltage reference.

$$I_{\mathrm{D}} = K\mu C_{\mathrm{OX}} V_{\mathrm{T}}^2 (\eta - 1) \exp\left[\left(\left|V_{\mathrm{GS}}\right| - \left|V_{\mathrm{TH}}\right|\right) / (\eta V_{\mathrm{T}})\right] \quad (1)$$

where K is the dimensional ratio ($K = W/L$) of a MOSFET, μ carrier mobility, C_{OX} gate oxide capacitance, η the slope factor in sub-threshold, V_{T} ($= k_{\mathrm{B}}T/q$) is the thermal voltage, k_{B} is the Boltzmann constant, T is the absolute temperature, and q is the electron charge.

In the structure of cascaded PTAT voltage generator, the PTAT voltage is obtained from the voltage difference of gate-source of M_{p1} and M_{p2}, which is proportional to the thermal voltage.

By adjusting the current and width ratios of the transistors ($I_{M_{p1}} K_{M_{p2}} > I_{M_{p2}} K_{M_{p1}}$), the first stage PTAT voltage can be obtained using (1) as (2):

$$V_{\text{Cascode PTAT}} = V_{\mathrm{DS,M_{p1}}} = \eta V_{\mathrm{T}} \ln\left(\frac{I_{M_{p1}}}{I_{M_{p2}}} \cdot \frac{K_{M_{p2}}}{K_{M_{p1}}}\right). \quad (2)$$

A differential PTAT circuit stage is also used to increase the PTAT voltage gradient, to eliminate the negative temperature dependence of V_{D}. The differential PTAT voltage is shown in (3):

$$V_{\text{Diff. Pair PTAT}} = V_{\mathrm{GS,M_{p3}}} - V_{\mathrm{GS,M_{p4}}} = \eta V_{\mathrm{T}} \ln\left(\frac{I_{M_{p3}}}{I_{M_{p4}}} \cdot \frac{K_{M_{p4}}}{K_{M_{p3}}}\right). \quad (3)$$

Conforming to (3), the differential PTAT voltage can also be investigated based on the difference between the gate-source voltages of the M_{p3} and M_{p4} transistors. It shall continually be noted that the value in front of Ln must be greater than unit to produce a PTAT voltage. Therefore, the voltage reference output is calculated as (4) according to the sum of the cascaded and differential PTAT voltage and half of the diode voltage:

$$V_{\mathrm{ref}} = \frac{V_{\mathrm{D}}}{2} + \eta V_{\mathrm{T}} \ln\left(\frac{I_{\mathrm{Mp1}}}{I_{\mathrm{Mp2}}} \cdot \frac{I_{\mathrm{Mp3}}}{I_{\mathrm{Mp4}}} \cdot \frac{K_{\mathrm{Mp2}}}{K_{\mathrm{Mp1}}} \cdot \frac{K_{\mathrm{Mp4}}}{K_{\mathrm{Mp3}}}\right). \quad (4)$$

As a result, by properly adjusting the dimensions of the transistors and the bias current, the PTAT voltage generator can neutralize the negative temperature coefficient of the CTAT voltage and produce a temperature-independent reference voltage.

2.2 The Structure of the Proposed DC Voltage Limiter and Its Sub-blocks

Figure 3 indicates the proposed limiter circuit. In this circuit, a part of the rectifier output voltage (V_{rec}) is sampled by the voltage sampling block. Six NMOS transistors (M_{S1} to M_{S6}) are used in the voltage sampling structure as a diode connection. Using voltage sampling block reduces the voltage level ($V_{\mathrm{samp}} < V_{\mathrm{ref}}$) which in other words also decreases the power consumption.

In the limiter structure, the sampled voltage (V_{samp}) is compared with the output voltage of voltage reference (V_{ref}) by the OPA block. In the design of OPA block, a differential pair circuit and a cascode current mirror as an active load are utilized. Assuming the value of V_{rec} is greater than V_{Lim}, the sampled voltage (V_{samp}) is higher than V_{ref}, so the M_{O2} gate voltage will be higher than the M_{O1} gate voltage. Since both transistors are PMOS and their source terminals are equipotential, the current through the M_{O1} transistor will be increased and consequently the voltage drop across the M_{O3} and M_{O5} transistors as active loads increases. As a result, the input of the first NOT is high, and finally the output of the fourth NOT, which is connected to the gate of the M_{Pass} transistor, also shows a high voltage, which causes the M_{Pass} transistor to be ON.

In this way, a large current flow can be observed in this branch, which prevents the rectifier voltage from increasing and limits it to a limited voltage. Now if the sampled voltage is lower than V_{ref}, with a similar analysis the voltage of the M_{Pass} gate will be logically low and the M_{Pass} transistor will not turn ON. In other words, it can be inferred that due to the low power consumption that reaches the receiver, the V_{rec} voltage level is not high and there is no need to activate the voltage limiter.

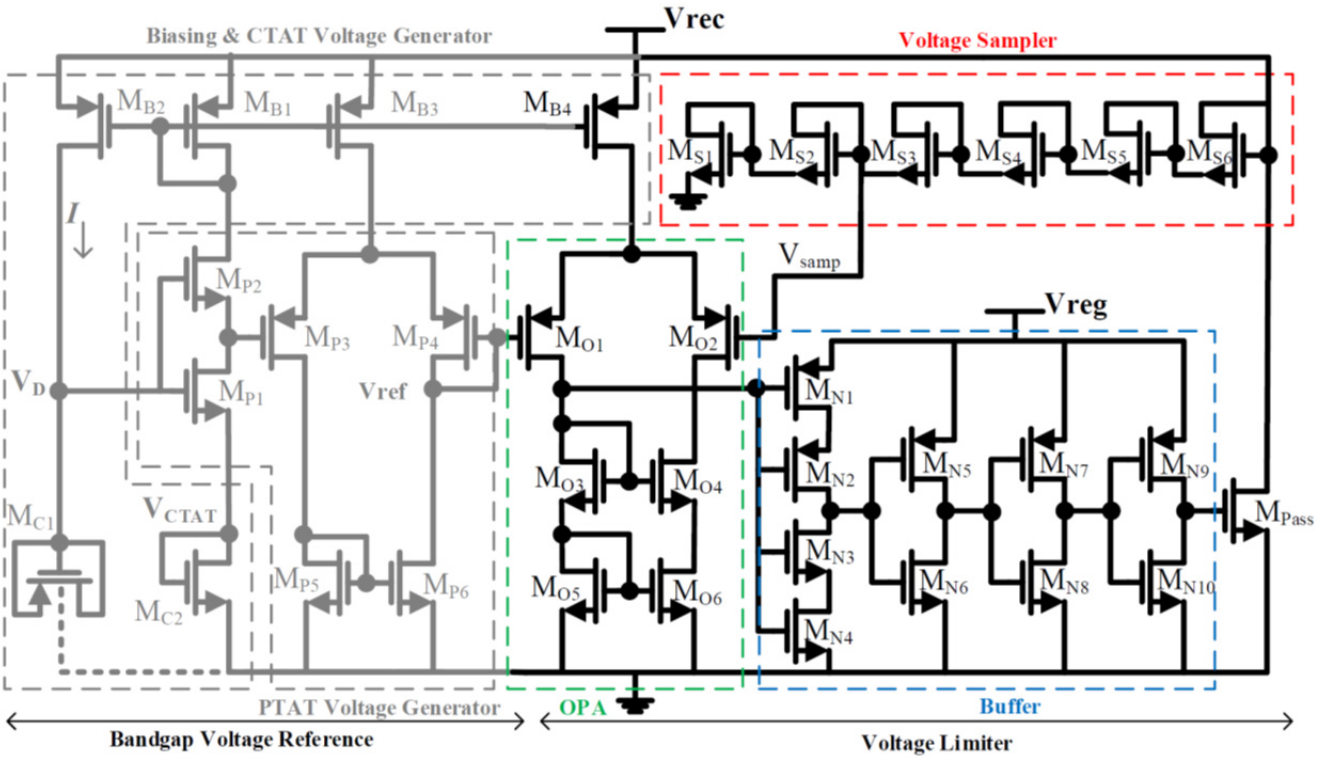

Fig. 3. General schematic of the proposed voltage limiter.

Ideally, when the limiter operates, the current drawn to protect the receiver from V_{rec} is infinite. For the proper operation of the limiter and approaching the ideal state, four inverters in a row are used at the OPA output to create the appropriate voltage level at the output of the fourth inverter. As the number of inverters increases, the I-V characteristic curve of the limiter becomes more ideal, but the circuit will consume more power. Therefore, four inverters are used to establish a proper trade-off power consumption and an almost ideal characteristic curve.

Four series inverters (M_{N1} to M_{N10}) are supplied by a 1 Volt regulator. The first inverter uses the series pass-gate transistors structure, which significantly reduces the power consumption of this block.

The DC limiting voltage equal to 2 V is obtained by the proposed circuit. Due to the fact that the required power of the receiver is provided by the transmitter waves, increasing the distance between the transmitter and the receiver reduces the received power. Therefore, less power dissipation of the receiver sub-blocks will increase the range of information exchange.

3. Post-layout Performance Evaluations

Regarding the design of the proposed voltage limiter, in the first step, with the help of equations (1), (2), and (3), a voltage reference circuit is designed to obtain a voltage, independent of temperature and supply. Then, using a comparator, a sample of the output is compared with the reference voltage. To reduce power consumption, instead of resistor voltage dividers, a fully MOSFET sampling circuit has been used, which can be achieved by using diode-connected transistors. Finally the buffer is used to provide the I-V limiting characteristic closer to the ideal situation. In the buffer structure, by using the series pass-gate transistors structure in the first inverter, the power consumption has been significantly reduced. The simulations are carried out by Cadence simulator using 0.18µm CMOS technology. In the design process, using the Global Optimization Cadence, the sizes of the transistors have reached the optimum possible state to reduce the layout area and power consumption and achieve the best answer.

Figure 4 clearly shows the results of the voltage reference output in terms of temperature variations in the range of –50°C to 50°C with $V_{rec} = 2$ V for the simulations in schematic and post-layout circumstances. Considering the voltage reference output equal to 0.579 V, the temperature coefficient based on [19] in schematic and post-layout simulations has been obtained 31.7 ppm/°C and 37.2 ppm/°C, respectively.

The output voltage characteristic in the schematic and post-layout simulations in terms of supply voltage variations from 0 V to 4 V is shown in Fig. 5. As can be seen, the results of the post-layout simulation are almost identical to the schematic simulation results. For the supply voltage variation from 0.7 V to 4 V and according to [19], the line regulation (LR) has been calculated equal to 0.008%/V.

The influence of the fabrication process on the performance of the voltage reference circuit is simulated using Monte Carlo, taking into account process variations and mismatch for 100 run, is shown in Fig. 6. The mean value (μ) and standard deviation (σ) of the reference voltage V_{ref} are 0.579 V and 0.019 V, respectively, and the value of the variation coefficient (σ / μ) is about 0.03.

The reference voltage variation attained by the corner analysis for the considered temperature range equal to –50°C to 50°C can be seen in Fig. 7. In this design, three processes including tt, fs and sf are evaluated for the corner analysis. The simulation results regarding the corner analysis for V_{ref} in three different considered circumstances versus supply voltage of 2 V demonstrate that V_{ref} varies at 27°C from 0.56 V to 0.59 V.

The voltage reference output in terms of power supply variations at –20°C, 0°C, 27°C (room temperature), and 40°C temperatures is illustrated in Fig. 8. Accordingly, the dependence of the reference voltage under the various intended temperatures for supply voltages higher than 0.7 V is low and the reference voltage operates near 0.59 V.

Figure 9 represents the measured output voltage versus temperature between –50°C to 50°C under different values of power supply (1 V, 1.2 V, 1.5 V, 1.8 V and 2 V). According to Fig. 9, for diverse power supply voltages, the temperature coefficient is acceptable and achieved as 42.5 ppm/°C, 32.7 ppm/°C, 26.4 ppm/°C, 29.8 ppm/°C and 37.2 ppm/°C, respectively.

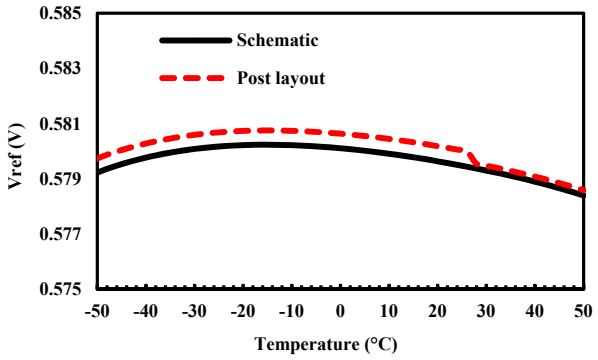

Fig. 4. Changes in the reference voltage in terms of temperature in the range of –50°C to 50°C.

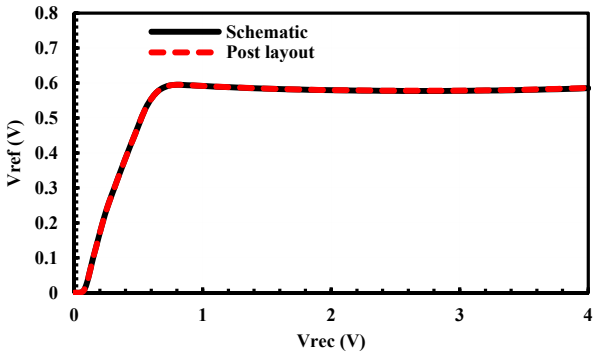

Fig. 5. Characteristics of the reference voltage in terms of power supply.

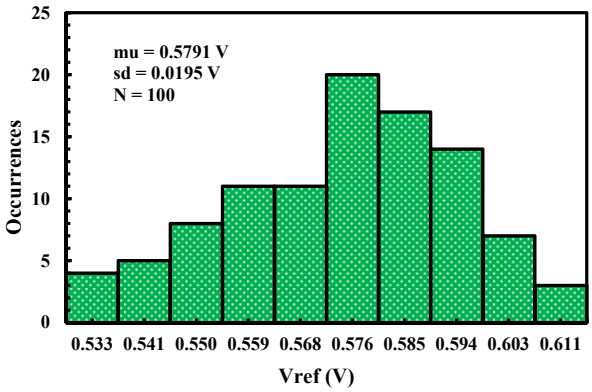

Fig. 6. Monte Carlo analysis results for V_{ref} versus 100 run.

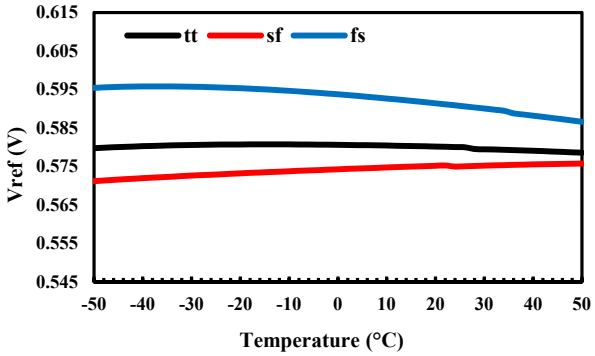

Fig. 7. Output voltage variations under the corner analysis for a temperature range of –50°C to 50°C.

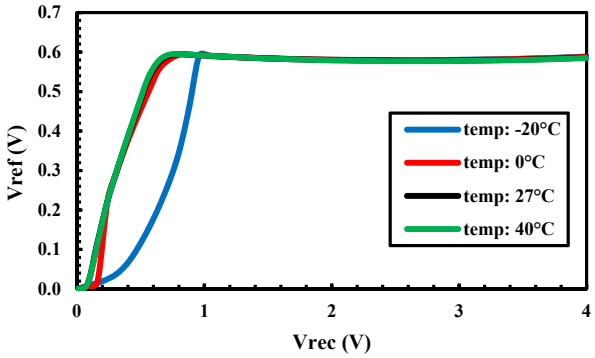

Fig. 8. Reference voltage variations based on power supply under four different temperatures.

The temperature coefficient characteristic in terms of supply voltage is shown in Fig. 10 .This parameter is optimized for the voltage of the power supply 2 V, which in this case reaches 37.2 ppm/°C, according to the figure, the temperature coefficient with the power supply voltage of 1 V will also reach 42.5 ppm/°C. This increase is mainly due to the output resistance of the transistors, which unbalances the current relations and changes the CTAT and PTAT voltage values.

The simulated PSRR of the proposed voltage reference at room temperature is indicated in Fig. 11. The obtained PSRR –45 dB is under the consideration of supply voltage of 2 V at 100 Hz. Also, the results of corner analysis in PSRR measurement for five processes tt, ff, ss, fs and sf are evaluated in Fig. 12. Table 1 provides the specifica-

tions of the proposed voltage reference circuit in comparison with the recently reported reference circuits which are without resistor and low-power.

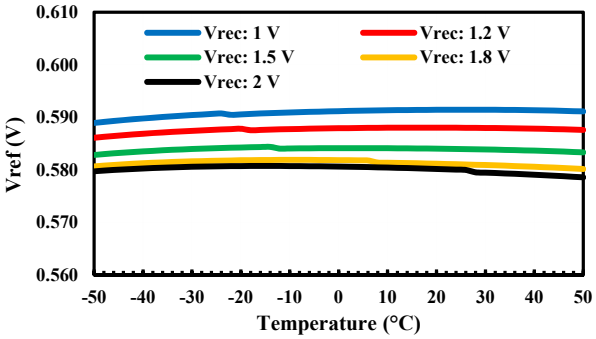

Fig. 9. Changes in the reference voltage with respect to temperature versus different supply voltages.

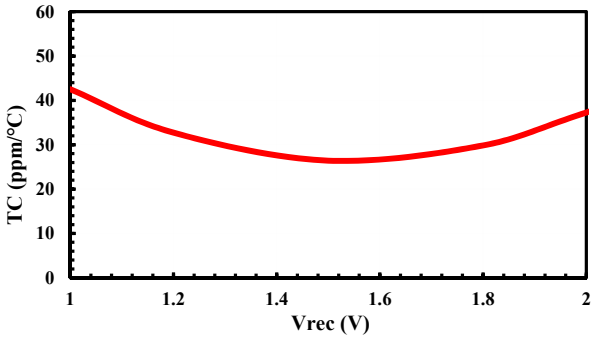

Fig. 10. Temperature coefficient characteristic in terms of supply voltage.

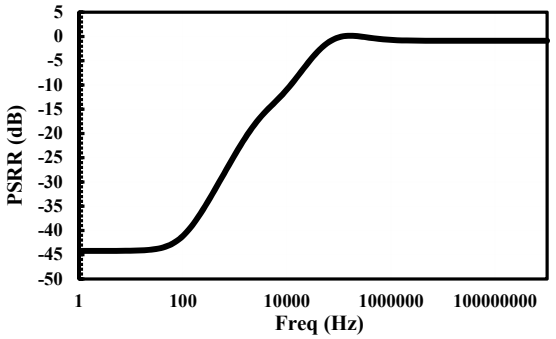

Fig. 11. Simulated PSRR for voltage reference.

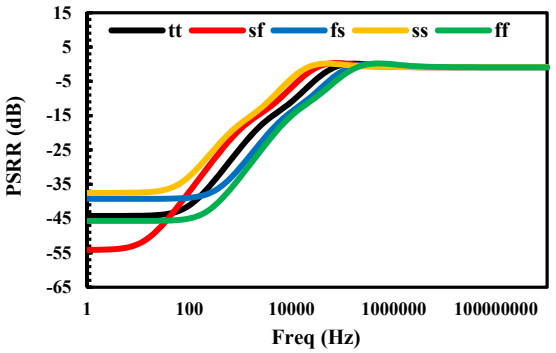

Fig. 12. The result of corner analysis of voltage reference's PSRR.

Figure 13 shows the I-V characteristic of limiter in the range of 1 V to 3 V rectifier for both schematic and post-layout modes. Also, the power consumption curve of the proposed limiter circuit in terms of V_{rec} is shown in Fig. 14. The total current consumption in the limited voltage is equal to 32.13 nA.

Figure 15 provides information regarding the temperature variations in the range –15°C to 35°C for the limited voltage. In addition, the results of the Monte Carlo analysis of the limited voltage with respect to process variations and mismatch versus 100 run are presented in Fig. 16. The mean value (μ) and standard deviation (σ) of the limited voltage (V_{Lim}) are 2 V and 0.31 V, respectively, and the value of the coefficient of variation (σ/μ) is about 0.155 V.

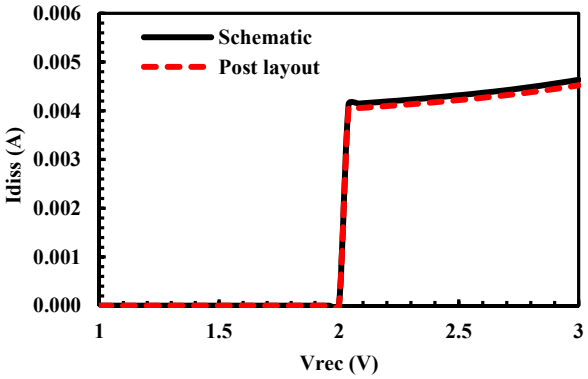

Fig. 13. I-V characteristic of voltage limiter.

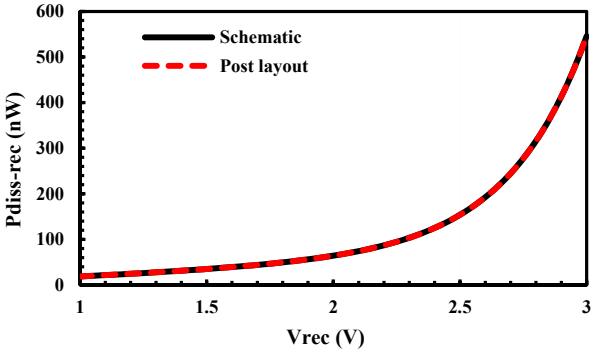

Fig. 14. Power consumption characteristic in terms of V_{rec} variations in the range 1 V to 3 V.

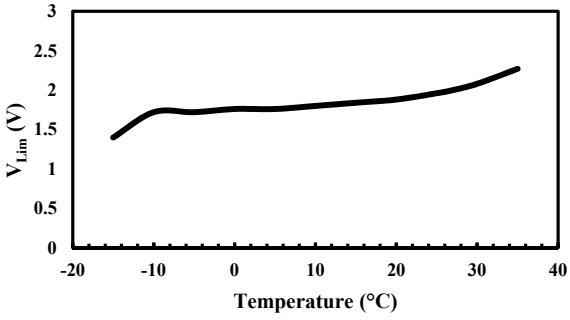

Fig. 15. Limited voltage changes versus temperature variations from –15°C to 35°C.

Parameter	This Work	[10]	[12]	[14]	[15]	[18]
Technology	0.18 µm CMOS	0.18 µm CMOS	0.18 µm BiCMOS	0.18 µm CMOS	0.18 µm Digital CMOS	0.13 µm CMOS
Temperature range (°C)	–50–50	–40–125	–40–125	–40–125	–40–120	0–80
Supply voltage (V)	0.7–4	0.9–2	0.7–2	0.6–2	0.7–2	0.5–1.5
Line regulation (%/V)	0.008	0.06	0.027	0.4	0.031	–
Vref (V)	0.579	0.411	0.368	0.218	147	0.498
Temperature Coefficient (ppm/°C)	37.2	33.7	43.1	23.5	66.38	75
PSRR (dB)	–45 @ 100 Hz	–44 @ 100 Hz	–39 @ 1 kHz	–42.4 @ 1 kHz	–64 @ 1 MHz	–
Power consumption (nW)	21.3	85	28	30.5	21	32
Area (mm^2)	0.002	0.11	0.055	0.075	0.005	0.0264

Tab. 1. Different parameters comparison of the proposed voltage reference and the other circuits.

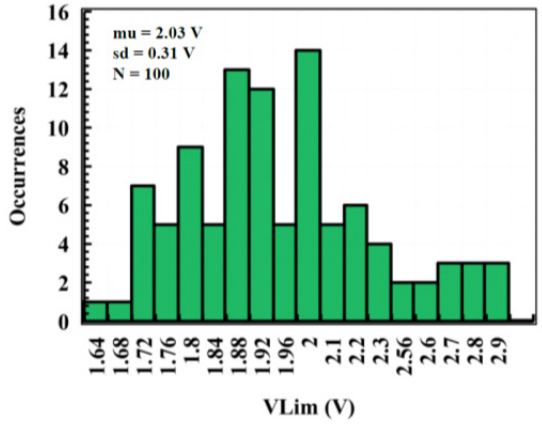

Fig. 16. Monte Carlo simulation of the limited voltage for 100 runs.

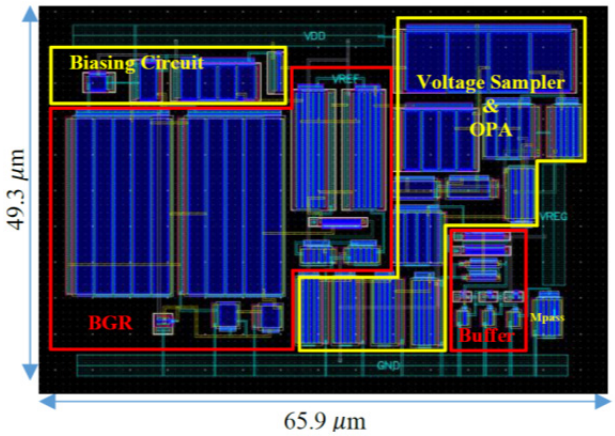

Fig. 17. The proposed circuit layout.

Parameter	This Work	[2]	[3]	[5]
Technology	0.18 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Temperature range (°C)	–15–35	35–45	–20–80	–
Voltage limiting (V)	2	2.9	2	3.1
Current consumption (nA)	32.13	150	120	100
Area ($µm^2$)	3249	–	8832	9048

Tab. 2. The comparison of the proposed DC voltage limiter with the other designed circuits.

Figure 17 indicates the proposed limiter voltage layout with a total area of 3249 $µm^2$. Table 2 shows the specifications of the proposed limiter circuit compared to other circuits. The results show that this circuit has achieved a small area consumption and lower current consumption.

4. Conclusion

This paper presents a low current DC voltage limiter. To generate the reference voltage, a MOSFET transistor in which its body is connected to ground, while the gate, drain and source terminals are connected to a non-zero positive voltage and has a function similar to a diode, has been used as a CTAT voltage generator. Also, in the proposed circuit, two cascaded and differential stages are used as PTAT voltage generators. The used sampling circuit is completely MOSFET and four inverter stages are used as buffer to achieve the ideal I-V characteristic for the limiter. The blocks utilized in this circuit are designed with MOSFET transistors which operate in the sub-threshold region.

The proposed circuit in 0.18 µm CMOS technology generates the reference voltage 0.579 V with a temperature coefficient of 37.2 ppm/°C in the range of –50°C to 50°C.

In this circuit, the limited voltage is about 2 V while the current consumption is attained 32.13 nA. The output voltage changes of the limiter are insignificant versus the temperature variations. In addition, the proposed limiter layout obtained with 3249 $µm^2$.

References

[1] LIN, K., WANG, B., WANG, X., et al. A high-efficient energy harvest chain for ultra-low power passive UHF RFID tags. In *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*. Guilin (China), 2014, p. 1–3. DOI: 10.1109/ICSICT.2014.7021596

[2] FERNANDEZ, E., BERIAIN, A., SOLAR, H., et al. A low power voltage limiter for a full passive UHF RFID sensor on a 0.35 µm CMOS process. *Microelectronics Journal*, 2012, vol. 43, no. 10, p. 708–713. DOI: 10.1016/j.mejo.2012.03.013

[3] LI, S., SHEN, J., LIU, S., et al. A novel voltage limiter circuit for passive RFID tag. In *IET International Conference on Information*

Science and Control Engineering (ICISCE). Shenzhen (China), 2012, p. 1–4. DOI: 10.1049/cp.2012.2400

[4] ZURIARRAIN, X., BERIAIN, A., BISTUÉ, G., et al. A CMOS low frequency analog RFID front-end for the IoT. In *Conference on Design of Circuits and Integrated Systems (DCIS).* Lyon (France), 2018, p. 1–6. DOI: 10.1109/DCIS.2018.8681486

[5] BERIAIN, A., REZOLA, A., DEL RIO, D. A high accuracy 3.1V voltage limiter for enabling high performance RFID sensor applications. In *IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*. Dallas (TX, USA), 2019, p. 973 to 976. DOI: 10.1109/MWSCAS.2019.8885052

[6] LEE, J.-W., VO, D. H. T., HUYNH, Q.-H., et al. A fully integrated HF-band passive RFID tag IC using 0.18-um CMOS technology for low-cost security applications. *IEEE Transactions on Industrial Electronics*, 2011, vol. 58, no. 6, p. 2531–2540. DOI: 10.1109/TIE.2010.2060460

[7] CHUNG, C., KIM, Y.-H., KI, T.-H., et al. Fully integrated ultra-low-power passive UHF RFID transponder IC. In *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. Beijing (China), 2011, p. 77–80. DOI: 10.1109/RFIT.2011.6141789

[8] SALEHI, M. R., DASTANIAN, R., ABIRI, E., et al. A 1.58 nW power consumption and 34.45 ppm/°C temperature coefficient bandgap reference (BGR) for subblocks of RFID tag. *Microelectronics Journal*, 2015, vol. 46, no. 5, p. 383–389. DOI: 10.1016/j.mejo.2015.03.002

[9] NEJADHASAN, S., ZAHERI, F., ABIRI, E., et al. PVT-compensated low voltage LNA based on variable current source for low power applications. *AEU - International Journal of Electronics and Communications*, 2022, vol. 143, no. 5, p. 1–17. DOI: 10.1016/j.aeue.2021.154042

[10] WANG, L., ZHAN, C., TANG, J., et al. A 0.9-V 33.7-ppm/°C 85-nW sub-bandgap voltage reference consisting of subthreshold MOSFETs and single BJT. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2018, vol. 26, no. 10, p. 2190–2194. DOI: 10.1109/TVLSI.2018.2836331

[11] PEREIRA-RIAL, Ó., CARRILLO, J. M., LÓPEZ, P., et al. A 0.6 V, ultra-low power, 1060 μm^2 self-biased PTAT voltage generator for implantable biomedical devices. *AEU - International Journal of Electronics and Communications,* 2021, vol. 137, no. 12, p. 1–8. DOI: 10.1016/j.aeue.2021.153800

[12] WANG, L., ZHAN, C. A 0.7-V 28-nW CMOS subthreshold voltage and current reference in one simple circuit. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2019, vol. 66, no. 9, p. 3457–3466. DOI: 10.1109/TCSI.2019.2927240

[13] PARK, M., PARK, S. M. A CMOS symmetric self-biased voltage reference. *Microelectronics Journal,* 2018, vol. 80, no. 11, p. 28–33. DOI: 10.1016/j.mejo.2018.08.002

[14] HUANG, C., ZHAN, C., HE, L., et al. A 0.6-V minimum-supply, 23.5 ppm/°C subthreshold CMOS voltage reference with 0.45% variation coefficient. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2018, vol. 65, no. 10, p. 1290–1294. DOI: 10.1109/TCSII.2018.2846808

[15] AMINZADEH, H., VALINEZHAD, M. M. 0.7-V supply, 21-nW all–MOS voltage reference using a MOS-only current-driven reference core in digital CMOS. *Microelectronics Journal,* 2020, vol. 102, no. 7, p. 1–10. DOI: 10.1016/j.mejo.2020.104841

[16] ABDOLLAHI, R., BADFAR, E. Harmonics mitigation approach by using pulse-doubling circuit in the AC-DC rectifier. *International Journal of Circuit Theory and Applications,* 2021, vol. 49, no. 8, p. 2436–2452. DOI: 10.1002/cta.2991

[17] SALEHI, M. R., DASTANIAN, R., ABIRI, E., et al. A 147 µW, 0.8 V and 7.5 (mV/V) LIR regulator for UHF RFID application. *AEU - International Journal of Electronics and Communications,* 2015, vol. 69, no. 1, p. 133–140. DOI: 10.1016/j.aeue.2014.08.004

[18] SHRIVASTAVA, A., CRAIG, K., ROBERTS, N. E., et al. A 32nW bandgap reference voltage operational from 0.5V supply for ultra-low power systems. In *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*. San Francisco (CA, USA), 2015, p. 94–95. DOI: 10.1109/ISSCC.2015.7062942

[19] RAYAT, H., DASTANIAN, R. A fully MOSFET voltage reference with low power consumption and high power supply rejection ratio for IoT microsystems. *Jordan Journal of Electrical Engineering*, 2022, vol. 8, no. 2, p. 102–113. DOI: 10.5455/jjee.204-1642106587

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