On the Investigation of Frequency-Related Fingerprints of Meminductor/Capacitor and Their Duals Realized by Circuit Emulators

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Abstract. This article investigates the frequency-related fingerprints of the meminductor/capacitors and their duals realized by the circuit emulators. The direct dependency of the hysteresis loop area on the inverse of operating frequency is an important property of the memristor confirming its resistive memory nature. This work shows that not all such elements (which exhibit hysteresis characteristics) seem to follow this fingerprint on subjected to the sinusoidal current/voltage excitation signal when they are realized by the emulator circuits. It is found that in some cases PHL (Pinched Hysteresis Loop) characteristics of the memcapacitor/inductor and their elements, may seem to create a fallacy in their appearance. Although this behavior is natural (but distinct from the memristor), it does produce some challenges during the measurements of these memelements and non-memelements. The behavior has been demonstrated in the MATLAB generated plots and also verified in the experimental and simulation results obtained for the designed emulators for the memcapacitor/meminductor and their duals. The paper also attempts to propose potential solutions to avoid this delusion perceived in the PHL characteristics of memcapacitor/meminductor and their duals, due to conventional measuring methods.

Keywords

Memelement, memcapacitor, meminductor, PHL

1. Introduction

The memristor was identified as a resistive memory element in 1971 by L. Chua [1]. The main difference, the memristor exhibits from the resistor, is found in the transient *v*-*i* characteristics. The resistor shows a straight line in the *v*-*i* plane passing through the origin, while the memristor displays a hysteresis curve pinched at the origin when subjected to a bipolar signal. Due to this property, the memristor finds uses in a wide range of analog and digital applications. Initially, there were Op-Amp-based realizations available for the memristor [1], but the physical architecture was also reported by HP labs based on the titanium oxide (TiO₂) based structure [2]. This discovery of solid-state memristor attracted circuit designers to realize emulator circuits to achieve the characteristics of HP memristor using active elements [3]. The input impedance function of these emulators is a charge/flux-controlled expression and PHL (Pinched Hysteresis Loop) characteristics are formed in the transient *v-i* plane when the circuit is subjected to a sinusoidal current/voltage input signal. The PHL characteristics is a very important phenomenon exhibited by the memristive element and its mathematical and graphical properties have been investigated for different operating parameters by different researchers [4–9].

In [4], Chua has answered all the popular questions regarding the different transient and static characteristics of the memristor, and also discussed the classifications of memristive systems. An interesting mathematical study has been discussed in [5] regarding some unconventional types of PHL characteristics generated due to some higher-order models of the memristive systems or due to multi-harmonic sinusoidal signals. The use of commercially available memristor IC (developed by Knowm semiconductors), has been shown in the generation of multiple pinch-off characteristics through the application of multi-harmonic signals in [6]. The work discussed in [7] gives some insight into some non-memristive systems, which generate PHL characteristics in the v-i plane, but do not possess the storage feature (like the inverse memristor). A similar kind of study has also been presented in [8]. In [9], a very simple mathematical model has been shown, which can be used to generate the PHL characteristics in the *v*-*i* plane.

The associated fingerprints of the PHL curve have been discussed in [10]. On increasing the operating frequency, the area of the PHL curve must get reduced and at very high frequency this curve approaches a straight line. The PHL is a very important characteristics of the memelements and essential for the measurement/verification of operating frequency range, non-volatility and resistive nature. The switching of the resistance is described by the PHL characteristics of the memristors, which is a requirement of the resistive memories as discussed in [11]. According to the work reported in [12], the area of the PHL curve is directly associated with the memory effect of the corresponding memelement therefore its right evaluation and measurement are important.

Now, since the memristor exhibits the PHL characteristics in the *v*-*i* plane, elements producing the hysteresis between charge (*q*)/flux (ϕ) and voltage (*v*)/current (*i*) must be memcapacitor/inductor [13], [14]. This is the basis for the realization of other memelement emulators. Some popular memelement emulators can be visited in [15–21], in which different PHL curves are shown for the realized memelements plotted in their related basic quantity plane (*v*-*i*, *q*-*v*, and ϕ -*i* respectively).

In [15], a floating and a grounded universal emulator has been presented using multiple second-generation current conveyors (CCIIs). The emulator can be used to realize all three memelements. Another floating memelement interface circuit is reported in [16] by using ICs AD844 and AD633, and some floating passive elements. The different memelement emulators have been given in [17] by using ICs AD844 and AD633 to realize the memristor, meminductor, and memcapacitor, respectively. Another set of three memelement emulators to emulate the memristor, memcapacitor, and meminductor respectively, have been proposed in [18] by employing the CCIIs and OTA (Operational Transconductance Amplifier). A very important design has been proposed in [19] for the emulation of memcapacitor emulator based on a piece-wisely linear constitutive relation of memcapacitive quantities. Some more emulation circuits of meminductor and memcapacitor can be found in [20] based on different active elements. In [21], a charge-controlled meminductor emulator by using Operation Amplifiers (Op-Amps) has been presented.

It is important to discuss that circuit-based realization is the only option to emulate the meminductor/capacitor behavior since physical architectures have not been found for these memelements. The fingerprints found in the memristor PHL, ideally must also be exhibited by the PHL characteristics of other memelements. On increasing the applied signal frequency, memristor behavior approaches a pure resistor with diminishing lobe areas. This property must also extend to other memelements (meminductor and memcapacitor), i.e. at high frequency the exhibited nature by these elements should approach the pure inductive and capacitive behavior. Interestingly, in some cases, when the memelements are realized by the emulator circuits this property is not witnessed in the same way for other memelements and their duals just as we observe in the case of memristor (through a reduction in the PHL lobes area on the rise of applied signal frequency). Now, this unconventionality of these elements as compared to the memristor poses some challenges with regards to the measurement of their different frequency-related parameters. This short article attempts to demonstrate this frequency-affected behavior of these elements through mathematical and graphical explanations and also endeavors to provide a possible solution to avoid the issue of measurement.

2. Dual Lobe Hysteresis in Memelements and Their Duals

As discussed, the emulator circuits have been popular for the realization of memelements. The test signal applied across an emulator is always a voltage or current signal like:

 $i(t) = i_{\rm m} \sin(\omega t) \tag{1}$

$$v(t) = v_{\rm m} \sin(\omega t). \tag{2}$$

For the memristor, we directly plot the characteristics between its voltage and current but in the case of meminductance and memcapacitance, the PHL characteristics are plotted in the flux-current and charge-voltage planes, respectively.

To generate the pinched hysteresis curve on the x-y plane, the mathematical model was discussed in [9], which is shown in (3)

$$y(t) = \left(a + b \int_{0}^{t} x(k) dk\right) x(t)$$
 (3)

Equation (3) is the basis of all the emulators reported in popular works on memelement realization. Equation (3) produces the PHL curve for $x(t) = cos(\omega t)$ which is shown in Fig. 1.

These characteristics can also be plotted between i and dv/dt and, v and di/dt in the case of dual of meminductor and memcapacitor, respectively [22]. Now, if we take (3) into account, we can see that if we are modifying the frequency then it is also affecting the values of linked flux and storage charge associated with the meminductor and memcapacitor, respectively. And, these two are the xaxis quantities, we use for plotting the characteristics. Based on (3), PHL characteristics of the memristor, meminductor and meminductor-dual have been investigated in different cases.

Case 1: Memristor

and

Equation (4) represents the *i*-*v* expression of the flux-controlled memristor:



Fig. 1. Plot obtained by using (3) for a = 0.1, b = 1.

$$i(t) = \left(a + b\int_{0}^{t} v(k) dk\right) v(t).$$
⁽⁴⁾

On applying the voltage signal $v(t) = \cos(\omega t)$, Equation (4) can be modified as:

$$i(t) = \left(a + \left(\frac{b}{\omega}\right)\sin(\omega t)\right)\cos(\omega t)$$
(5)

where *a* and *b* are the memelement coefficients and ω is the operating signal frequency.

The transient i(t)-v(t) plot of the voltage-controlled memristor has been shown in Fig. 2 generated using (5). We see that the PHL curves of the memristor realized by (5), perfectly follow the stated fingerprints (discussed in [9]). Therefore, properly designed emulation circuits based on (5) can be the perfect replacements for physical memristors.

The inconsistencies (in the standard fingerprints) arise in the meminductor/capacitor emulators, which have been described in further cases.

Case 2: Meminductor

In the literature, generally, the flux-controlled and charge-controlled meminductors have been designed, which are discussed below. Here, we have also considered the case of di/dt controlled-dual of meminductor, since it is also an element that produces the PHL characteristics for di/dt input.

(i) Flux-controlled Meminductor

Equation (6) depicts the realization expression used for the flux-controlled meminductor emulators

$$i(t) = \left(a + b \int_{0}^{t} \varphi(m) dm\right) \varphi(t)$$
(6)

where $\varphi(t) = \int_{0}^{t} \cos(\omega k) dk = \frac{\sin(\omega t)}{\omega}$ for applied sinusoi-

dal voltage signal $v(t) = cos(\omega t)$ at the input of an emulator circuit.

Equation (6) can be written as:

$$i(t) = \left(a + \left(\frac{b}{\omega}\right)\frac{(1 - \cos(\omega t))}{\omega}\right)\frac{\sin(\omega t)}{\omega}.$$
 (7)



Fig. 2. Plots obtained by using (5) for a = 0.1, b = 1.



Fig. 3. Plots obtained using (7) for a = 0.001 and b = 1.

Now, since $\sin(\omega t)/\omega$ represents the flux of the input signal applied to the emulator, it must be used as the *x*-axis quantity. But unavoidably, its amplitude is frequency-dependent quantity, and when $i(t)-\phi(t)$ curves are plotted, we obtain the PHL curves as shown in Fig. 3.

From Fig. 3 it can be observed that on increasing the ω value, the horizontal span also decreases, which creates an ambiguity regarding the frequency dependency of lobe areas.

Another interesting thing to notice is that both fluxcontrolled memristors, as well as the meminductor emulators take the same sinusoidal signal as the input but on the x-y plane their PHL curves present a significant difference in their extent, even when the LHS quantity is current (*i*), in both cases (as shown in Fig. 4(a) and (b)). The difference is created due to the x-axis quantity, which is just $\cos(\omega t)$ in the case of memristor (MR), but becomes $\sin(\omega t)/\omega$ for the meminductor (MI).



Fig. 4. PHL curves of FC MI and FC MR plotted at a = 0.01, b = 0.1

A similar type of behavior can also be observed in the charge-controlled memcapacitor (with respect to chargecontrolled memristor), which has the expression as follows:

$$v(t) = \left(a + b \int_{0}^{t} q(k) dk \right) q(t)$$
(8)

where q(t) is the integration of the applied current signal.

Now, taking current i(t) and di(t)/dt as the inputs corresponding to a conventional inductor, we can define the two inductive elements.

(ii) Charge-controlled Meminductor

We can find the $\phi(t)$ -i(t) of a charge-controlled meminductor as follows;

$$\varphi(t) = \left(a + b \int_{0}^{t} i(k) dk \right) i(t) \cdot$$
(9)

On applying $i(t) = \cos(\omega t)$ at the input of the emulator circuit realizing the meminductor expression given in (9). Equation (9) can be written as:

$$\varphi(t) = \left(a + \left(\frac{b}{\omega}\right)\sin(\omega t)\right)\cos(\omega t). \tag{10}$$

Now, as this type of meminductor emulator has i(t) as the x-axis quantity, no unusual behavior of PHL curves with the operating is found in the $\phi(t)$ -i(t) plane. Similarly, the flux-controlled memcapacitor emulator also shows perfect frequency dependency like the memristor emulator.

(iii) Dual of Meminductor

The inductor produces a voltage difference proportional to the change in current with time, which is equivalent to di(t)/dt. Therefore, an element producing the duallobe hysteresis in *v*-d*i*(*t*)/d*t* plane can be defined as:

$$v(t) = (a + bi(t))(di(t) / dt)$$
 (11)

Although, the equivalent inductance, in this case, will be (a + bi(t)), which is representing a current-controlled meminductor, but it must be remembered that i(t) is the integration of applied input di(t)/dt, therefore, Equation (11) becomes a PHL generating function. Such types of elements are non-linear inductors but the theory presented in [22] defines them as the dual of the meminductor (there-



Fig. 5. Plots obtained by using (10) for a = 0.01, b = 0.1.



Fig. 6. Plots obtained by using (12) for a = 0.1, b = 0.1.

fore, equally useful in all non-linear circuit applications of actual meminductor).

Applying $i(t) = \cos(\omega t)$ at the input of the emulator circuit based on (11), Equation (11) can be written as:

$$v(t) = (a + b\cos(\omega t))(-\omega\sin(\omega t)).$$
(12)

By using (12), the *v*-d*i*/d*t* curves are plotted in Fig. 6. Due to $di/dt = -\omega \sin(\omega t)$, the span of PHL curve increases with the frequency ω as shown in Fig. 6 ("–"sign in di/dt is neglected during plotting).

The difference in the transient v-i curves realized by (12) and the current-controlled memristor (with the same coefficients a and b) can be seen in Fig. 7. It can be seen that the horizontal span of the curves generated by (12) is larger by the factor of operating frequency value than that of the memristor.

It can also be understood that the same phenomenon will also be exhibited by such non-linear capacitors (dual of



Fig. 7. Difference between the PHL curves of the memristor and dual of meminductor (dMI) for the coefficients' values of a = 0.1, b = 0.1.

memcapacitor) (with respect to the flux-controlled memristor), which can be defined by the following relationship;

$$i(t) = (a + bv(t))(dv(t) / dt)$$
(13)

with equivalent capacitance to be $C_{\rm M}(t) = (a + bv(t))$.

3. Verification of the Presented Theory

Now, to verify this theory regarding the different types of memelements/non-memelements, the emulation circuits using OTAs and CCII are employed. Figure 8 depicts the meminductor emulator circuit using three OTAs.

The equivalent flux-current relationship of this meminductor emulator is found as;

$$I_{\rm in} = k_3 \frac{g_{\rm m1}}{C_1} \left(\frac{g_{\rm m1} g_{\rm m2}}{C_1 C_2} \rho - V_{\rm SS} - V_{\rm th} \right) \phi \tag{14}$$

where

$$\phi = \int (V_1 - V_2) \mathrm{d}t \tag{15}$$

is the flux and g_{m1} , g_{m2} and g_{m3} are transconductance gains corresponding to OTA1, OTA2 and OTA3 respectively, with k_3 being the gain parameter corresponding to g_{m3} , and

$$\rho = \int_{0}^{t} \phi \, \mathrm{d}t \tag{16}$$

is the time integral of the flux (TIF).

Now, the equivalent inverse meminductance by using (14) can be given as:

$$L^{-1} = k_3 \frac{g_{\rm m1}}{C_1} \left(\frac{g_{\rm m1}g_{\rm m2}}{C_1 C_2} \rho - V_{\rm SS} - V_{\rm th} \right).$$
(17)

Experimental Results:

The presented circuit has been verified through breadboard implementation based on the physical ICs LM13700 which comprises two transconductance stages [23]. Since the proposed circuit requires three OTAs, it can be implemented using two LM13700 ICs along with biasing resistances and two capacitances. In Fig. 9, the breadboard implementation of the realized meminductor emulator has been depicted. The passive element values are



Fig. 8. Flux-controlled meminductor emulator designed using OTAs.





Fig. 9. PHL plots of LM13700 based meminductor traced at the DSO screens: (a) for 1 MHz, (b) for 1.5 MHz.

selected as $C_1 = C_2 = 4.7$ nF and biasing resistances R_1 , R_2 and R_3 are selected as 30 k Ω , 50 k Ω , and 56 k Ω , respectively with power supply voltage as ± 12 V. It can be observed from the plots that on increasing the operating frequency the PHL lobe area, as well as the horizontal span, gets reduced, which is as per the discussed theory of flux-controlled meminductor.

Emulation Circuits for Dual of Memcapacitor and Meminductor:

The emulation circuits for the dual of meminductor and memcapacitor are presented in Fig. 10 and Fig. 11.

On applying the KVL-KCL analysis, the basic relationship between v(t) and i(t) is found as;

$$v_{\rm in}(t) = R_{\rm l}k_0 \left(R_2 i_{\rm in}(t) - V_{\rm SS} - V_{\rm th}\right) \left(L_{\rm l} \, {\rm d}i_{\rm in}(t) / \, {\rm d}t\right) (18)$$

where k_0 is the transconductance parameter of the OTA, $V_{\rm SS}$ is the supply voltage and $V_{\rm th}$ represents the threshold



Fig. 10. A novel realization of meminductor-dual emulator realizing $v(t) = (L_M(t)) (di(t)/dt)$.



Fig. 11. Designed memcapacitor-dual emulator.

voltage of internal CMOS transistors. It can be observed from (18) that this circuit given in Fig. 10 is realizing the dual of meminductor defined by (11). Also, a memcapacitor-dual emulator modeled by (13) has been designed, which is shown in Fig. 11.

On applying the circuital analysis, the equivalent relationship of the realized voltage-controlled memcapacitordual is found as:

$$i_{\rm in}(t) = R_{\rm l}k_0 \left(\frac{C_2}{C_1} v_{\rm in}(t) - V_{\rm SS} - V_{\rm th}\right) \left(C_2 \, \mathrm{d}v_{\rm in}(t) / \,\mathrm{d}t\right) \cdot (19)$$

Now, to verify these designed circuits, the simulations have been performed by using PSPICE for the CMOS implementations of OTA and CCII given in [24], [25]. Figure 12 shows the PHL characteristics of the current-controlled meminductor-dual emulator given in Fig. 11, plotted between the voltage across inductor L_1 , v_{L1} and in-



Fig. 12. Hysteresis curves of the meminductor-dual emulator given in Fig. 10 operated at $R_1 = 1 \text{ k}\Omega$, $R_2 = 50 \text{ k}\Omega$, $L_1 = 1000 \text{ mH}$ with the peak value of the input, $I_P = 9.5 \text{ }\mu\text{A}$.



Fig. 13. PHL behavior of the memcapacitor-dual for sinusoidal input of $V_P = 0.01$ V and $R_1 = 8 \text{ k}\Omega$, $C_1 = 0.01$ nF and $C_2 = 0.075$ nF.

put voltage v_{in} . It can be seen that on increasing applied signal frequency, the span of the PHL curve expands in the horizontal directions. It was also seen in the MATLAB generated plots shown in Fig. 6.

Similarly, the realized voltage-controlled memcapacitor-dual shown in Fig. 11, has also been simulated, whose PHL characteristics are given in Fig. 13.

It should also be mentioned that despite having the PHL characteristics, the non-linear inductors/capacitors do not possess the storage feature just like the memristor.

4. Methods to Measure the PHL Characteristics of Meminductor/Memcapacitor Emulator to Avoid the Discrepancies

In this section, we have depicted an interesting solution to avoid the undesired contradiction observed in the frequency response of the PHL curves of memcapacitor and meminductor emulators. Figure 14 shows a general approach, which is followed to realize a flux-controlled meminductor.

When we plot the ϕ -*i* curve of the realized meminductor, we pick *i*(*t*) from the input and ϕ (*t*) from the output of the integrator. Now, this results in the addition of the integration factor *k*, due to which the actual flux value gets scaled up/down. To avoid this, we can use a multiplier (with a gain of 1/*k*) to remove this factor as shown in Fig. 15. Now, pure ϕ (*t*) i.e. integration of the input can be obtained.

Now, in the case of a sinusoidal signal, integration of the input voltage results in the multiplication of the $1/\omega$ factor, this should also be removed to obtain the pure sinusoidal form of flux $\phi(t)$ independent from the frequency, which can be done by adding one more multiplier (with gain having a numerical value equal to the operating frequency value), as depicted in Fig. 16.



Fig. 14. Concept of realizing flux-controlled meminductor in the conventional circuits.



Fig. 15. Block diagram showing the removal of integration factor from input voltage flux.



Fig. 16. Method to obtain frequency-independent input voltage flux (SG: Signal Generator).

5. Conclusion

The issue discussed in the article is related to the delusion created in the measured transient characteristics of memelements (memcapacitor and meminductor) and their duals realized by the circuit emulators. The emulation circuits always take current/voltage quantities as the input. It is shown that in charge/flux controlled memcapacitor and meminductor emulators, on the application of sinusoidal current/voltage signal, the measured PHL behavior seems to exhibit frequency-related fingerprints contrasting to the memristor. However, this behavior is natural as per the mathematical models, but it does not let us analyze these elements by observing only their PHL plots. In emulator circuits of di/dt and dv/dt dependent dual of memcapacitor and meminductors, on increasing the applied signal frequency the area of the PHL curve is found to be expanded. This behavior has been discussed through the MATLAB simulation results, and verified by the experimental results and PSPICE-generated simulation results. The MATLAB plots show that change in the applied signal frequency also affects the horizontal span of the PHL curve exhibited by the meminductor/capacitor emulators, which is not found in the memristor emulators. Finally, it is clearly shown that these disagreements in the PHL characteristics are only present due to the employed methods of the measurement, the realized nature may have all the desired properties of memelement. These inconsistencies will not be found in the plotted PHL curves if the reported methods are employed for the measurements.

References

- CHUA, L. O. Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory*, 1971, vol. 18, no. 5, p. 507–519. DOI: 10.1109/TCT.1971.1083337
- [2] STRUKOV, D. B., SNIDER, G. S., STEWART, D. R., et al. The missing memristor found. *Nature*, 2008, vol. 453, p. 80–83. DOI: 10.1038/nature06932
- [3] YANG, C., CHOI, H., PARK, S., et al. A memristor emulator as a replacement of a real memristor. *Semiconductor Science and Technology*, 2015, vol. 30, p. 1–9. DOI: 10.1088/0268-1242/30/1/015007
- [4] CHUA, L. O. Everything you wish to know about memristors but are afraid to ask. *Radioengineering*, 2015, vol. 24, no. 2, p. 319–368. DOI: 10.13164/re.2015.0319

- [5] BIOLEK, D., BIOLKOVA, V., KOLKA, Z. Memristor pinched hysteresis loops: Touching points. Part I. In *International Conference on Applied Electronics*. Pilsen (Czechia), 2014, p. 37–40. DOI: 10.1109/AE.2014.7011663
- [6] MAIZOUB, S., ELKAWIL, A. S., PSYCHALINOS, C., et al. On the mechanism of creating pinched hysteresis loop using a commercial memristor device. *International Journal of Electronics and Communication (AEU)*, 2019, vol. 111, p. 1–4. DOI: 10.1016/j.aeue.2019.152923
- [7] BIOLEK, D., BIOLEK, Z., BIOLKOVA, V., et al. About v-i pinched hysteresis of some non-memristive systems. *Mathematical Problems in Engineering*, 2018, p. 1–10. DOI: 10.1155/2018/1747865
- [8] MOUTTET, B. Memresistors and non-memristive zero crossing hysteresis curves. arXiv:1201.2626v3, 2012, p. 1–8.
- [9] ELWAKIL, A. S., FOUDA, M. E., RADWAN, A. G. A simple model of double-loop hysteresis behavior in memristive elements. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2013, vol. 60, no. 8, p. 487–491. DOI: 10.1109/TCSII.2013.2268376
- [10] ADHIKARI, S. P., SAH, M. P., KIM, H., et al. Three fingerprints of memristor. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2013, vol. 60, no. 11, p. 3008–3021. DOI: 10.1109/TCSI.2013.2256171
- [11] CHUA, L. O. Resistance switching memories are memristors. *Applied Physics A*, 2011, vol. 102, p. 765–783. DOI: 10.1007/s00339-011-6264-9
- [12] BIOLEK, D., BIOLEK, Z., BIOLKOVA, V., et al. Computing areas of pinched hysteresis loops of mem-systems in OrCAD PSPICE. *Applied Mechanics and Materials*, 2013, vol. 278–280, p. 1081–1090. DOI: 10.4028/www.scientific.net/AMM.278-280.1081
- [13] DI VENTRA, M., PERSHIN, Y. V., CHUA, L. O. Circuit elements with memory: Memristors, memcapacitors, and meminductors. *Proceedings of the IEEE*, 2009, vol. 97, no. 10, p. 1717–1724. DOI: 10.1109/JPROC.2009.2021077
- [14] YIN, Z., TIAN, H., CHEN, G., et al. What are memristor, memcapacitor, and meminductor? *IEEE Transactions on Circuits* and Systems II: Express Briefs, 2015, vol. 62, no. 4, p. 402–406. DOI: 10.1109/TCSII.2014.2387653
- [15] ZHAO, Q., WANG, C., ZHANG, C. X. A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit. *Chaos*, 2019, vol. 56, p. 1–14. DOI: 10.1063/1.5081076
- [16] YU, D., ZHAO, X., SUN, T., et al. A simple floating mutator for emulating memristor, memcapacitor, and meminductor. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020, vol. 67, no. 7, p. 1334–1338. DOI: 10.1109/TCSII.2019 2936453
- [17] LIU, Y., IU, H. H. Novel floating and grounded memory interface circuits for constructing mem-elements and their applications. *IEEE Access*, 2020, vol. 8, p. 114761–114772. DOI: 10.1109/ACCESS.2020.3004160
- [18] RAJ, N., RANJAN, R. K., KHATEB, F., et al. Mem-elements emulator design with experimental validation and its application. *IEEE Access*, 2021, vol. 9, p. 69860–69875. DOI: 10.1109/ACCESS.2021.3078189
- [19] BIOLEK, D., BIOLKOVA, V., KOLKA, Z., et al. Analog emulator of genuinely floating memcapacitor with piecewiselinear constitutive relation. *Circuits, Systems, and Signal Processing*, 2016, vol. 35, p. 43–62. DOI: 10.1007/s00034-015-0067-8
- [20] ROMERO, F. J., OHATA, A., TORAL-LOPEZ, A., et al. Memcapacitor and meminductor circuit emulators: A review. *Electronics*, 2021, vol. 10, no. 11, p. 1–21. DOI: 10.3390/electronics10111225

- [21] SAH, M, P., BUDHATHOKI, R. K., YANG, C., et al. Charge controlled meminductor emulator. *Journal of Semiconductor Technology and Science*, 2014, vol. 14, no. 6, p. 750–754. DOI: 10.5573/JSTS.2014.14.6.750
- [22] ITOH, M., CHUA, L. Duality of memristor circuits. *International Journal of Bifurcation and Chaos*, 2013, vol. 23, no. 1. DOI: 10.1142/S0218127413300012
- [23] TEXAS INSTRUMENTS. LM13700 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffer. Datasheet. 2015. Available at: https://www.ti.com/lit/ds/symlink/lm13700.pdf
- [24] SEDRA, A., SMITH, K. C. A second-generation current conveyor and its application. *IEEE Transactions on Circuit Theory*, 1970, vol. 17, p. 132–134. DOI: 10.1109/TCT.1970.1083067
- [25] KAEWDANG, K., SURAKAMPONTORN, W. A wide tunable range CMOS OTA. In 5th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology. Krabi (Thailand), 2008, p. 705–708. DOI: 10.1109/ECTICON.2008.4600528

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