

Tunable Balanced-to-Unbalanced In-Phase Power Divider: Theoretical Analysis and Design

Amar Nath YADAV

Dept. of Electronics and Communication Engineering, Indian Institute of Information Technology, Allahabad, India

amarnath@iiita.ac.in

Submitted May 9, 2022 / Accepted August 5, 2022 / Online first October 7, 2022

Abstract. *This paper presents a tunable power divider (PD) which is balanced at the input port and unbalanced at the output ports. This tunable balanced-to-unbalanced (TBU) PD divides the power either equally or in specific ratio by varying capacitance in the circuit. The complete theoretical study is presented for this type of PD. The analysis is based on the impedance matching of all the ports and isolation requirements of the two unbalanced output ports. By changing the capacitance, different power dividing ratio (PDR) can be achieved. The theoretical results are obtained from the design equations of the proposed PD. The reflection coefficient of the unbalanced ports are better than 10 dB with fractional bandwidth of 21.5%. The isolation between the two output unbalanced ports is achieved better than 15 dB with fractional bandwidth of 23.5%. The proposed PD shows the in-phase characteristic between the two output signals.*

Keywords

Tunable power divider, balanced-to-unbalanced, differential mode, microwave circuit

1. Introduction

The beamforming network is the backbone of RF front-end block for providing feeding network to the phased array antennas [1]. In such system, high antenna gain and narrow beam-width in particular direction is obtained by use of a beamforming network. The role of beamforming network is very critical in order to feed the large antenna array with proper magnitude and phase [2].

PD is one of the main component of beam-forming network which divides the power based on the PDR. There are two types of reported PDs based on the phase difference between the output ports. These are in-phase PDs and out-of-phase PDs. PD can be formed using T or Y junction of the waveguide and transmission lines. These PDs show very poor isolation performance between the output ports and it cannot be matched to all the ports as well. E. J. Wilkinson proposed a PD which provides isolation (by connecting

isolation resistor between the output ports) and matched to all the ports [3]. For high power applications, U. H. Gysel proposed a new kind of PD in which heat is transferred to the ground via isolation resistor [4]. Over the years, these two types of PD attracted major attention of research fraternity to enhance the performance in different applications such as multi-band, tunability, N-way power division. The focus of these researches was on the single-ended PDs [5–8].

Nowadays, fully balanced, BTU (balanced-to-unbalanced) and UTB (unbalanced -to-balanced) PDs are much more investigated because of its applications in high speed RF front-end block. All these PDs are designed for a specific PDR [9–15]. Therefore, to achieve different PDR, multiple circuits are required. One can think of PD circuit which can provide the power division for any specific PDR. This type of PD can forgo the requirements of multiple circuits for different PDR. In [16], a fully balanced tunable PD is reported which can provide the tunability. The proposed circuit which provides the tunability function in BTU type PD is the extension of author's previous work [15].

This study presents a new tunable PD which is having a balanced input port and two unbalanced output ports. The proposed PD shows in-phase response between the two output signals. Sections 2 and 3, present the complete theoretical analysis and comparison of results which verifies the design process of the PD, respectively.

2. Theoretical Analysis

The block diagram of the proposed TBU PD is shown in Fig. 1. This is a TBU PD which is having balanced port A (combination of port 2 and 4) at the input and unbalanced ports (port 1 and 3) at the output. Therefore, this PD is a four port network. Transmission line of characteristic impedance Z_1 and electrical length π is connected between the input balanced port. There are two transmission lines of characteristic impedance Z_2 and electrical length θ_1 . The balanced input port is matched to an impedance (R_s) and two output ports are matched with Z_0 ($50\ \Omega$). R_s is an arbitrary balanced port impedance which can be further matched to the $50\ \Omega$. There are two tunable capacitors (C) which makes

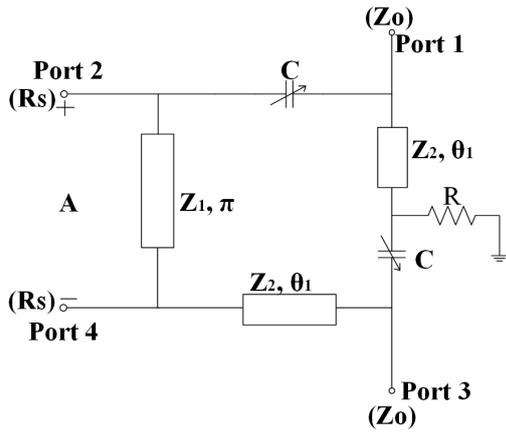


Fig. 1. Block diagram of the proposed TBU PD.

the PD as tunable PD. By varying the capacitance, different PDR can be achieved. The isolation resistor R (one end is connected to the ground) provides the isolation between the two output ports.

2.1 Formulation of Scattering Matrix

In this subsection, mixed-mode S-matrix \mathbf{S}^{mm} has been formulated based on the requirements of the proposed PD. Standard four port scattering matrix \mathbf{S}^{std} has been derived from mixed-mode S-matrix \mathbf{S}^{mm} .

The proposed PD is a reciprocal network. A standard scattering matrix of this PD is given as:

$$\mathbf{S}^{\text{std}} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{22} & S_{23} & S_{24} \\ S_{13} & S_{23} & S_{33} & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix}. \quad (1)$$

Mixed-mode scattering matrix \mathbf{S}^{mm} is used to characterized the balanced circuits which in this case is given in (2).

$$\mathbf{S}^{\text{mm}} = \begin{bmatrix} S_{\text{ddAA}} & S_{\text{cdAA}} & S_{\text{dsA1}} & S_{\text{dsA3}} \\ S_{\text{dcAA}} & S_{\text{ccAA}} & S_{\text{csA1}} & S_{\text{csA3}} \\ S_{\text{sd1A}} & S_{\text{sd3A}} & S_{\text{ss11}} & S_{\text{ss13}} \\ S_{\text{sc1A}} & S_{\text{sc3A}} & S_{\text{ss31}} & S_{\text{ss33}} \end{bmatrix} \quad (2)$$

where S_{sd1A} and S_{sd3A} represent balanced port (A) to unbalanced port (1 and 3) transmission coefficients. S_{sc1A} and S_{sc3A} denote common-mode suppression (CMS) to unbalanced ports 1 and 3. S_{dcAA} , S_{ccAA} and S_{ddAA} represent differential to common-mode conversion coefficient, common-mode reflection coefficient and differential-mode reflection coefficient, respectively. S_{ss11} , S_{ss33} and S_{ss13} are the reflection coefficients of unbalanced ports (1 and 3) and isolation between the ports 1 and 3, respectively.

Based on the requirements of this type of PD given in [9], [12], mixed-mode scattering matrix is obtained and given in (3):

$$\mathbf{S}^{\text{mm}} = \begin{bmatrix} 0 & 0 & \beta e^{j\phi_1} & \frac{\sqrt{1-\beta^2}}{e^{-j\phi_2}} \\ 0 & e^{j\phi_3} & 0 & 0 \\ \beta e^{j\phi_1} & \frac{\sqrt{1-\beta^2}}{e^{-j\phi_2}} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (3)$$

where ϕ_1 , ϕ_2 and ϕ_3 are the phases of mixed-mode scattering parameters. $0 < \beta < 1$ is the transmission coefficient from port A to port 1.

The relationship between mixed-mode scattering matrix \mathbf{S}^{mm} and standard scattering matrix \mathbf{S}^{std} is given in [17]. Using this relationship, mixed-mode scattering matrix given in (3) is converted into standard scattering matrix \mathbf{S}^{std} of four port network.

$$\mathbf{S}^{\text{std}} = \begin{bmatrix} 0 & \frac{\beta}{\sqrt{2}} e^{j\phi_1} & 0 & -\frac{\beta}{\sqrt{2}} e^{j\phi_1} \\ \frac{\beta}{\sqrt{2}} e^{j\phi_1} & \frac{1}{2} e^{j\phi_3} & \frac{\sqrt{1-\beta^2}}{\sqrt{2} e^{-j\phi_2}} & \frac{1}{2} e^{j\phi_3} \\ 0 & \frac{\sqrt{1-\beta^2}}{\sqrt{2} e^{-j\phi_2}} & 0 & -\frac{\sqrt{1-\beta^2}}{\sqrt{2} e^{-j\phi_2}} \\ -\frac{\beta}{\sqrt{2}} e^{j\phi_1} & \frac{1}{2} e^{j\phi_3} & -\frac{\sqrt{1-\beta^2}}{\sqrt{2} e^{-j\phi_2}} & \frac{1}{2} e^{j\phi_3} \end{bmatrix}. \quad (4)$$

2.2 Power Transmission from Balanced Ports

Based on the PDR, input power at the balanced port A is divided into port 1 and 3 and no power is absorbed in the isolation resistor. The equivalent circuit diagram for this analysis is shown in Fig. 2.

Z_{in1} is obtained from Fig. 2 which is given as:

$$Z_{\text{in1}} = Z_0 \parallel \frac{1}{j\omega C} = \frac{Z_0}{1 + j\omega C Z_0}. \quad (5)$$

Z_{in2} is obtained as:

$$Z_{\text{in2}} = Z_2 \frac{Z_L + jZ_2 \tan \theta_1}{Z_2 + jZ_L \tan \theta_1} \quad (6)$$

where Z_{in1} acts as a load:

$$Z_L = Z_{\text{in1}}. \quad (7)$$

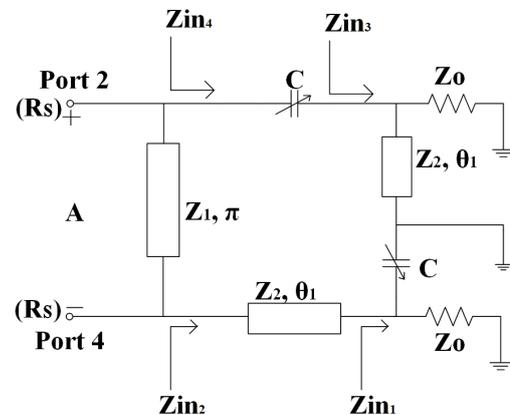


Fig. 2. Power transmission from balanced port to unbalanced ports.

From (5)–(7), Z_{in2} is simplified and obtained as:

$$Z_{in2} = Z_2 \frac{Z_0 + jZ_2(1 + j\omega CZ_0) \tan \theta_1}{Z_2(1 + j\omega CZ_0) + jZ_0 \tan \theta_1}. \quad (8)$$

Z_{in3} is parallel combination of Z_0 and transmission line of characteristic impedance Z_2 terminated with short circuit:

$$Z_{in3} = \frac{jZ_0Z_2 \tan \theta_1}{Z_0 + jZ_2 \tan \theta_1}. \quad (9)$$

Z_{in4} is the series combination of C and Z_{in3} :

$$Z_{in4} = \frac{1}{j\omega C} + \frac{jZ_0Z_2 \tan \theta_1}{Z_0 + jZ_2 \tan \theta_1}. \quad (10)$$

Now, transmission matrix T_{24} between port 2 and port 4 is obtained from Fig. 2.

$$T_{24} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in2}} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{in4}} & 1 \end{bmatrix}, \quad (11)$$

$$T_{24} = \begin{bmatrix} -1 & 0 \\ -\frac{1}{Z_{in2}} & -\frac{1}{Z_{in4}} \end{bmatrix}. \quad (12)$$

From (3), differential reflection coefficient S_{ddAA} is zero.

$$S_{ddAA} = \frac{1}{2} (S_{22} - S_{24} - S_{42} + S_{44}) = 0. \quad (13)$$

The scattering parameters between port 2 and 4 are obtained by applying parameter conversion in (12). Now putting these scattering parameters into (13) leads to the following condition:

$$\frac{1}{Z_{in2}} + \frac{1}{Z_{in4}} = \frac{2}{R_S}. \quad (14)$$

Using (8), (10) and (14), the following equation is obtained.

$$\frac{\frac{Z_2(1+j\omega CZ_0)}{\tan \theta_1} + jZ_0}{\frac{Z_0Z_2}{\tan \theta_1} + jZ_2^2(1 + j\omega CZ_0)} + \frac{j\omega C \left(\frac{Z_0}{\tan \theta_1} + jZ_2 \right)}{\frac{Z_0}{\tan \theta_1} + jZ_2 - \omega CZ_0Z_2} = \frac{2}{R_S}. \quad (15)$$

At the centre frequency, $\theta_1 = \frac{\pi}{2}$, therefore, (15) is further simplified and given in (16).

$$\frac{Z_0}{Z_2^2(1 + j\omega CZ_0)} + \frac{j\omega C}{1 + j\omega CZ_0} = \frac{2}{R_S}. \quad (16)$$

After solving (16), close form of the design equation has been obtained:

$$R_S = 2Z_2 = 2Z_0. \quad (17)$$

From (17), Z_2 is obtained and given in (18).

$$Z_2 = Z_0. \quad (18)$$

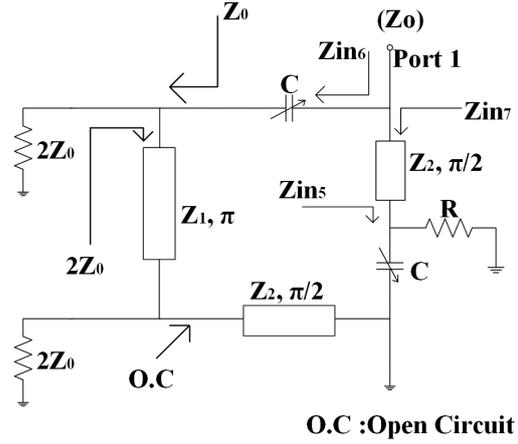


Fig. 3. Equivalent circuit of PD in isolation analysis.

2.3 Isolation Between Output Ports

The two output ports of the PD must be isolated to each other so that signal does not interfere with each other. When port 1 is excited, no signal is obtained at port 3. Based on the analysis done in the previous Sec. 2.2, equivalent diagram of the proposed PD under this analysis is shown in Fig. 3.

Figure 3 shows the impedances at different points of the circuit using properties of quarter and half wavelength transmission lines.

From Fig. 3, Z_{in5} , Z_{in6} and Z_{in7} are obtained:

$$Z_{in5} = R || \frac{1}{j\omega C} = \frac{R}{1 + j\omega CR}, \quad (19)$$

$$Z_{in6} = Z_0 + \frac{1}{j\omega C} = \frac{1 + j\omega CZ_0}{j\omega C}, \quad (20)$$

$$Z_{in7} = \frac{Z_2^2}{Z_{in5}} = \frac{Z_2^2(1 + j\omega CR)}{R}. \quad (21)$$

The parallel combination of Z_{in6} and Z_{in7} is equal to the port impedance Z_0 .

$$Z_{in6} || Z_{in7} = Z_0. \quad (22)$$

Using (20)–(22), isolation resistor R is obtained.

$$R = Z_0. \quad (23)$$

2.4 Power Dividing Ratio

Let the PDR is k^2 . Therefore, the power division from balanced port to unbalanced port is given as:

$$\left| \frac{S_{sd1A}}{S_{sd3A}} \right| = k. \quad (24)$$

From (3) and (4), S_{sd1A} and S_{sd3A} are obtained and given below.

$$S_{sd1A} = \sqrt{2}S_{21}, \quad (25)$$

$$S_{sd3A} = \sqrt{2}S_{23}. \quad (26)$$

From (24)–(26), following relation has been obtained.

$$\left| \frac{S_{sd1A}}{S_{sd3A}} \right| = \left| \frac{S_{21}}{S_{23}} \right| = k. \quad (27)$$

To obtain S_{21} , PD is converted into a two port network between port 2 and 1, all ports are terminated to their port impedances. The equivalent circuit is shown in Fig. 4. S_{21} is obtained by converting admittance matrix between port 2 and 1 into scattering matrix.

As shown in Fig. 4, Path I and Path II are connected in parallel combination, therefore, admittance matrix between port 2 and 1 is obtained.

$$\mathbf{Y}_{21} = \mathbf{Y}_{\text{Path I}} + \mathbf{Y}_{\text{Path II}}. \quad (28)$$

$\mathbf{Y}_{\text{Path I}}$ and $\mathbf{Y}_{\text{Path II}}$ are obtained from their corresponding transmission matrices $\mathbf{T}_{\text{Path I}}$ and $\mathbf{T}_{\text{Path II}}$, respectively.

$\mathbf{T}_{\text{Path I}}$ is obtained from Fig. 4 and given in (29).

$$\mathbf{T}_{\text{Path I}} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{2Z_0} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_0} & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix}. \quad (29)$$

Using (18), (23) and (29), $\mathbf{T}_{\text{Path I}}$ is simplified and given in (30).

$$\mathbf{T}_{\text{Path I}} = \begin{bmatrix} 1 - \frac{j}{\omega C Z_0} & 2Z_0 - \frac{j}{\omega C} \\ \frac{1}{2Z_0} - \frac{j}{2\omega C Z_0^2} & 2 - \frac{j}{2\omega R C} \end{bmatrix}. \quad (30)$$

$\mathbf{T}_{\text{Path II}}$ is obtained from Fig. 4, and given in (31).

$$\mathbf{T}_{\text{Path II}} = \begin{bmatrix} 1 & \frac{1}{j\omega C} \\ 0 & 1 \end{bmatrix}. \quad (31)$$

After converting $\mathbf{T}_{\text{Path I}}$ and $\mathbf{T}_{\text{Path II}}$ into their corresponding admittance matrices and substituting in (28), \mathbf{Y}_{21} is derived.

After converting \mathbf{Y}_{21} into scattering matrix, corresponding parameters are given in (32)–(34).

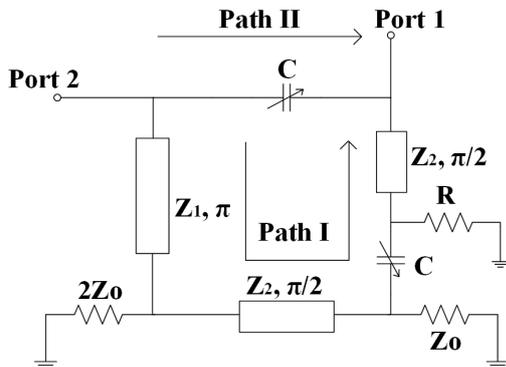


Fig. 4. Equivalent circuit to obtained S_{21} .

$$S_{22} = \frac{-1}{2}, \quad (32)$$

$$S_{21} = S_{12} = \frac{Z_0 \omega C (2Z_0 \omega C - j) (1 + jZ_0 \omega C)}{5Z_0^2 \omega^2 C^2 - 1 + j2Z_0 \omega C (Z_0^2 \omega^2 C^2 - 2)}, \quad (33)$$

$$S_{11} = 0. \quad (34)$$

Two port network between port 2 and 3 is shown in Fig. 5, which is used to obtain S_{23} . All other ports are terminated to their port impedances, as shown in Fig. 5.

To obtain scattering matrix between port 2 and 3, first admittance matrix between port 2 and 3 is obtained and then converted into scattering matrix.

The admittance matrix between port 2 and 3 (\mathbf{Y}_{23}), is the sum of admittance matrix of Path III ($\mathbf{Y}_{\text{Path III}}$) and Path IV ($\mathbf{Y}_{\text{Path IV}}$).

$$\mathbf{Y}_{23} = \mathbf{Y}_{\text{Path III}} + \mathbf{Y}_{\text{Path IV}}. \quad (35)$$

Transmission matrix of Path III, is obtained from Fig. 5.

$$\mathbf{T}_{\text{Path III}} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{2Z_0} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix}. \quad (36)$$

Using (18), (36) is further simplified and transmission matrix between port 2 and 3 is obtained.

$$\mathbf{T}_{\text{Path III}} = \begin{bmatrix} 0 & -jZ_0 \\ -\frac{j}{Z_0} & \frac{-j}{2} \end{bmatrix}. \quad (37)$$

From Fig. 5, transmission matrix of Path IV is obtained.

$$\mathbf{T}_{\text{Path IV}} = \begin{bmatrix} 1 & \frac{1}{j\omega C} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_0} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ \frac{j}{Z_2} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C} \\ 0 & 1 \end{bmatrix}. \quad (38)$$

Using (18) and (23), (38) is further simplified.

$$\mathbf{T}_{\text{Path IV}} = \begin{bmatrix} \frac{2+j\omega C Z_0}{\omega C Z_0} & \frac{2}{\omega C} + j \left(Z_0 - \frac{2}{\omega^2 C^2 Z_0} \right) \\ \frac{j}{Z_0} & \frac{2}{\omega C Z_0} + j \end{bmatrix}. \quad (39)$$

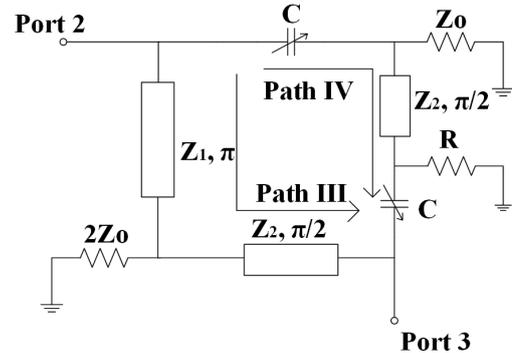


Fig. 5. Equivalent circuit to obtained S_{23} .

Converting transmission matrix of Path III and IV into admittance matrices and using (35), admittance matrix Y_{23} is obtained. Converting Y_{23} into scattering matrix, scattering parameters between port 2 and 3 are derived.

$$S_{22} = \frac{-1}{2}, \tag{40}$$

$$S_{23} = \frac{(1 + j\omega CZ_0)(2\omega CZ_0 - j2 + j\omega^2 C^2 Z_0^2)}{7\omega^2 C^2 Z_0^2 + j4\omega^3 C^3 Z_0^3 - j6\omega CZ_0 - \omega^4 C^4 Z_0^4 - 2}, \tag{41}$$

$$S_{32} = S_{23}, \tag{42}$$

$$S_{33} = 0. \tag{43}$$

Using (27), (33) and (41), relationship between capacitance and PDR is obtained.

$$k = \left| \frac{S_{21}}{S_{23}} \right| = Z_0 \omega C. \tag{44}$$

3. Results

3.1 Theoretical Results

The design equations derived in Sec. 2 are (17), (18), (23) and (44). The transmission line of characteristic impedance Z_1 is of length π , therefore, it is an independent parameter. Z_1 can be chosen based on the microstrip design constrain. Z_0 is taken as 50Ω . The design frequency is taken as 2 GHz.

PDR [k^2]	$R [\Omega]$	$Z_1 [\Omega]$	$Z_2 [\Omega]$	$R_s [\Omega]$	C [pF]
1	50	70.71	50	100	1.59
2	50	70.71	50	100	2.25
3	50	70.71	50	100	2.75
4	50	70.71	50	100	3.18

Tab. 1. Design parameters of TBU PD.

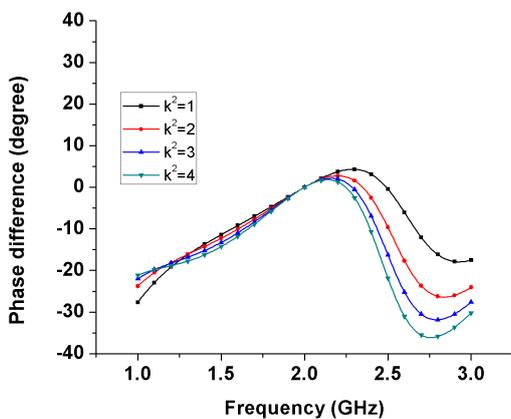


Fig. 6. Theoretical results of phase-difference for different PDR.

Table 1 shows the design parameters based on the design equations obtained in Sec. 2. As shown in Tab. 1, R , Z_1 , Z_2 and R_s are same for different PDR (k^2). Capacitance (C) is the only parameter which changes due to change in PDR. Therefore, by tuning the capacitance (C) value, the proposed PD can divide the power equally or in any specific ratio.

Based on the design parameters listed in Tab. 1, theoretical results are obtained and are shown in Figs. 6 and 7. Figure 6 shows the phase difference between the two output signals (at port 1 and 3). At the center frequency, phase difference is zero and as the frequency increases, variation in the phase difference increases as well. Figure 7(a) shows the return losses of unbalanced ports and isolation between the two output ports. It shows that PD is perfectly matched at the output ports and these ports are isolated with each other. Figure 7(b) shows that balanced port A is matched and the common-mode reflection coefficient of port A is unity. There is no differential-mode to common-mode conversion and vice-versa. Figures 7(c)–(f) show the power division from port A to ports 1 and 3. Figure 7(c) shows that power is divided equally $k^2 = 1$ ($S_{sd1A} = S_{sd3A}$) at the center frequency. Figures 7(d)–(f) show that power is divided according to PDR $k^2 = 2$ ($S_{sd1A} - S_{sd3A} = 3$ dB), $k^2 = 3$ ($S_{sd1A} - S_{sd3A} = 4.77$ dB) and $k^2 = 4$ ($S_{sd1A} - S_{sd3A} = 6.02$ dB), respectively at the center frequency. Figures 7(b)–(f) also show that common-mode signals are perfectly suppressed.

3.2 Simulation Results

Advanced design system (ADS) is used to design the layout of the proposed PD. FR-4 substrate having dielectric constant $\epsilon_r = 4.4$ and thickness $h = 1.6$ mm is used for the micorstrip implementation of the transmission lines. As mentioned in Tab. 1, tunable capacitor is required to achieve proper PDR. A varactor diode (SMV1233-079 (LF)) is used for this purpose.

The complete layout design of the tunable PD is shown in Fig. 8. DC blocking capacitor of 100 pF and 50 pF is used in the circuit. For the biasing circuit RF choke is implemented using high impedance transmission line (100Ω). In order to match the port impedance of balanced port A ($R_s = 100 \Omega$), a quarter-wave transformer of impedance 70.71Ω ($\sqrt{100 \times 50}$) is used in the circuit. Microstrip design equations given in [18] are used to obtain the length and width of the transmission lines. All the dimensions of the microstrip lines which are shown in Fig. 8, summarized in Tab. 3. The DC biasing voltage for different PDR is shown in Tab. 2.

PDR [k^2]	V_{DC} [Volts]
1	5.65
2	3.8
3	3
4	2.55

Tab. 2. Biasing voltage for different PDR.

Dimensions	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}	W_1	W_2	W_3
Values [mm]	8	18.92	11.57	10	8	11	9.5	9.2	11.6	7.4	12	9	3.01	1.56	0.66

Tab. 3. Layout dimensions of the proposed PD.

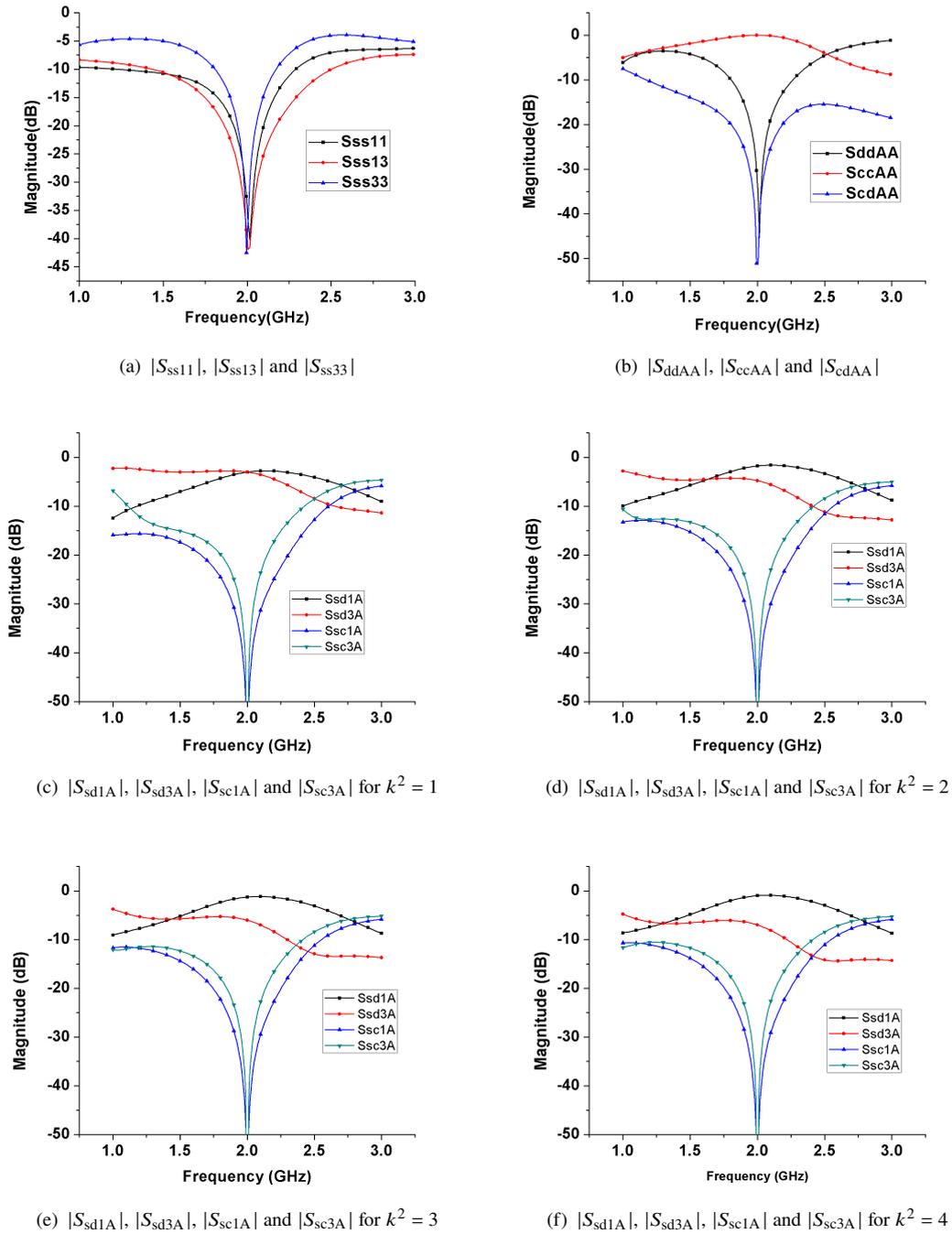


Fig. 7. Theoretical results.

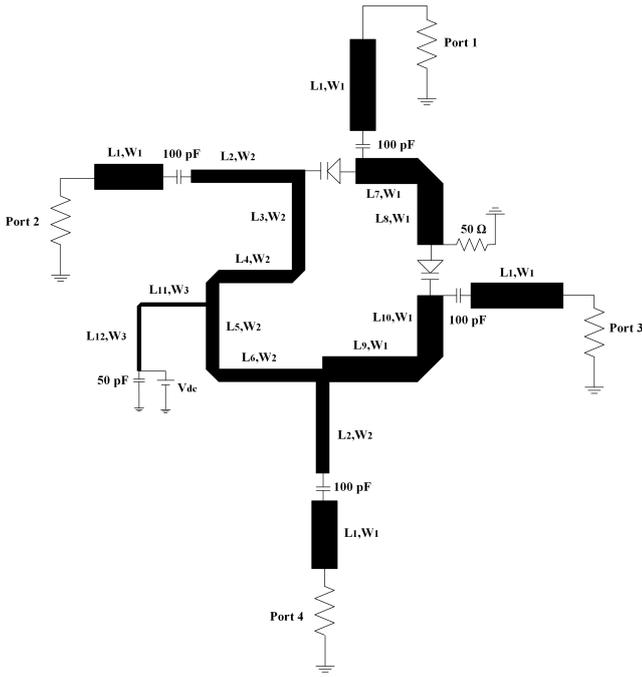


Fig. 8. Layout of the tunble PD.

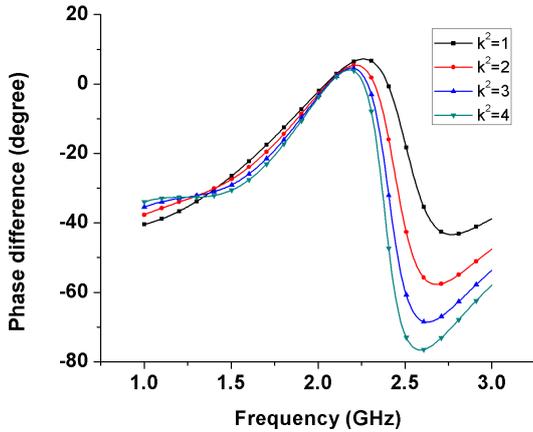


Fig. 9. Simulation results of phase-difference for different PDR.

The simulation results are shown in Figs. 9–10. The phase difference between the two output signals is shown in Fig. 9. At the center frequency, phase difference for $k^2 = 1, 2, 3$ and 4 are $2^\circ, 2.69^\circ, 3.26^\circ$ and 3.70° , respectively. The phase difference increases as frequency increases from 2.35 GHz onward. The variation in phase difference also increase as the change in PDR increases. As shown in Fig. 10(a), return losses of unbalanced ports and isolation between the output ports are better than 20 dB at the center frequency. Differential-mode return loss of port A and differential-mode to common-mode conversion is also better than 20 dB, as shown in Fig. 10(b). The Common-mode reflection coefficient is -0.2 dB at the center frequency. The results shown in Figs. 10(c)–(f) are similar for different PDR. Figures 10(c)–(f) show the power division from balanced port to unbalanced port for PDR $k^2 = 1, 2, 3$ and 4 , respectively. The difference in power division between the output ports at the center frequency for $k^2 = 1, 2, 3$ and 4 are 0.2 dB, 3 dB, 4.7 dB and 5.89 dB, respectively. For all PDR, common-mode suppression is better than 20 dB.

3.3 Results Comparison

The fabricated prototype of the proposed PD and measurement setup is shown in Fig. 11(a) and Fig. 11(b), respectively. The scattering parameters of the unbalanced port are measured using two port VNA E5071C from Agilent Technologies.

The comparison study between the results are shown in Fig. 12. Figure 12(a) shows that results of measured return losses of unbalanced ports and isolation between the output ports are in good match with the simulation results. Figure 12(b) shows that theoretical and simulated results of return loss of balanced port and mode-conversion coefficient are in good match as well. Figure 12 (c)–(f) shows that power division (theoretical and simulated results) from the input balanced port to unbalanced ports follows the similar pattern for PDR $k^2 = 1, 2, 3$ and 4 , respectively.

Table 4 shows the comparison of present work with recent reported works.

Reference	Type of PD	Operating frequency [GHz]	Size [$\lambda_g \times \lambda_g$]	Isolation [dB]	Bandwidth (RL) (unbalanced Ports) [%]
[8]	Unbalanced (filtering)	2.6	$0.0374 (\lambda_g^2)$	NA	NA
[10] (Design II)	BTU	1.88	0.3×1.1	>15	NA
[11]	BTU	1.8	$0.11 (\lambda_g^2)$	>28	37.2 (including all parameters)
[12]	BTU	2	0.73×0.45	>15	38
[13]	BTU	4	0.99×0.73	>15	137
[14] (3 stage)	BTU	1.84	0.56×0.9	>20	62.5
[15]	BTU	2	NA	>15	25
This work	BTU	2	0.82×0.73	>15	21.5

Tab. 4. Comparison of the proposed work with recently reported works.

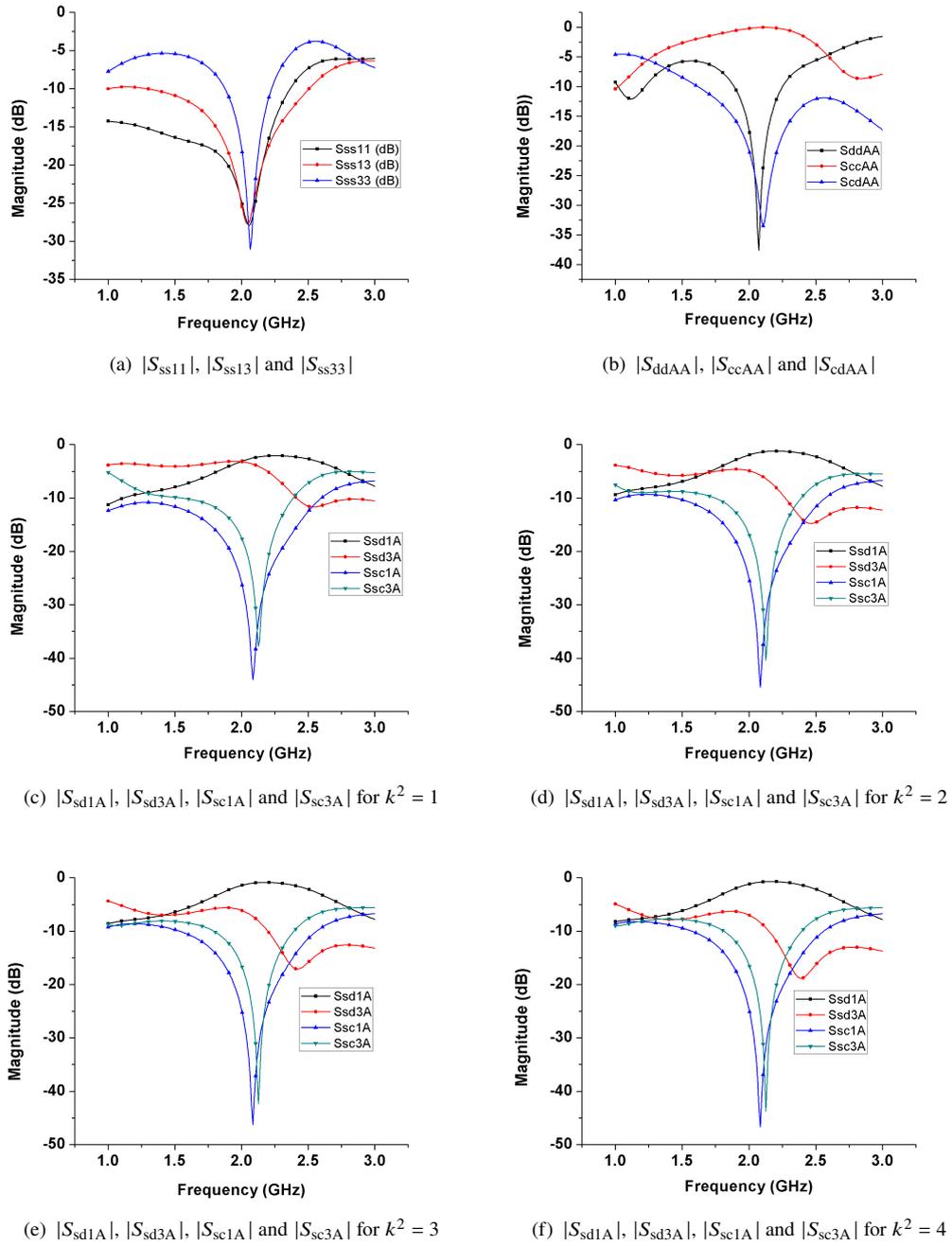


Fig. 10. Simulation results.

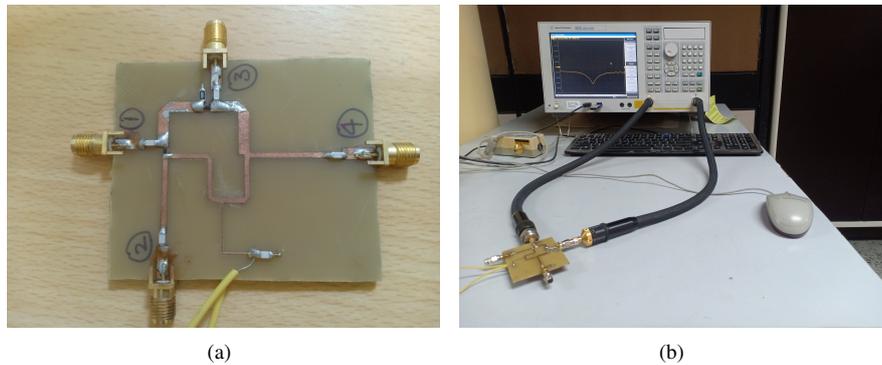
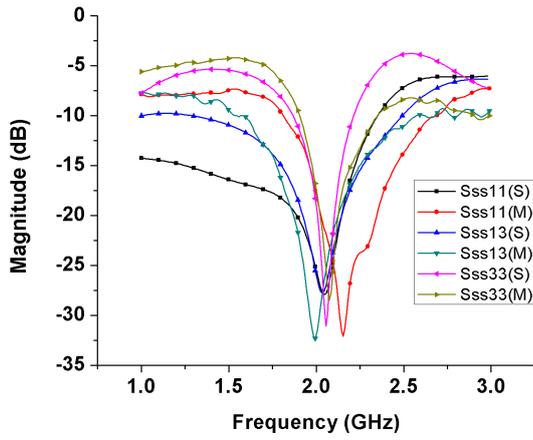
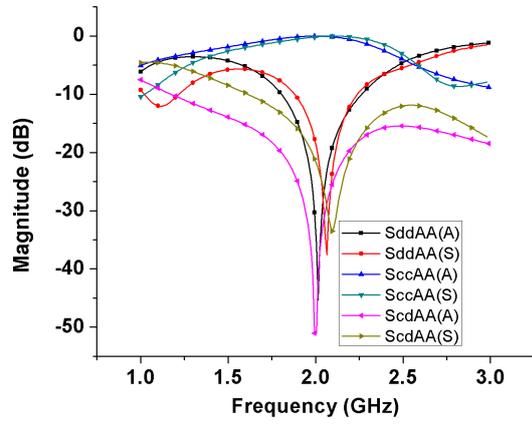


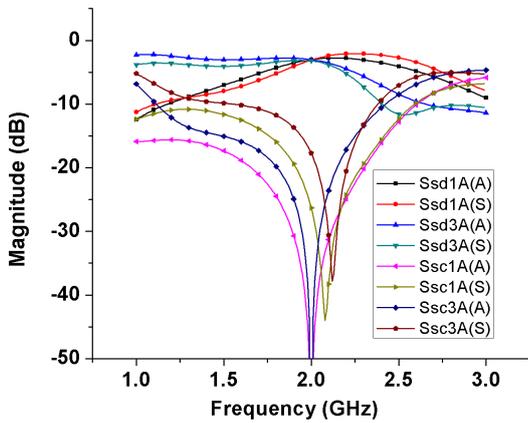
Fig. 11. (a) Fabricated prototype of the TBU PB. (b) Measurement of isolation using two port VNA.



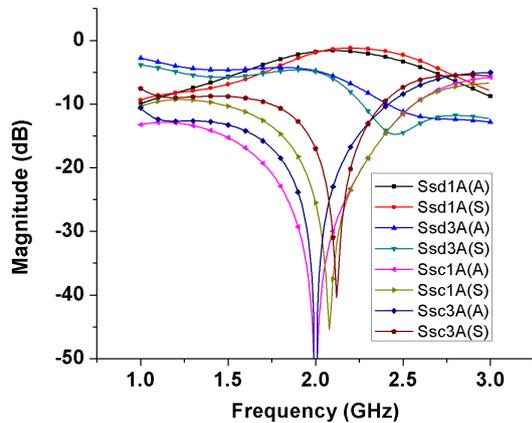
(a) $|S_{ss11}|$, $|S_{ss13}|$ and $|S_{ss33}|$



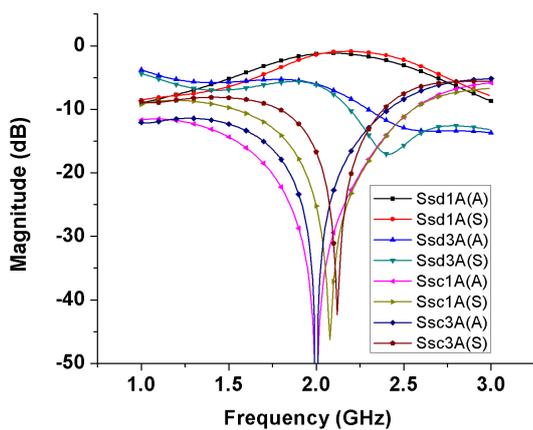
(b) $|S_{ddAA}|$, $|S_{ccAA}|$ and $|S_{cdAA}|$



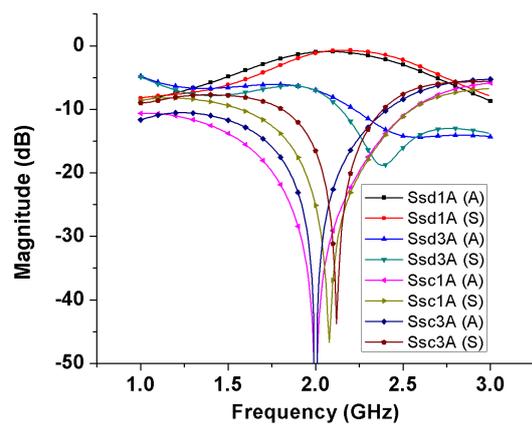
(c) $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ for $k^2 = 1$



(d) $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ for $k^2 = 2$



(e) $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ for $k^2 = 3$



(f) $|S_{sd1A}|$, $|S_{sd3A}|$, $|S_{sc1A}|$ and $|S_{sc3A}|$ for $k^2 = 4$

Fig. 12. Results comparison.

4. Conclusion

This paper presents a novel TBU PD which can divide the power from balanced input port to unbalanced output ports. This PD divide the power in a specific PDR by changing the biasing voltage. The complete theoretical analysis is presented in Sec. 2 for this type of PD. The standard scattering matrix is derived from the constrains of the proposed PD in-terms of mixed-mode scattering parameters. The theoretical analysis is based on the transmission line scattering parameters, transmission parameters and impedance matching of all ports. The analysis of the PD conclude that by changing the capacitance PDR can be changed. This tunable characteristic of the capacitance is achieved by the varactor diode. There is no need to change the transmission line impedance for the change in PDR. The theoretical results shown in Sec. 3 support the analysis of the PD. The circuit simulation is carried out in ADS. A prototype is fabricated and scattering parameters of unbalanced ports are measured using two port VNA. The Comparison of results verified the analysis presented for this PD.

References

- [1] SCHUHLER, M. On evaluation of beamforming networks. *IEEE Antennas and Wireless Propagation Letters*, 2014, vol. 13, p. 766–769. DOI: 10.1109/LAWP.2014.2316542
- [2] LIALIOS, D., ZEKIOS, C. L., GEORGAKOPOULOS, S. V., et al. A mm-wave true-time-delay beamformer architecture based on a blass matrix topology. In *IEEE International Symposium on Antennas and Propagation and North American Radio Science Meeting*. Montreal (QC, Canada), 2020, p. 1609–1610. DOI: 10.1109/IEECONF35879.2020.9329535
- [3] WILKINSON, E. J. An N-way hybrid power divider. *IRE Transactions on Microwave Theory and Techniques*, 1960, vol. 8, no. 1, p. 116–118. DOI: 10.1109/TMTT.1960.1124668
- [4] GYSEL, U. H. A new N-way power divider/combiner suitable for high-power applications. In *IEEE-MTT-S International Microwave Symposium*. Palo Alto (CA, USA), 1975, p. 116–118. DOI: 10.1109/MWSYM.1975.1123301
- [5] WU, L., SUN, Z., YILMAZ, H., et al. A dual-frequency Wilkinson power divider. *IEEE Transactions on Microwave Theory and Techniques*, 2006, vol. 54, no. 1, p. 278–284. DOI: 10.1109/TMTT.2005.860300
- [6] WU, L., YILMAZ, H., BITZER, T., et al. A dual-frequency Wilkinson power divider: For a frequency and its first harmonic. *IEEE Microwave and Wireless Components Letters*, 2005, vol. 15, no. 2, p. 107–109. DOI: 10.1109/LMWC.2004.842848
- [7] LI, J., WANG, B. Novel design of Wilkinson power dividers with arbitrary power division ratios. *IEEE Transactions on Industrial Electronics*, 2011, vol. 58, no. 6, p. 2541–2546. DOI: 10.1109/TIE.2010.2066536
- [8] NWAJANA, A. O., IJEMARU, G. K., ANG, K. L.-M., et al. Unbalanced two-way filtering power splitter for wireless communication systems. *Electronics*, 2021, vol. 10, no. 5, p. 1–9. DOI: 10.3390/electronics10050617
- [9] XIA, B., WU, L. S., REN, S. W., et al. A balanced-to-balanced power divider with arbitrary power division. *IEEE Transactions on Microwave Theory and Techniques*, 2013, vol. 61, no. 8, p. 2831–2840. DOI: 10.1109/TMTT.2013.2268739
- [10] XU, K., SHI, J., LIN, L., et al. A balanced-to-unbalanced microstrip power divider with filtering function. *IEEE Transactions on Microwave Theory and Techniques*, 2015, vol. 63, no. 8, p. 2561–2569. DOI: 10.1109/TMTT.2015.2445051
- [11] ZHANG, W., WU, Y., LIU, Y., et al. A wideband balanced-to-unbalanced coupled-line power divider. *IEEE Microwave and Wireless Components Letters*, 2016, vol. 26, no. 6, p. 410–412. DOI: 10.1109/LMWC.2016.2561400
- [12] YADAV, A. N., BHATTACHARJEE, R. Balanced to unbalanced power divider with arbitrary power ratio. *IEEE Microwave and Wireless Components Letters*, 2016, vol. 26, no. 11, p. 885–887. DOI: 10.1109/LMWC.2016.2615006
- [13] ZHU, Y., SONG, K., FAN, M., et al. Wideband single-ended-to-balanced power divider with intrinsic common-mode suppression. *IEEE Microwave and Wireless Components Letters*, 2020, vol. 30, no. 4, p. 379–382. DOI: 10.1109/LMWC.2020.2973863
- [14] SHI, J., YIN, Z., LU, J., et al. An approach to N-stage balanced-to-single-ended out-of-phase power divider with enhanced operating bandwidth. *IEEE Access*, 2020, vol. 8, p. 13584–13592. DOI: 10.1109/ACCESS.2020.2966490
- [15] YADAV, A. N., BHATTACHARJEE, R. Balanced-to-unbalanced in-phase power divider. In *IEEE MTT-S International Microwave and RF Conference (IMaRC)*. Ahmedabad (India), 2017, p. 1–4. DOI: 10.1109/IMaRC.2017.8449687
- [16] XIAO, Y., LIN, F., MA, H., et al. A planar balanced power divider with tunable power-dividing ratio. *IEEE Transactions on Microwave Theory and Techniques*, 2017, vol. 65, no. 12, p. 4871–4882. DOI: 10.1109/TMTT.2017.2722403
- [17] FAN, W., LU, A., WAI, L., et al. Mixed-mode S-parameter characterization of differential structures. In *Proceedings of the 5th Electronics Packaging Technology Conference (EPTC)*. Singapore, 2003, p. 533–537. DOI: 10.1109/EPTC.2003.1271579
- [18] POZAR, D. M. *Microwave Engineering*. 4th ed., Wiley, 2012. ISBN: 9780470631553

About the Author

Amar Nath YADAV was born in 1986. He received his Ph.D from IIT Guwahati in 2019. His research interests include microwave circuits and antennas. He is working as an Assistant Professor in IIIT Allahabad, India.