An Overview of Fully On-Chip Inductors

Robert ONDICA, Martin KOVAC, Adam HUDEC, Richard RAVASZ,
David MALJAR, Viera STOPJAKOVA, Daniel ARBET

Dept. of IC Design and Test, Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava, Slovakia

robert.ondica@stuba.sk, martin_kovac@stuba.sk, adam.hudec@stuba.sk, richard.ravasz@stuba.sk,
david.maljar@stuba.sk, viera.stopjakova@stuba.sk, daniel.arbet@stuba.sk

Abstract. *This paper focuses on full integration of passive devices, especially inductors with emphasis on multi-layer stacked (MLS) structures of fully integrated inductors using patterned ground shield (PGS) and fully integrated capacitor. Comparison of different structures is focused on the main electrical parameters of integrated inductors (e.g. inductance L, inductance density L_A, quality factor Q, frequency of maximum quality factor F_{Qmax}, self-resonant frequency FSR, and series resistance R_{DC}) and other non-electrical parameters (e.g. required area, manufacturing process, purpose, etc.) that are equally important during comparison of the structures. Categorization of inductor structures with most significant results that was reported in the last years is proposed according to manufacturing process. Final geometrical and electrical properties of the structure in great manner accounts to the fabrication process of integrated passive device. This work offers an overview and state-of-the-art of the integrated inductors as well as manufacturing processes used for their fabrication. Second purpose of this paper is insertion of the proposed structure from our previous work among the other results reported in the last 7 years. With the proposed solution, one can obtain the highest inductance density $L_A = 23.59\,nH/mm^2$ and second highest quality factor $Q = 10.09$ amongst similar solutions reported in standard technologies that is also suitable competition for integrated inductors manufactured in advanced technology nodes.*

Keywords

Fully integrated inductor, fully integrated capacitor, integrated passive device, silicon embedded inductor, air core inductor, magnetic core inductor

1. Introduction

Full integration of an inductor is still considerably challenging task these days. There are plenty of unwanted phenomena occurring during integration of such a device on the chip, which are associated to necessary changes in its geometry. Some compensations of power dissipation in such structures (linked with alterations of the structure geometry) are possible also in standard CMOS technologies. Possibilities to use different materials with connection to special fabrication steps bring interesting results that have been reported in recent years. However, complex fabrication processes still tend to be more expensive that is not always favourable for large scale semiconductor manufacturing.

Usage of Integrated Passive Devices (IPDs) in standard circuits is rising nowadays particularly in Power Management Units (PMUs), Power Management Integrated Circuits (PMICs) and integrated Voltage Regulators (VRs) in general. Another frequent use of inductors is in integrated circuits working in radio frequency region. Voltage regulators based on switching of inductor (or combination of inductor with capacitor) is ideally more efficient than VR based on switching of capacitor [1]. Challenging the current fabrication processes or trying new approaches towards full integration of an inductor is therefore, the essential step in enhancement of electrical properties not only for IPDs but also the whole VR circuits and systems.

In this work, we propose a solution for the full integration of passive devices for integrated voltage regulator already characterized in [2]. This *Multi-Layer Stacked Structure of Fully Integrated Inductor with Patterned Ground Shield* underneath is essential part of a conventional boost converter (CBC) and is applied as the input capacitor and inductor within the voltage regulator. Achieved parameters can be included among the best results from recently published works summarized in this paper. The best results obtained from simulations of the proposed on-chip inductor include: inductance $L = 11.66\,nH$, inductance density $L_A = 23.59\,nH/mm^2$, the maximum quality factor $Q = 10.09$ at frequency $F_{Qmax} = 409.32\,MHz$, series resistance $R_{DC} = 1.75\,\Omega$, and self-resonant frequency $FSR = 920\,MHz$. Similarly, the best parameters of integrated capacitor are the following: capacitance $C = 1.6\,nF$ and capacitance density $C_A = 2.51\,nF/mm^2$. Our structure is the leading solution in terms of inductance density and the second best device in terms of quality factor between similar works in standard technologies, and it represents competition to other works realized in more complex fabrication technologies.

ACI	Air Core Inductor
BEOL	Back End of Line
BiCMOS	Bipolar CMOS
BW	Bandwidth
CBC	Conventional Boost Converter
CMOS	Complementary MOS
DRIE	Deep-Silicon Reactive Ion Etching
EPL	Equal Path Lengths
eSiFO	Embedded Silicon Fan-Out
FBEOL	Far-BEOL
FC	Flip-Chip
FEOL	Front End of Line
FET	Field Effect Transistor
FIVR	Fully Integrated Voltage Regulator
FoM	Figure of Merit
FSR	Self-Resonant Frequency
FOWLP	Fan-Out Wafer-Level Packaging
GP	General Purpose
HIVR	Highly Integrated Voltage Regulator
IC	Integrated Circuit
InFO	Integrated Fan-Out
IPD	Integrated Passive Device
IVR	Integrated Voltage Regulator
MCI	Magnetic Core Inductor
MEOL	Mid End of Line
MOS	Metal Oxide Semiconductor
PGS	Patterned Ground Shield
PMU	Power Management Unit
PMIC	Power Management Integrated Circuit
PTH	Plated Through Holes
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SEI	Silicon Embedded Inductor
SIC	Switched-Inductor-Capacitor
SMMT	Silicon Molded Metal Transfer
SoC	System-on-Chip
SOI	Silicon on Insulator
TGV	Through Glass Via
TSV	Through Silicon Via
VCO	Voltage Controlled Oscillator
VR	Voltage Regulator

Tab. 1. Alphabetical list of used abbreviations.

This paper is organized as follows: In Sec. 2, fully integrated inductors [2–41], reported in years 2015–2022, are categorized firstly by shape and then, by technology used for manufacturing of inductors. Section 3 summarizes results achieved in [2]. Section 4 brings an overview of fully integrated inductors manufactured within the last few years using different fabrication processes and compares them with respect to results presented in [2]. This section also introduces a Figure of Merit (FoM) that can be used for direct comparison of different integrated inductor structures. The last section concludes the performed overview of fully integrated inductors and discuss their comparison. Abbreviations used in this paper are summarized in Tab. 1 in alphabetical order.

2. Categorization of Inductors

Categorization of inductors is proposed for purposes of this work. Several differences in the structure geometry, and used materials and fabrication process can cause significant differences in final electrical parameters of the inductor. During design of the inductor structure (that is commonly made as a custom passive device designed from the bottom), the intended purpose must be taken into account, and suitable process and geometry should be chosen. Influence of the inductor shape was confirmed and reported in [7, 11, 19, 42].

Common shapes of on-chip inductors are the following:

- Stripline   [9, 11, 32, 36, 37],

- Circle Spiral   [6, 19],

- Rectangle   [4, 5, 11–13, 16, 19, 23, 24, 28, 37],

- Octagon   [2, 11, 19, 22, 35],

- 8-Shaped   [7, 15],

- Solenoid   [3, 8, 10, 14, 18–21, 25, 26, 29, 33],

- Toroid   [17, 27, 34].

Enhancing the electrical properties of inductors is often more efficient by using more complex fabrication processes, which on the other hand, tend to be more expensive than standard ones. Non-standard advanced technologies allow creation of passive devices with specifications critical for realization of fully integrated mixed-signal Systems-on-Chip (SoC). Technology process used for manufacturing of IPDs indicates boundaries for electrical parameters of the final structure as well as for its dimensions and shape. Some of processes used for manufacturing of integrated inductors in recent years with outstanding parameters are summarized in Tab. 2. Important feature of each technology is highlighted, and a work example with the highest achieved inductance density L_A is reported. Some of these processes could be combined with each other to further improve properties of inductors. Last column of Tab. 2 shows other works using the inductor integration in the respective technology.

Technological process	Feature	Example result		Other works
Standard General Purpose CMOS	-	$L_A = 150\,\text{nH/mm}^2$ $Q = 8.8$	[7]	[2, 15, 22, 24] [30, 35, 37]
RF Compatible CMOS	Thick Low-Resistive Metal Layers	$L_A = 93\,\text{nH/mm}^2$ $Q = 12.92$	[11]	-
Far-BEOL	Part of the Packaging Process	$L_A = 133.33\,\text{nH/mm}^2$ $Q = 14.5, R_{DC} = 270\,\text{m}\Omega$	[29]	[21]
Silicon on Insulator	High Resistive Substrate	$L_A = 722.22\,\text{nH/mm}^2$ $Q = 40$	[41]	[38–40, 56]
Integrated Fan-Out	Part of the Packaging Process	$L_A = 1.35\,\text{nH/mm}^2$ $Q = 16.57$	[19]	-
Embedded Silicon Fan-Out	Part of the Packaging Process	$L_A = 1.67\,\text{nH/mm}^2$ $Q = 34.68, R_{DC} = 5.1\,\text{m}\Omega$	[5]	[4]
Silicon Embedded Inductor	In Substrate	$L_A = 171.9\,\text{nH/mm}^2$ $Q = 22, R_{DC} = 2.3\,\text{m}\Omega$	[16]	[8, 13, 23]
Through-Silicon-Via	In Substrate	$L_A = 20\,\text{nH/mm}^2$ $Q = 11.5, R_{DC} = 265\,\text{m}\Omega$	[17]	-
Through-Glass-Via	In Substrate	$L_A = 370.15\,\text{nH/mm}^2$ $Q = 16.6$	[33]	[3]
Plated Through Holes	In Substrate	$L_A = 6.25\,\text{nH/mm}^2$ $Q = 33, R_{DC} = 12\,\text{m}\Omega$	[25]	[8]
Silicon Molded Metal Transfer Process	Suspended Over Substrate	$L_A = 8.62\,\text{nH/mm}^2$ $Q = 33, R_{DC} = 121\,\text{m}\Omega$	[6]	-
Bond Wire Inductors	Part of the Packaging Process	$L_A = 5\,\text{nH/mm}^2$	[36]	[37]
Thin Film Magnetic Traces	Magnetic Materials	$L_A = 36.68\,\text{nH/mm}^2$ $Q = 30, R_{DC} = 2\,500\,\text{m}\Omega$	[28]	[9]
Surface Coating	Magnetic Materials	$L_A = 370.15\,\text{nH/mm}^2$ $Q = 16.6$	[33]	[12, 32]
Magnetic Embedded	Magnetic Materials	$L_A = 68.68\,\text{nH/mm}^2$ $Q = 12.71, R_{DC} = 89\,\text{m}\Omega$	[34]	[26]
Core Insertion	Magnetic Materials	$L_A = 354.3\,\text{nH/mm}^2$ $Q = 1.31, R_{DC} = 149.6\,\text{m}\Omega$	[18]	[10, 14, 17, 20, 21] [25, 27, 29, 31]

Tab. 2. Overview of technological processes suitable for integration of inductors.

2.1 Standard Technologies

Standard general-purpose technologies widely used for manufacturing of Integrated Circuits (ICs) have benefits in high yield, reliability, and low cost without significant process variations for a wide variety of commonly manufactured circuits. However, these technologies are less suitable for full integration of inductors due to a lack of thick low-resistivity metal layers, and absence of magnetic materials and high-resistivity substrates. Further scaling of technology associated with thinning of metal and dielectric layers to increase wiring density has results that are opposite to requirements for high-quality integrated inductors [43]. Standard bulk CMOS process usually consists of three consequent stages:

- **Front-end of line (FEOL)** - single crystal of polycrystalline Si wafers in initial stages of processing with possible SiO_2 and Si_3N_4 patterns without exposed metal patterns. Process of creation of transistors, resistors and capacitors in the substrate material with formation of trenches, wells and insluations [44], [45].

- **Mid-end of line (MEOL)** - creation of metal interconnections between gate, source, drain and bulk contacts of transistors [44], [45].

- **Back-end of line (BEOL)** - connection of devices on the chip using metal layers, vias and insulation layers [44], [45].

There is also possibility to enhance electrical properties of IPDs using special layout optimization techniques that can be utilized also in most of the special and more complex manufacturing processes to further enhance electrical properties of on-chip inductors. Such layout optimization techniques include:

- Multi-Layer Stacked Topology (MLS) [2, 46],
- Slicing [2, 47],
- Tapering [2, 38, 40, 48],
- Equal Path Length (EPL) [2, 49],
- Patterned Ground Shield (PGS) [2, 50–52].

2.2 RF Compatible CMOS

Radio Frequency (RF) compatible CMOS processes offer more options for metallization with thick, ultra thick and dual-metal stack layers with low sheet resistance [43]. These features can effectively decrease parasitic serial resistance and suppress unwanted power losses. For example, RF compatible technologies include rf CMOS or Silicon-Germanium Bipolar Complementary Metal-Oxide-Semiconductor (SiGe BiCMOS) technology used in [11].

2.3 Far-BEOL

Far Back-end of line (FBEOL) is an extension of the standard CMOS process by other use of BEOL process stage. New deposited layers on top of the BEOL stack of the chip can form patterns with openings and interconnections similar to the standard BEOL process. These layers can be patterned to form spirals for integrated inductors that can also include magnetic cores. The main purpose here is encapsulation and protection of manufactured chip [53].

2.4 Through-Chip-Via

Creating connections using vertical conductive contacts between bottom and top sides of the substrate (or whole die) is Through-Chip-Via process. Connections are created by deep etching of holes and subsequent deposition of conductive materials into them. Process is commonly used as an alternative to wire bonding, flip-chip (FC) packaging or package-on-package connections [54]. It is also possible to manufacture integrated inductor by deposition of conductive patterns on both sides of substrate and connecting them using conductive holes. Following extension of this process is possible with variations of the used materials or adding more process steps:

- **Through-Silicon-Via (TSV)** - standard Through-Chip-Via process through silicon substrate [54],

- **Through-Glass-Via (TGV)** - silicon substrate is replaced by glass substrate [3], [33],

- **Plated Through Holes (PTH)** - vertical holes plated with a magnetic material [25].

2.5 Silicon on Insulator (SOI)

Power dissipation in the substrate significantly influences performance of integrated devices as well as the whole systems [55]. High resistivity substrates (e.g. glass) can effectively suppress parasitic capacitance between devices placed on the chip and silicon substrate [51], [56].

2.6 Silicon Embedded Inductor

Silicon Embedded Inductor (SEI) is created by insertion of a conductive material into non-conductive silicon substrate that is contacted with on-chip circuitry by Through-Silicon-Via process. Insertion of high resistivity materials into silicon substrate and consequent insertion of metal wiring of the inductor can be suitable step for suppressing capacitive coupling and power losses in substrate.

Inductors can be either embedded in the silicon during special post-CMOS process steps [8, 13, 16, 23] or during Fan-Out Wafer-Level Packaging (FOWLP) process through creating Integrated Fan-Out (InFO) inductors [19]. Similarly, simpler packaging process with small alterations, e.g. Embedded Silicon Fan-Out (eSiFO), was used for creating SEI inductors reported in [4], [5]. This process omits molding and temporary bonding and de-bonding process steps necessary for standard FOWLP, replacing them by less-complicated steps that are part of the FEOL process [57].

2.7 Silicon Molded Metal Transfer Process

Silicon Molded Metal Transfer (SMMT) process can be used for manufacturing of air-core integrated inductors (ACI) suspended over the chip and electrically insulated by air gap. The first part of this process is fabrication of inductor wiring drowned in the silicon trenches created by deep-silicon reactive ion etching (DRIE). Subsequent step is the creation of conducting metal bumps that are later used for interconnecting the inductor to circuitry on the chip. Last step is separation of the silicon mold from the final flip-chip integrated circuit [58].

2.8 Bond Wire Inductors

Essential part of the packaging process of IC fabrication is wire bonding. Common materials used for creating interconnections between chip and its package frame are aluminum, copper, silver and gold [59], [60]. Fundamental parameters of a bond wire include its parasitic resistance and inductance that are frequency dependent, and should always be considered in circuit-level simulations. On the other hand, bond wire inductance can be advantageous when creating integrated inductors.

2.9 Magnetic Alloy Deposition

Implementation of magnetic materials can be suitable step for enhancing electrical properties of integrated inductors. Magnetic materials can effectively increase inductance of a structure and subsequently, also its quality factor. Magnetic materials do not have to necessarily be implemented into the inductor core but can be implemented in the following ways:

- **Thin Film Magnetic Traces** - thin film magnetic materials used for creation of inductor wires [32],

- **Surface Coating** - deposition of magnetic patterns on top of non-magnetic inductor wires [61],

- **Magnetic Embedded** - non-magnetic inductor structure embedded into magnetic substrate [62],

- **Core Insertion** - insertion of a magnetic core into inductor structure during fabrication [18].

Magnetic materials were also used in [25] as part of the through-chip-via process resulting in a new PTH process.

3. Proposed Structure

In our previous work [2], we proposed *Multi-Layer Stacked Structure of Fully Integrated Inductor with and without structure of Patterned Ground Shield* underneath. Geometry modifications were applied to the inductor structure during modelling. All layout optimization techniques mentioned in Sec. 2 (MLS topology, Slicing, Tapering, EPL, and PGS) were applied and obtained results of multi-layer structure with PGS were the following: inductance $L_{f\to 0\,\text{MHz}} = 11.66\,\text{nH}$, the maximum quality factor $Q = 10.09$ at switching frequency $F_{Q\text{max}} = 409.32\,\text{MHz}$, and the minimum series resistance $R_{\text{DC}} = 1.75\,\Omega$. With area required for the integrated inductor of $0.494\,\text{mm}^2$ ($560.65\,\mu\text{m} \times 881.65\,\mu\text{m}$), we achieved high inductance density $L_{\text{A}} = 23.59\,\text{nH/mm}^2$. Integrated inductor was formed by 4-turn structure with 8 slices [47] in each turn, 3 EPL crosses [49], and tapering optimization method with linear step [48]. This structure was realized in three top metal layers offered by a standard general-purpose bulk 65nm CMOS technology provided by UMC foundry: UMC L65N Logic/Mixed-Mode/RF - LL with metallization option 1P8M1T0F1U for mini@sic run [63].

The PGS structure also implemented a fully integrated capacitor. Its capacitance is represented by the oxide capacitance of native MOS FET structure together with capacitance between metallic interconnections. This capacitor was implemented in two bottom metal layers closest to the substrate. Upper M2 metal layer was connected to substrate potential (GND) and served as patterned ground shield for electric field generated by the inductor. Bottom M1 layer was then used as second port of the capacitor. The total capacitance of $1.6\,\text{nF}$ was achieved, and area required for the integrated capacitor was $A_{\text{Cap}} = 0.638\,\text{mm}^2$ ($644.98\,\mu\text{m} \times 989.42\,\mu\text{m}$), thus capacitance density $C_{\text{A}} = 2.51\,\text{nF/mm}^2$ was reported. Structure of the developed integrated inductor with Patterned Ground Shield and integrated capacitor is shown in the Fig. 1.

Insertion of PGS structure between the integrated inductor and substrate caused differences in frequency characteristics. Parasitic parallel capacitance between the integrated inductor and GND potential negatively affected self-resonant frequency (decrease by 15.6%) that is the essential bandwidth (BW) of the device, and also quality factor (decrease by 12.1%). On the other hand, implementation of PGS structure slightly increased inductance at low frequencies $L_{f\to 0\,\text{MHz}}$ by 0.4% and also series resistance R_{DC} by 1.1%. Peaks of quality factor and inductance were also shifted to lower frequencies that is a positive effect considering operation frequency in intended application.

Intended purpose of the structure is its implementation in a fully integrated DC-DC boost converter as a switched inductor and input capacitor. Frequency characteristics (quality factor Q, series resistance R_{DC}, inductance L) of the proposed fully integrated inductor with and without PGS obtained by simulation are shown in Fig. 2 and Fig. 3, respectively. All important parameters of MLS inductor structure with PGS and integrated inductor are summarized in Tab. 3, where a comparison to the most recent and relevant works has been done as well. All results summarized in Tab. 3 are parameters of multi-layer stacked structures of fully integrated capacitor located underneath integrated inductor, and structures were fabricated in different standard general-purpose CMOS technologies and used for on-chip voltage regulation purposes.
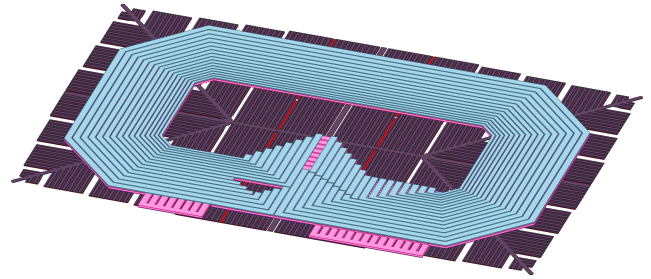

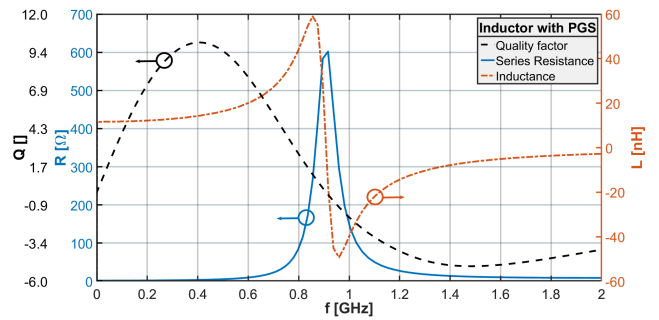**Fig. 1.** Structure of the fully integrated inductor.

Fig. 2. Frequency characteristics of the proposed on-chip inductor with PGS.
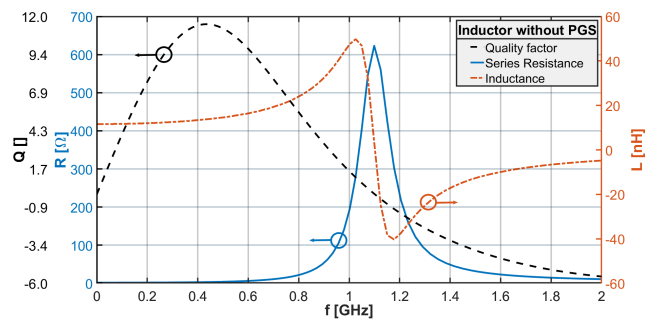

Fig. 3. Frequency characteristics of the inductor without PGS.

Parameter		Our work [2]	[22]	[24]	[35]	[36]	[37]
CMOS technology		65 nm	65 nm	65 nm	180 nm	28 nm	55 nm
Year		2022	2020	2016	2020	2022	2022
Evaluation method		Simulation		Measurement			
Purpose		CBC FIVR	SIC FIVR	Buck FIVR	ReSC Buck FIVR	6-Phase Buck HIVR	2-Phase Buck FIVR
Integrated inductor							
Q_{max}		11.48	10.09	7	16*	-	-	-
$f_{Q_{max}}$	[MHz]	437.55	409.32	450	600*	-	-	-
$L_{f \to 0\,MHz}$	[nH]	11.61	11.66	0.93	3.08	7.7	6×1	2×2
R_{DC}	[Ω]	1.77	1.75	0.16	-	-	-	-
FSR	[GHz]	1.09	0.92	-	2*	-	-	-
L_A	[nH/mm^2]	23.49	23.59	5.17	8.56	2.38	4.58	5
Width $_{Ind}$	[μm]	560.65		-	600	1800	-	-
Length $_{Ind}$	[μm]	881.65		-	600	1800	-	-
Area $_{Ind}$	[mm^2]	0.494		0.181	0.36	3.24	1.31	0.8
Metal layers		M7–M9		Top	M9	M2–M6	Bond Wire	-
Shape		Octagon		Octagon	Square	Octagon	Stripline	Square
Integrated capacitor							
C	[nF]	-	1.6	1.73	1.8	6.8	6	2×2
C_A	[nF/mm^2]	-	2.51	8.72*	5	2.09	4.58	5
Width $_{Cap}$	[μm]	-	644.98	-	600	1800	-	-
Length $_{Cap}$	[μm]	-	989.42	-	600	1800	-	-
Area $_{Cap}$	[mm^2]	-	0.638	0.197*	0.36	3.24	1.31	0.8
Metal layers		-	M1–M2	-	M1–M7	M4–M5	-	-

* - Approximate data

Tab. 3. Comparison of multi-layer stacked structures of fully integrated inductors with capacitors similar to [2].

4. Comparison of the Proposed Structure

Basic comparison of two inductors could be established on quality factor Q of structures. However, comparison based on one parameter could lead to highly misleading conclusions. Other electrical parameters (e.g. inductance L, inductance density L_A, series resistance R_{DC}, self-resonant frequency *FSR*), and non-electrical parameters (e.g. area, fabrication process, and purpose) are equally important for thorough comparison and reliable results.

For example, series resistance R_{DC} of the inductor causes undesired power dissipation and decrease in the circuit efficiency. This parameter is tightly connected to used materials, geometry of the structure, and length and width of conducting wires. Any change in length and width of the conductor has opposite effect on the inductance value than on series resistance. Therefore, integrated inductors should be designed with reasonable compromise between these two parameters, with focus on the final purpose of structure.

On the other hand, a frequency range of the inductor has also high importance. The maximum value of quality factor should be located within the operation frequency range of a circuit. Thus, frequency range of RF circuits (e.g. VCO, RFIC, etc.) will be higher than the operation range of on-chip voltage regulators. Having extremely high frequency of the maximum quality factor $F_{Q_{max}}$ and self-resonant frequency *FSR* would not be useful for voltage regulators working within the frequency range from ones to hundreds of MHz.

4.1 Comparison to MLS Structures with Inductor and Capacitor

Usage of inductor in fully integrated voltage regulators is commonly linked to capacitor usage as well. Since both IPDs occupy large areas, increasing of inductance density and capacitance density are crucial for the area efficiency. One way is to separately increase inductances of both devices. Second option is to create a MLS structure implementing both devices on top of each other to conserve the area further.

Parasitic parallel capacitance between the integrated inductor and substrate $C_{Ind||Sub}$ should be suppressed by any means since it represents causes of power losses in the circuit. Efficient methods to counter the capacitive losses include: using very high-resistivity substrate, very low-resistivity substrate [52], Patterned Ground Shields [50–52] or locating the inductor as far away from the substrate as possible. Parasitic parallel capacitance between the integrated capacitor and substrate $C_{Cap||Sub}$ could also be the reason of further power dissipation in the circuit, especially, when the capacitor is implemented in the circuit as flying device not connected to

the substrate potential. By connecting one port of the capacitor to ground, parasitic parallel capacitance becomes series capacitance that positively increases desired capacitance of the device. Distance of the capacitor from substrate is then of lower importance. Parasitic parallel capacitance between integrated inductor and capacitor $C_{\text{Ind}||\text{Cap}}$ will be then present that might also increase energy losses. This parasitic capacitance could also be suppressed by increasing distance between two IPDs or by implementing a PGS structure in between. Creating a MLS structure of on-chip inductor on top of the integrated capacitor could mean significant space conservation and considerable increase of reactance density.

Our reported inductance $L_{f \to 0\,\text{MHz}} = 11.66\,\text{nH}$ and inductance density $L_A = 23.59\,\text{nH/mm}^2$ are the highest values among the summarized structures reported in recent years. These values are related to the length of conducting paths and number of turns that also increases series resistance R_{DC}. The undesired parasitic resistance is also relatively high in our structure ($R_{\text{DC}} = 1.75\,\Omega$). Best quality factor of the inductor, approximately $Q = 16$ at the switching frequency of $600\,\text{MHz}$ was reported in [24], with the second best inductance density $L_A = 8.56\,\text{nH/mm}^2$. The highest obtained capacitance density of capacitor under the inductor structure - $C_A = 8.72\,\text{nF/mm}^2$ was reported in [22].

4.2 Comparison to Other Inductors

Creating integrated inductor in special technologies, more suitable for inductor integration (i.e. more low-resistivity metal layers, high-resistivity substrates, magnetic materials), could lead to enhancement of inductor electrical properties that is not possible in standard GP CMOS technologies. However, usage of layout optimization techniques turned out to be efficient way to achieve competitive results. Figure 4 shows comparison of series resistance R_{DC} and inductance density L_A of fully integrated inductors. In Fig. 5, a comparison of the maximum quality factor Q_{max} and frequency at maximum quality factor $F_{Q\text{max}}$ of fully integrated inductors is depicted. From the visual comparison of Fig. 4 and Fig. 5, one can observe that our proposed structure is middle-course of all parameters.

The highest inductance density obtained from simulations $L_A = 722.22\,\text{nH/mm}^2$ was reported in $180\,\text{nm}$ RS-SOI technology with 10-turn regular octagon structure in two metal layers. Peak of quality factor reaches values around $Q = 40$ at frequency $F_{Q\text{max}} = 800\,\text{MHz}$ and self-resonant frequency over $2\,\text{GHz}$ [41]. The second best result in means of inductance density achieved in complex advanced technologies is $L_A = 354.3\,\text{nH/mm}^2$ with relatively high series resistance $R_{\text{DC}} = 149.6\,\text{m}\Omega$. The maximum achieved quality factor in this work was $Q = 1.31$ at frequency $F_{Q\text{max}} = 5\,\text{MHz}$ [18]. CMOS-compatible solenoid inductor with a magnetic iron core was in this work embedded in silicon substrate. Another intriguing result was the inductor with inductance density $L_A = 171.9\,\text{nH/mm}^2$ with series resistance $R_{\text{DC}} = 2.3\,\Omega$ and quality factor $Q = 22$ at

frequency $F_{Q\text{max}} = 3.4\,\text{GHz}$, reported in [16]. This Inductor was manufactured as silicon embedded inductor drowned in SU-8 high-resistivity material, which has proven to suppress capacitive losses by more than two orders in comparison to inductor embedded only in silicon.

The lowest series resistance was achieved in InFO inductors with $R_{\text{DC}} = 3.1$–$3.2\,\text{m}\Omega$, inductance density $L_A = 0.61$–$0.78\,\text{nH/mm}^2$ and quality factor $Q = 62.7$–63.9 at frequency $F_{Q\text{max}} = 140\,\text{MHz}$ [19]. Investigated inductor shapes are: rectangle, octagon and circle spiral.

Study of three different solenoid inductors (8, 10 and 12 turns) embedded in four different magnetic materials (HBS1, XVSZ2, XVSZ3 and XVSZ4) resulted in the lowest frequency at which peak values of quality factor Q were achieved, $F_{Q\text{max}} = 300\,\text{kHz}$. Highest obtained quality factor was $Q = 14.38$ with series resistance $R_{\text{DC}} = 49.8\,\text{m}\Omega$ and inductance density $L_A = 67.5\,\text{nH/mm}^2$ with 8-turn structure embedded in XVSZ4. Highest obtained inductance density was $L_A = 68.7\,\text{nH/mm}^2$ with quality factor $Q = 12.71$ and series resistance $R_{\text{DC}} = 89\,\text{m}\Omega$ with 12-turn inductor embedded in the same material. These integrated inductors were designed for use in fully integrated voltage regulators [34].

The highest quality factor of integrated inductor was achieved using Through-Glass-Via method with quality factor up to $Q = 150$ at frequency around $F_{Q\text{max}} = 4.5\,\text{GHz}$. In this fabrication process, solenoid inductor with 24 turns and inductance density of $66.48\,\text{nH/mm}^2$ was fabricated for applications in RF frequency region [3].
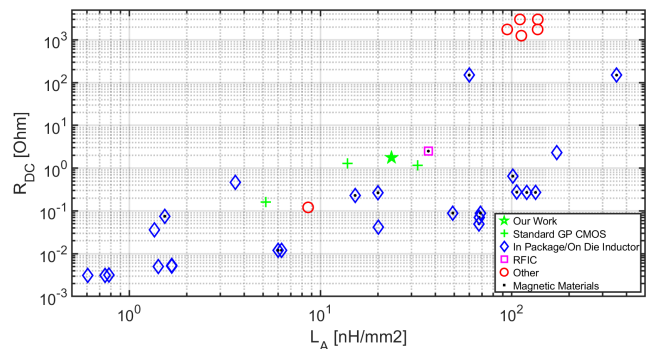

Fig. 4. Comparison of series resistance R_{DC} and inductance density L_A of fully integrated inductors.
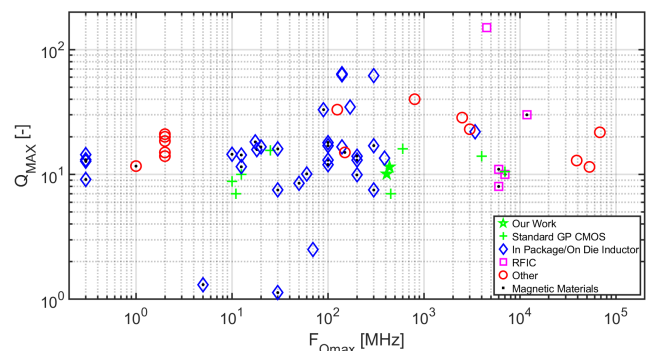

Fig. 5. Comparison of the maximum quality factor Q_{max} and frequency at maximum quality factor $F_{Q\text{max}}$ of fully integrated inductors.

From the comparison reported in Fig. 4 and Fig. 5, the following conclusions can be carried out:

1. With increase in inductance L, the series resistance R_{DC} of structures increases as well. This is caused by the length of inductor wire.

2. With implementation of magnetic materials (thin film magnetic traces, core insertion, surface coating or magnetic embedded), inductance density L_A of the inductor can be effectively increased.

3. Maximum quality factor Q_{max} can be shifted to lower frequencies using magnetic materials.

4.3 Figure of Merit

Another conclusion, resulting from the comparison carried out, is highlighting the best solutions worth considering for future research and design of fully integrated inductors. For this purpose, we propose new Figure of Merit (FoM) aimed for the direct evaluation of analyzed and compared inductor structures. The FoM, which considers the maximum quality factor Q, inductance density L_A, series resistance density R_A at low frequencies (F → 0 Hz), self-resonant frequency FSR, and frequency at the maximum quality factor F_{Qmax}, is given as follows:

$$FoM = \frac{L_A}{R_A} Q_{max} \frac{FSR}{F_{Qmax}} \qquad \left[\frac{nH}{\Omega} \right]. \qquad (1)$$

If Q_{max} is equal to:

$$Q_{max} = \frac{2\pi F_{Qmax} L_{Qmax}}{R_{Qmax}}, \qquad (2)$$

one can also interpret (1) as:

$$FoM = \frac{L_A}{R_A} \frac{2\pi F_{Qmax} L_{Qmax}}{R_{Qmax}} \frac{FSR}{F_{Qmax}} \qquad \left[\frac{nH}{\Omega} \right]. \qquad (3)$$

The FoM is relevant for comparison of any inductors, and its individual parts describe performance of the structure at low frequencies (L_A/R_A), performance at working frequency (L_{Qmax}/R_{Qmax}), and the bandwidth usage effectiveness (FSR/F_{Qmax}). It is important to note that the FoM does not consider fabrication process as a comparative parameter, and the evaluation can be performed only for works with sufficient data available.
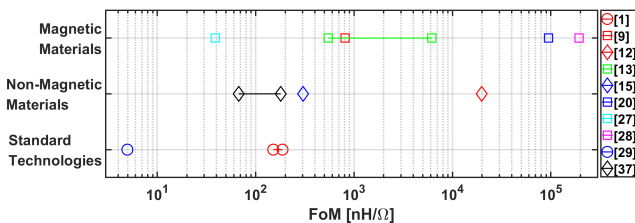

Fig. 6. Visualization of the proposed Figure of Merit for fully integrated inductors.

Comparison of structures, which description is sufficiently accurate and provides all the necessary data for evaluation through the proposed FoM, is visually represented in Fig. 6. From this visualization, we can conclude that our structure [2] achieved higher FoM than the other works realized in standard CMOS technology [30]. Moreover, the FoM evaluation shows that the developed inductor structure is better than some structures fabricated in more complex advanced technologies (e.g. SOI [38] or processes using magnetic materials [28]). The proposed solution was the only one that included a fully integrated capacitor underneath the integrated inductor. All structures within the comparison were fabricated for use in integrated voltage regulators (except structures from [28] and [38]).

The highest FoM was achieved for the solenoid inductor from [29] with a magnetic iron core that was developed for a DC-DC integrated voltage regulator. This result was possible mainly because of extremely high inductance L = 120 nH and relatively high maximum quality factor Q_{max} = 14.5 at low frequency F_{Qmax} = 10 MHz. The frequency BW of this device was also considerable (FSR = 300 MHz). Similar results were reported in [21] for a structure with the second highest FoM.

5. Conclusion

The main aim of this paper was bringing an overview and state-of-the-art of achieved results in integration of inductors in the last few years. Achieved results, reported within years 2015–2022 in [2–41], are compared and conclusion are made. Within this comparison analysis, an overview of technological processes is only logical consequence of the main purpose. Fully integrated inductors are categorized according to process used for manufacturing the structures. Another categorization is made according to common shapes of the inductor structures. Some of the most outstanding results are presented in Sec. 4.2.

For the direct comparison of structures, we introduced a new figure of merit defined by (1) and (3). Using this evaluation method, we consider works [21] and [29] as the best examples of integrated inductor design. Both integrated inductors were designed and fabricated for use in a fully integrated voltage regulator.

Second object of this work is a brief description of electrical parameters of *multi-layer stacked structure of fully integrated inductor with patterned ground shield with fully integrated capacitor* proposed in [2], and their comparison to recent relevant studies. Such structures are designed for use in fully integrated voltage regulators of various topologies and realized in standard general purpose CMOS technologies. This comparison is made in Sec. 4.1 and summarized in Tab. 3. The proposed structure achieved the best results in means of inductance L and inductance density L_A, and second best results in means of quality factor Q amongst the similar structures. In comparison to the other integrated

inductors manufactured in various more complex technological processes, this work achieves middle-coarse of inductance density L_A, series resistance R_{DC}, quality factor Q and frequency at which the peak value of quality factor is located F_{Qmax}. The developed on-chip inductor will be implemented in an integrated DC-DC converter.

Acknowledgments

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About the Authors . . .

Róbert ONDICA received his M.Sc. in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 2019. Since September 2019 he is Ph.D. student at the Institute of Electronics and Photonics of the same institution. His main research interests include low-voltage low-power analog design, ASIC design, energy harvesting, DC-DC conversion and power inductors.

Martin KOVÁČ received his M.Sc. and the Ph.D. degrees in Electronics from Slovak University of Technology in Bratislava, Slovakia in 2013 and 2018, respectively. He is currently a postdoc at Institute of Electronics and Photonics of the same university. His research is focused on low-voltage and low-power analog IC, UWB antenna design, on-chip parametric testing, and energy-efficient RF integrated systems for biomedical applications.

Adam HUDEC received his M.Sc. in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 2019. Since September 2019 he is Ph.D. student at the Institute of Electronics and Photonics of the same institution. His main research interests include digital ASIC design, MPPT algorithms, energy harvesting and DC-DC conversion.

Richard RAVASZ received his M.Sc. in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 2019. Since September 2019 he is Ph.D. student at the Institute of Electronics and Photonics of the same institution. His main research interests include low-voltage low-power analog and digital design, ASIC design and on-chip parametric testing.

David MALJAR received his M.Sc. in Electronics from Slovak University of Technology in Bratislava, Slovakia, in 2019. Since September 2019 he is Ph.D. student at the Institute of Electronics and Photonics of the same institution. His main research interests include low-voltage low-power analog design, ASIC design, digital autocalibration and sigma-delta ADCs.

Viera STOPJAKOVÁ received the M.Sc. and the Ph.D. degrees in Microelectronics from Slovak University of Technology in Bratislava, Slovakia in 1992 and 1997, respectively. Currently, she is a full-time Professor at the Institute of Electronics and Photonics of the same university. She has been involved in more than 20 international and national research projects under different funding schemes. She has published over 200 papers in various scientific journals and conference proceedings; and she is a co-inventor of two US patents in the field of on-chip supply current testing. Her main research interests include IC design and test, low-voltage analog IC design, smart sensors, on-chip energy harvesting and biomedical monitoring.

Daniel ARBET received the M.Sc. degree and Ph.D. degree in Electronics from Slovak University of Technology in Bratislava, Slovakia in 2009 and 2013, respectively. Currently, he is a researcher at the Institute of Electronics and Photonics. He has published more than 80 scientific papers. His main research interests are low-voltage low-power analog and mixed-signal IC design, on-chip parametric testing, analog BIST and voltage conversion.