A Wideband Rectifier Design for Internet of Things (IoT) and Wireless Sensor Network Applications

Aminu Muhammad ABBA [1,5], Tologon KARATAEV [1*], Omotayo OSHIGA [1], Surajo MUHAMMAD [2,5], Jun Jiat TIANG [3*], Nazih Khaddaj MALLAT [4], Aliyu Danjuma USMAN [5]*

[1] Dept. of Electrical and Electronics Engineering, Nile University of Nigeria, 900108, Abuja, Nigeria
[2] Centre for Intelligent Network, Telekom Research & Development (TM R&D), Sdn Bhd, Multimedia University, TM Innovation Centre, Lingkaran Teknokrat Timur, 63000, Cyberjaya, Selangor, Malaysia
[3] Centre for Wireless Technology, CoE for Intelligent Network, Faculty of Artificial Intelligence, Multimedia University, Persiaran Multimedia, 63100, Cyberjaya, Selangor, Malaysia
[4] College of Engineering, Al-Ain University, 64141, Al-Ain, United Arab Emirates
[5] Dept. of Electronics and Telecommunications Engineering, Ahmadu Bello University, 810106, Zaria, Nigeria

aminuabba1055@gmail.com, tologon.karataev@nileuniversity.edu.ng, jjtiang@mmu.edu.my

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Abstract. *This paper presents a compact wideband rectifier for low-power Internet of Things (IoT) and Wireless Sensor Network (WSN) applications, which enables efficient energy harvesting across multiple frequency bands. The proposed wideband rectifier operates efficiently over a broad bandwidth from 0.5–1.4 GHz covering the DTV band, LTE-700, ISM-900, and GSM-900. It employs a Coupled Three-Line Transformer (CTLT) as an impedance matching network to achieve a compact design and robust performance across a wide bandwidth. The circuit uses a voltage doubler configuration with SMS7630 diodes. It was designed, simulated, and validated through fabrication. At 0 dBm, it achieves a Power Conversion Efficiency (PCE) greater than 57% with a 3 kΩ load. The results show that the CTLT matching network can also maintain a high PCE over a wide range of load impedance from 2 to 7 kΩ. The design has a maximum efficiency of 74,2% at 0.65 GHz; it is compact with an electrical size of $0.428\lambda \times 0.037\lambda$, outperforming conventional rectifiers in efficiency and size. This rectifier is well-suited for powering battery-less IoT applications and WSN devices.*

Keywords

Coupled three-line transformer (CTLT), impedance matching network, power conversion efficiency (PCE), radio frequency energy harvesting (RFEH), rectifier, voltage doubler

1. Introduction

Technological advancements have transformed industrial operations. The fifth industrial revolution (Industry 5.0) emphasizes value-driven strategies, integrating human-centric and sustainable technological solutions to achieve social and industrial objectives. It complements Industry 4.0, which is technology-driven. Energy-efficient approaches to autonomous device operation are key enablers for Industry 5.0 [1]. The emergence of the Internet of Things (IoT) has introduced numerous low-power devices into the environment, such as sensor nodes, which are connected through the Internet. By 2025, over 30.9 billion IoT devices are expected to be in use [2], but their reliance on costly batteries with limited capacity necessitates frequent replacement for continuous operation.

Radio Frequency Energy Harvesting (RFEH) offers a sustainable solution by converting ambient RF energy to DC power for IoT and Wireless Sensor Network (WSN) applications [3]. The rectifier is a critical component in an RFEH system. Figure 1 shows a block diagram of an RFEH system, which comprises an antenna, impedance matching network, rectifier, and load.

Rectifiers are classified according to their operating frequency as single-band, multiband, and wideband. The single-band rectifier captures energy from a single frequency of interest and converts it to DC power. This rectifier can achieve high Power Conversion Efficiency (PCE). However, since RF energy is spread across a wide frequency spectrum, the single-band rectifier captures insufficient power for most applications. To improve the harvested power, multiband rectifiers [4–7] or wideband rectifiers [8–10] are employed. Multiband rectifiers comprise an array of single-band rectifiers that combine their outputs or

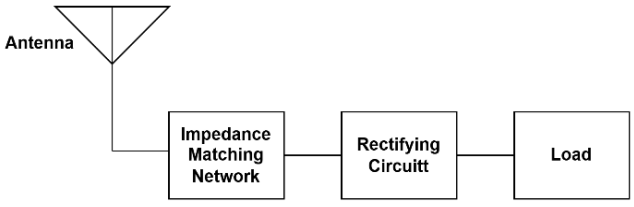

Fig. 1. Block diagram of a Radio Frequency Energy Harvesting (RFEH) system.

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a single circuit tuned to multiple frequencies to achieve increased total power output. Wideband rectifiers capture energy from various sources over a continuous frequency range. Designing efficient wideband rectifiers is more challenging than designing multiband rectifiers because of the non-linear behavior of Schottky diodes [3], [11].

In recent years, the wideband rectifiers have gained significant research attention due to their versatility in applications. In [12], a wideband rectifier based on parallel-shunt diode topology was proposed for energy harvesting in 3G/4G, the ISM band, and biomedical applications. It employs a series transmission line for impedance matching, but has a complex design and low PCE at low input power levels. In [13], a wideband rectifier operating from 1.7 GHz to 2.5 GHz was designed using a voltage doubler topology with an inductor and transmission lines as a matching network. The rectifier offers a simple design but achieves low PCE. In [14], a wideband rectifier for energy harvesting in a frequency range from 1.9 GHz to 2.5 GHz was presented. It utilizes a half-wave topology with transmission lines as a matching network. The rectifier has a complex design with low PCE. A wideband rectifier with an exponential tapered transmission line impedance matching network was reported in [15]. The rectifier has a fractional bandwidth of 194% with a maximum efficiency of 68.8% at 21 dBm input power. The rectifier in [16] achieved a PCE greater than 50% in a frequency range from 0.39 GHz to 2.90 GHz using a multi-stage matching network. In [17], a rectifier using an impedance compression circuit was proposed with a PCE over 50% from 0.33 GHz to 2.61GHz.

Most existing wideband rectifiers rely on complex impedance matching networks, requiring high input power and specific loads. Different wideband matching networks include: transmission lines [12–14], tapered lines [15], and multi-stage matching network [16]. Hence, there is still a need to design efficient and compact wideband rectifiers that are suitable for ambient energy harvesting.

The Coupled Three-Line Transformer (CTLT) was used in [18] as an impedance transformer for wideband impedance transformation (50-170 Ω). The use of CTLT for rectifier impedance matching is underexplored, offering new opportunities for compact, efficient designs.

This paper proposes a novel wideband rectifier that utilizes a Coupled Three-Line Transformer (CTLT) as an impedance matching network for the 0.5–1.4 GHz frequency range. The 0.5–1.4 GHz range covers key RF bands such as the DTV, LTE-700, GSM-900, and ISM-900. The CTLT enables a simple, compact design with high PCE, wideband impedance transformation and stable performance over varying loads. The main contribution of this work is the use of a CTLT as an impedance matching network for a high efficiency, and compact wideband rectifier design. Section 2 presents the theoretical analysis of the CTLT, Section 3 details the design methodology of the wideband rectifier. Section 4 discusses the results of the fabricated wideband rectifier and compares its performance with other wideband rectifiers in the literature, followed by the conclusion in Sec. 5.

2. Coupled Three-Line Transformer

The coupled three-line transformer (CTLT) is widely used in microwave and RF circuits for applications such as impedance matching [18], wideband filters [19], [20] and couplers [21], [22]. Unlike the conventional quarter-wave transformer, which is limited to narrowband impedance matching, the CTLT offers greater flexibility and a compact structure for wideband impedance matching due to its multiple design parameters.

The CTLT is a six-port network consisting of three symmetric coupled lines, each of length l as shown in Fig. 2 [18]. The outer lines have width, w_1, the middle line has width, w_2 and a gap S separating adjacent lines. The length l is a quarter-wavelength at the center frequency. The CTLT transforms the load impedance Z_L to the source impedance Z_S.

The CTLT, implemented on a microstrip, supports three quasi-TEM propagation modes (a, b, and c). Each line i of the CTLT has a modal impedance Z_{0ik} (i = 1,2,3 and k = a,b,c).The impedance matrix CTLT is a 6×6 matrix, which depends on the modal impedances Z_{0ik}, and electrical lengths (θ_a, θ_b, θ_c) determined by the microstrip geometry of the CTLT (l, w_1, w_2, S).

3. Design Methodology

This section presents the proposed rectifier design. The circuit diagram of the proposed wideband RF rectifier using a CTLT transformer as an impedance matching network is shown in Fig. 3.

The source impedance of the RF input is 50 Ω. The rectifier comprises a voltage doubler, a matching network, and a load designed to operate efficiently for 0.5–1.4 GHz. The impedance matching is achieved through a series inductor and a CTLT. The design methodology flow chart is shown in Fig. 4.

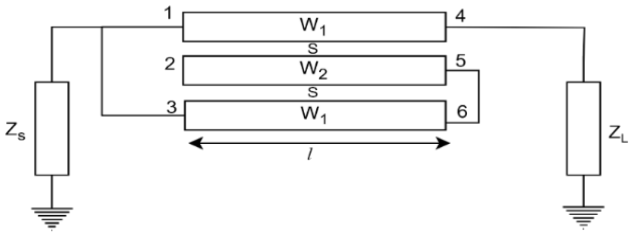


Fig. 2. Schematic diagram of a coupled three-line transformer.

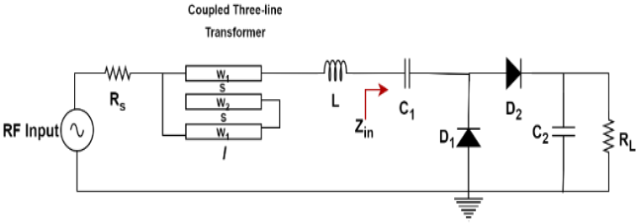


Fig. 3. Schematic diagram of the proposed wideband rectifier.

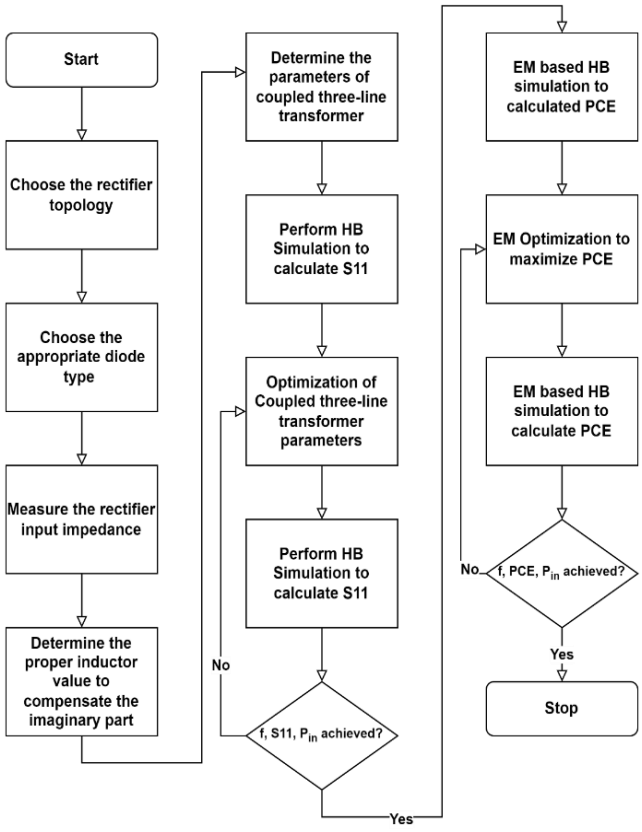


Fig. 4. Flow chart of the wideband rectifier design methodology.

3.1 Voltage Doubler

The voltage doubler consists of an SOT-23 package (which includes two SMS7630 diodes), a DC block capacitor C_1, and a DC pass filter C_2. SMS7630 diode from Skyworks was selected as the rectifying element due to its high saturation current, low emission coefficient, and low junction capacitance [23]. The capacitors C_1 and C_2 are properly selected to be as high as possible to minimize the ripple effect during rectification, subject to availability of Murata components. The values of each capacitor were chosen as 100 nF. Advanced Design System (ADS) was used for the simulation. Source-pull simulation was performed to determine the load that can provide the optimal efficiency across the rectifier operating frequencies. The optimal load of the rectifier design is found to be 3 kΩ. The voltage doubler converts RF signals into DC signals by full-wave rectification. The voltage doubler operates as follows: during the negative wave cycle, D_1 conducts and charges capacitor C_1 whereas, on the positive wave cycle D_2 conducts and charges capacitor C_2. The voltage across the first capacitor V_{c1} and the output voltage V_{out} are calculated as [24]:

$$V_{c1} = V_{in} - V_{th1}. \tag{1}$$

At the output

$$V_{out} = V_{c2} = 2V_{in} - V_{th1} - V_{th2}. \tag{2}$$

where V_{in} is the RF input signal, V_{th1} and V_{th2} are the threshold voltages for D_1 and D_2, respectively.

The rectifier input impedance depends on the RF input power P_{in}, operating frequency f, diode non-linear impedance Z_d and the load R_L

$$Z_{in} = \mathrm{f}\left\{P_{in}, f, Z_d, R_L\right\}. \tag{3}$$

The input impedance of the voltage doubler connected to the load was measured using Harmonic Balance (HB) simulation in ADS. Figure 5 shows the rectifier input impedance against frequency when P_{in} = 0 dBm and R_L = 3 kΩ. The rectifier has a complex and non-linear input impedance including capacitive reactance. It can be observed from Fig. 5 that the real part of the input impedance decreases from 128 Ω at 0.5 GHz down to 23 Ω at 1.4 GHz. The imaginary part of the input impedance also decreases in magnitude from 247.96 Ω at 0.5 GHz to 21.8 Ω at 1.4 GHz.

As it was shown in [18], the CTLT offers a wideband matching for only real valued impedances. However, due to the complex input impedance of the rectifier, it is necessary to minimize the capacitive reactance. Hence, an inductor is connected in series to the input of the rectifier. The value of the inductor is carefully selected to reduce the effect of the capacitive reactance at the center frequency which is 0.95 GHz.

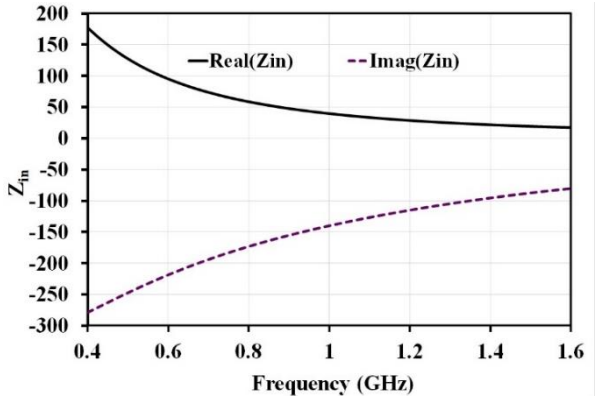


Fig. 5. Rectifier input impedance against frequency.

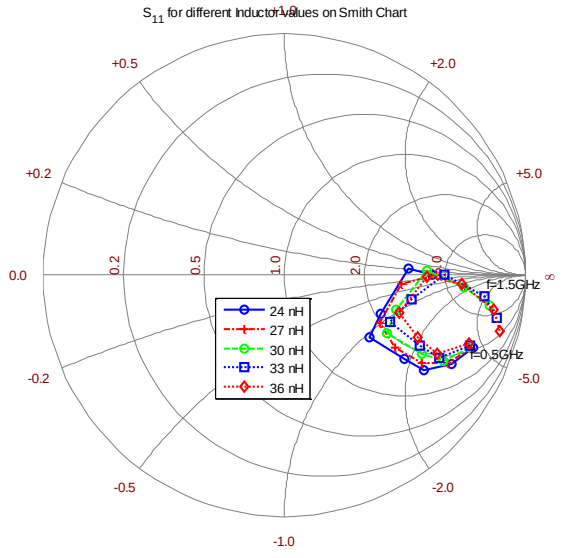


Fig. 6. S_{11} for different inductor values on Smith chart.

L (nH)	$\lvert S_{11}\rvert$ (0.95 GHz) (dB)	S_{11} (0.95 GHz) (Mag∠Phase)	Z_{in} (0.95 GHz) (Ω)
24	–4.35	0.61∠–35.02°	84.5 – j93
27	–5.2	0.55∠–33.1°	91.5 – j78.5
30	–6.21	0.49∠–29/66°	97.75 – j62.25
33	–6.39	0.48∠–23.82°	109 – j54.9
36	–5.97	0.5∠–17.98°	126 – j52.45

Tab. 1. $\lvert S_{11}\rvert$, S_{11} and Z_{in} for different inductor values on Smith chart.

From Fig. 5, the input impedance at the center frequency, Z_{in}(0.95 GHz) = (43.67 – j147.64) Ω. Given the reactance, the value of the inductor is obtained analytically as 24.7 nH. Using this inductor value and employing available inductors from Murata components, several simulations were carried out in ADS to determine the optimal inductor value. Figure 6 shows the S_{11} for different inductor values on Smith chart. The $\lvert S_{11}\rvert$, S_{11} and Z_{in} at the center frequency for different inductor values are shown in Tab. 1. It can be observed that the inductors with 30 nH and 33 nH have the best $\lvert S_{11}\rvert$ and S_{11} response at center frequency compared to the other inductors.

3.2 Wideband Impedance Matching Network

To achieve a wideband performance, the matching network combines an inductor and a CTLT. The CTLT provides a wideband performance at the center frequency. The circuit is designed on a 0.762 mm-thick (h = 0.762 mm), Taconic RF-35 substrate, with a relative dielectric electric ε_r = 3.5 and a loss tangent tanδ = 0.0018. The performance of the transformer depends on the values of l, w_1, w_2, and S. The length l of CTLT is determined at the quarter wavelength of the center frequency (0.95 GHz) as 47.7 mm, while the gap S is set at 0.2 mm (for maximum bandwidth, S is chosen as small as possible). Increasing the bandwidth of the proposed structure would correspondingly demand both the increment of the width and the decrement of the gaps, as well as minimum adjustment of w_1, where $w_2 > w_1$ [18]. Based on this, w_2 and w_1 are chosen to be w_1 = 0.3 mm, w_2 = 0.6 mm as a starting point.

The inductor values of 24 nH, 27 nH, 30 nH, 33 nH and 36 nH from Murata components are simulated along with CTLT to determine the optimal value of the inductor based on the rectifier design bandwidth. Figure 7 shows the corresponding $\lvert S_{11}\rvert$ response against frequency for different inductor values.

It can be observed from Fig. 7 that, among the different inductors, the 30 nH outperforms the other inductors in terms of bandwidth and maximum $\lvert S_{11}\rvert$. One reason that the value of the inductor changed from theoretically calculated value to 30 nH could be that the Murata inductor model presents real-world components with parasitic components.

The plot of $\lvert S_{11}\rvert$ against frequency of the rectifier with a series connected 30 nH inductor only, CTLT only and that

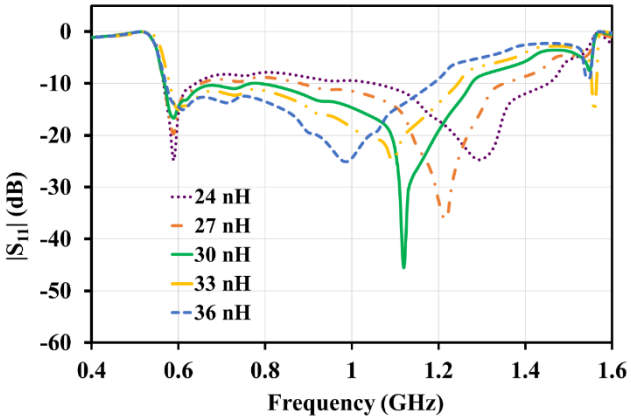


Fig. 7. Simulated $\lvert S_{11}\rvert$ of the rectifier against frequency for different inductor values combined with CTLT.

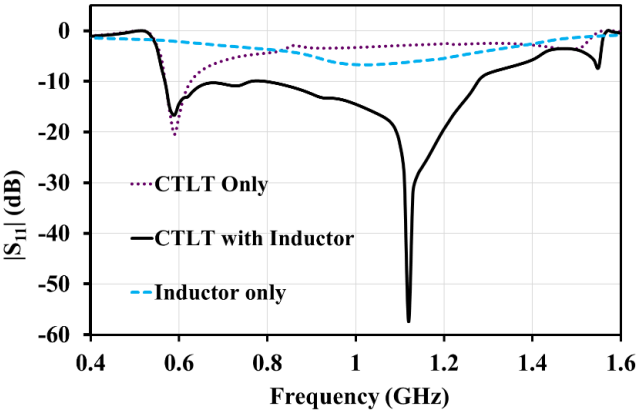


Fig. 8. Simulated $\lvert S_{11}\rvert$ of the rectifier against frequency.

of series 30 nH inductor along with CTLT is shown in Fig. 8. It can be observed that the inductor only and the CTLT only responses exhibit a narrowband response, while the inductor along with CTLT provides a wideband performance with a good $\lvert S_{11}\rvert$ response.

The CTLT parameters were circuit optimized using gradient optimization in ADS to ensure $\lvert S_{11}\rvert \leq -10$ dB at 0 dBm input power across the design frequencies of 0.5–1.4 GHz. The optimized values are: l = 50.58 mm, w_1 = 0.23 mm, w_2 = 1.95 mm and S = 0.47 mm. It can be ob-

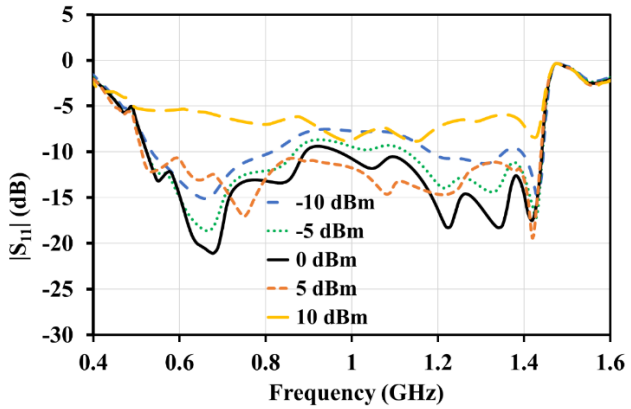


Fig. 9. Simulated $\lvert S_{11}\rvert$ of the rectifier against frequency at different P_{in}.

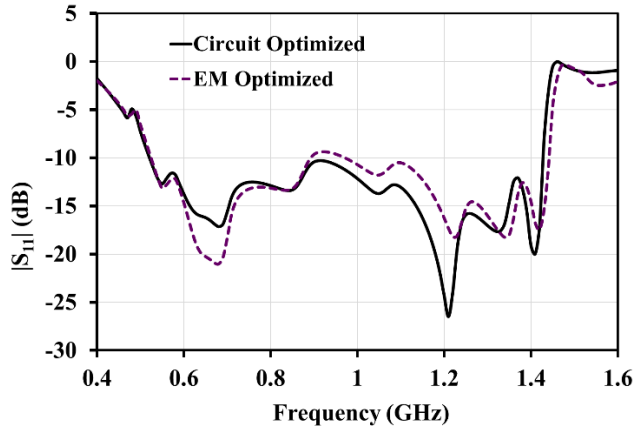


Fig. 10. Simulated $|S_{11}|$ of the rectifier against frequency after optimization.

Parameter	Initial (mm)	Circuit Optimized (mm)	EM Optimized (mm)
w_1	0.30	0.23	0.21
w_2	0.60	1.95	2.00
S	0.20	0.47	0.50
l	47.7	50.58	50.69

Tab. 2. Physical parameters of the coupled three-line transformer.

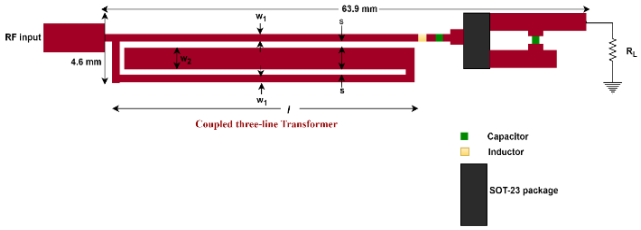


Fig. 11. Layout diagram of the proposed wideband rectifier.

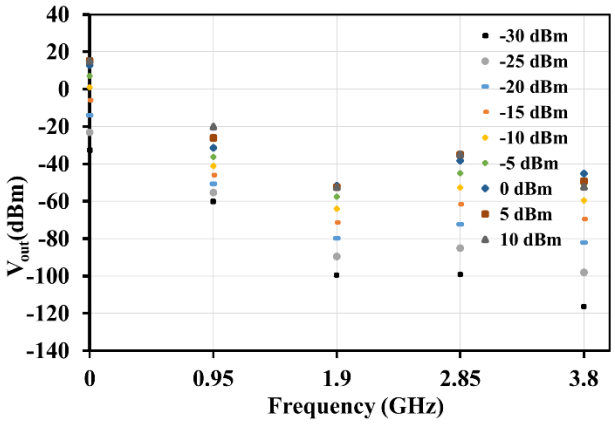


Fig. 12. Simulated 4th order harmonics spectrum in dBm of the rectifier at different P_{in}.

served from Fig. 9 that at 0–5 dBm input power range, $|S_{11}| \leq -10$ dB across the design frequencies. At –5 dBm input power, the $|S_{11}|$ response is acceptable.

After the circuit optimization, the electromagnetic (EM) simulation and optimization was performed using the same design parameters. The goal of the EM based optimization was to achieve an RF-DC efficiency of greater than 55% across the rectifier design frequencies. Figure 10 shows the circuit and EM optimized $|S_{11}|$ against frequency at 0 dBm. Figure 11 shows the layout of the proposed rectifier after optimization in ADS. The physical parameters of the CTLT are presented in Tab. 2.

Figure 12 shows 4th order harmonics of the proposed rectifier simulated in ADS. It can be observed that the proposed rectifier has a strong DC output, which confirms the circuit is functioning as intended. Besides, the harmonics present are well suppressed.

4. Fabrication and Measurements

The wideband rectifier was designed and fabricated on a RF-35 Taconic substrate. The measurement setup includes a signal generator (APSIN12G) and a digital multimeter. Figure 13(a) is a photograph of the measurement setup; Figure 13(b) shows the prototype of the fabricated wideband rectifier. The EM simulated and measured $|S_{11}|$ of the rectifier is shown in Fig. 14 for comparison. As it can be seen, both the simulated and measured results are in good agreement, with minor deviations probably, due to soldering losses and diode modelling error.

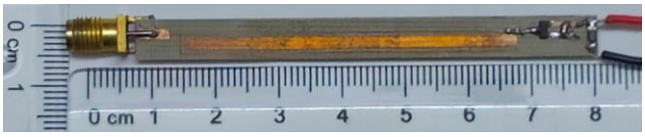
The rectifier PCE (η_{PCE}) is calculated as:

$$\eta_{PCE} = \left(V_{DC}^{\ 2} / R_L P_{in}\right) \times 100\% \tag{4}$$

where V_{DC} is the output voltage across the load.

Figure 15 shows the comparison of the measured and simulated PCE under different input powers from –20 dBm to 0 dBm with a load of 3 kΩ. From the figure, it can be seen that, when the input power is between –5 dBm to 0 dBm, the PCE from 0.5–1.3 GHz is greater than 52%. This shows the high level of efficiency of the rectifier over a wide range of frequencies. The rectifier performs optimally at 0 dBm with an efficiency more than 57% from 0.5–1.4 GHz. The CTLT's low insertion loss as established in [18] contributes to the rectifier's high efficiency (>57%) across 0.5–1.4 GHz.

(a)



(b)

Fig. 13. (a) Photograph of the measurement setup. (b) Photograph of the fabricated rectifier prototype.

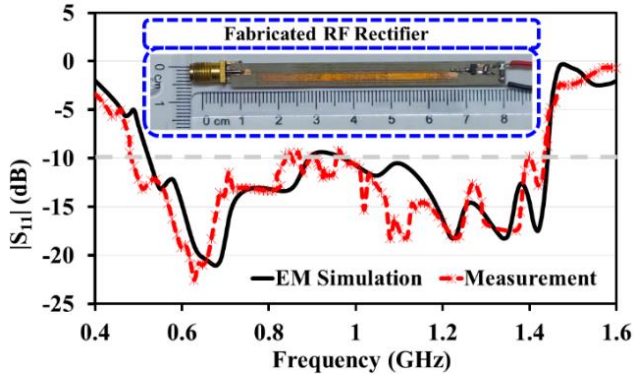


Fig. 14. Simulated and measured $|S_{11}|$ of the rectifier against frequency.

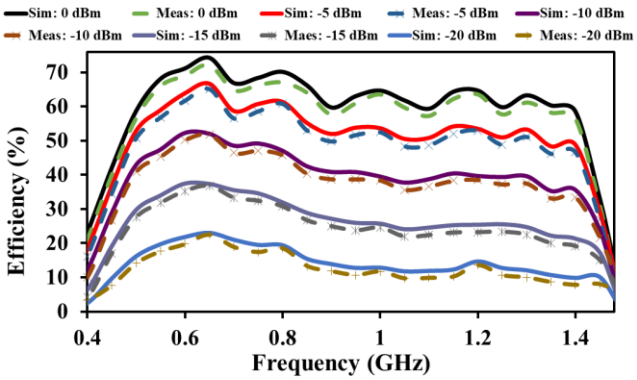


Fig. 15. Simulated and measured PCE against frequency for different input powers.

The measured and simulated PCE of the rectifier versus P_{in} for (a) 0.65 and 0.8 GHz and (b) 1 and 1.2 GHz are shown in Fig. 16, respectively. The rectifier achieves maximum PCE values of 74.2%, 67.68%, 63.18% and 63.18% at 0 dBm for the following frequencies: 0.65 GHz, 0.8 GHz, 1 GHz and 1.2 GHz, respectively. Figure 17 compares the simulated and measured PCE versus load for different input power values. The maximum PCE was observed for 3 kΩ at 0 dBm. The rectifier performance is relatively stable (PCE > 50%), when the load ranges from 2–7 kΩ and the input power is from –5 dBm to 0 dBm. Also, the rectifier has a relatively stable PCE across the loads from 2–15 kΩ for –5 dBm to –20 dBm. The rectifier performs optimally (PCE > 50%), when the input power is from –5 to 0 dBm.

The performance of the proposed wideband rectifier was compared to related works in Tab. 3. The rectifier achieves a PCE greater than 57% across its operating bandwidth at a low input power of 0 dBm, with a maximum PCE of 74.2%. In contrast, the rectifiers in [15–17, 25–27] which achieve PCEs above 50%, but require high input power levels (8–23.5 dBm), have limited suitability for ambient energy harvesting, where available power is typically below 0 dB.

The rectifier in [28] achieves a PCE greater than 40% at 0 dBm, but its maximum PCE is 63% at a much higher input power of 10 dBm, indicating lower efficiency. The proposed rectifier has a narrower bandwidth compared with [15] (0.06–3.91 GHz) and [25] (0.6–3.8 GHz). However, its

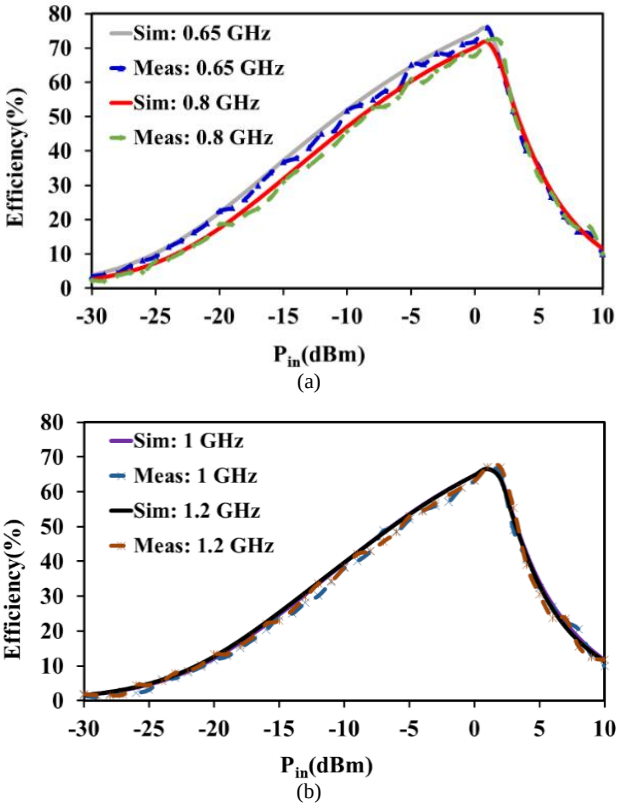


Fig. 16. Simulated and measured PCE of the proposed wideband rectifier against different input powers P_{in}: (a) 0.65 and 0.8 GHz; (b) 1 and 1.2 GHz.

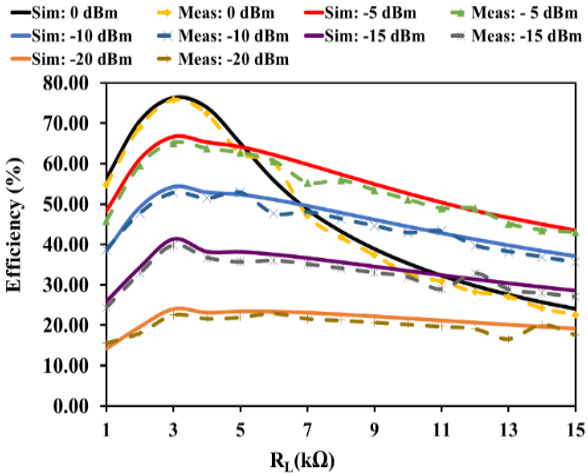


Fig. 17. Simulated and measured PCE of the proposed wideband rectifier against load for different input powers.

high PCE at low input power compensates for this, as ambient energy harvesting prioritizes efficiency over ultra-wide bandwidths. The 0.5–1.4 GHz range covers key RF bands like the DTV, LTE-700, GSM-900 and ISM-900. The rectifier in [28] has a bandwidth of 0.87–2.0 GHz (1.13 GHz), which is slightly wider than the proposed design, but its PCE is lower.

In terms of size, the proposed rectifier is compact, measuring 72.3×6.3 mm^2, with an electrical size of $0.428\lambda \times 0.037\lambda$. It is smaller than the designs in [26] (670 mm^2), (528 mm^2), [27] (570 mm^2),and [30]

(6871 mm^2), but larger than [15] (141 mm^2), [16] (99 mm^2), [17] (120 mm^2) and [28] (114 mm^2). The rectifier in [16] is the most compact among those listed in Tab. 3, but it requires a high input power of 20 dBm, reducing its suitability for low-power applications. The proposed rectifier balances size and efficiency, making it suitable for integration into compact devices such as IoT devices. The proposed rectifier employs a CTLT structure, reducing design complexity while maintaining high performance. In contrast, [16], [17], [25–27, 29, 30] use complex designs increasing fabrication costs, while [15] has moderate complexity and [28] is also simple but less efficient. Its low input power requirement, high PCE, compact size, and simple design make the proposed rectifier suitable for harvesting RF signals in applications like IoT devices and wearable electronics.

Ref.	PCE, P_{in} at operating bandwidth				Size (mm^2)	Design complexity
	BW	PCE	P_{in} (dBm)	Max PCE		
[15]	0.06–3.91	>50	17	68.8% @ 21 dBm	141	Moderate
[16]	0.39–2.9	>50	20	71.7% @ 20 dBm	99	Complex
[17]	0.33–2.61	>50	8.5–23.5	79.7% @ 19 dBm	120	Complex
[25]	0.6–3.8	>50	8	66.6% @ 8 dBm	528	Complex
[26]	0.54–1.3	>50	10	80% @ 10 dBm	670	Complex
[27]	0.2–3.2	>50	15	78.2% @ 15 dBm	570	Complex
[28]	0.87–2.0	>40	0	63% @ 10 dBm	114	Simple
[29]	1.55–2.6	>50	−5.0–5.0	70% @ 4 dBm	NA	Complex
[30]	2.3–2.8	>30	−20.0–10.0	67% @ 7 dBm	6871	Complex
This work with CTLT	**0.5–1.4**	**>57**	**0**	**74.2% @ 0 dBm**	**459**	**Simple**

Tab. 3. Comparison with other related works.

5. Conclusion

This paper presents a wideband rectifier using a Coupled Three-line Transformer (CTLT) for low-power Internet of Things (IoT) and Wireless Sensor Network (WSN) applications. The detailed design procedure of the impedance matching network was presented. The rectifier has a simple structure, operates from 0.5–1.4 GHz and achieves a Power Conversion Efficiency (PCE) greater than 57% at 0 dBm across the design range. It has a maximum efficiency of 74.2% at 0 dBm. The design maintains stable performance (>50% PCE) for loads from 2–7 kΩ with a compact electrical size of $0.428\lambda \times 0.037\lambda$. While the proposed design achieves high PCE at low input power, its bandwidth is narrower than some recent designs. The measured results showed that the proposed rectifier design is suitable for wideband rectifier applications. Future research includes integrating an antenna with the rectifier and extending the bandwidth further.

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About the Authors ...

Aminu Muhammad ABBA (corresponding author) received a B.Eng. degree in Electrical Engineering from Ahmadu Bello University, Zaria, in 2014 and an M.Sc. degree in Telecommunications Engineering from the same institution in 2017. He is currently pursuing a Ph.D. in Electrical and Electronics Engineering at Nile University of Nigeria, Abuja. He is a student member of the Institute of Electrical and Electronics Engineers (IEEE), a member IEEE Antenna and Propagation Society, and a member of the Nigerian Society of Engineers. His areas of research interest are wireless sensor networks, RF energy harvesting, optimization, and wireless communications.

Tologon KARATAEV (corresponding author) is an Associate Professor in the Department of Electrical and Electronics Engineering at Nile University of Nigeria, Abuja. He received his bachelor's degree in Electrical and Electronics Engineering from Istanbul University, Istanbul, Turkey in 2003, an M.Sc. degree in Electronics and Communications Engineering from Yildiz Technical University, Istanbul, Turkey, in 2007 and a Ph.D. degree in Electronics and Communications Engineering from the same institution in 2016. He served as a Lecturer and Head of Department at International Alatoo University (IAU), Kyrgyzstan, from 2011 to 2016 and as a Postdoctoral Research Fellow in the Department of Microelectronic Systems at Gdansk University of Technology, Poland from 2016 to 2019. He was a Senior Lecturer in the Department of Electrical and Electronics Engineering, Nile University of Nigeria from 2019 to 2023. His research interests include broadband wireless systems, RF energy harvesting (rectifiers), passive RF/microwave circuits, low-noise amplifiers, RF/microwave filters, matching circuits; metamaterials, composite right/left-handed transmission lines; metaheuristic optimization applications. He has been a member of the Institute of Electrical and Elec-

tronics Engineers (IEEE) and the Institute of Engineering and Technology (IET) since 2021.

Omotayo OSHIGA is a Professor and Head of the Department of Electrical and Electronics Engineering of Electrical and Electronics Engineering, Nile University of Nigeria, Abuja. He received a B.Tech. degree in Physics Electronics from the Federal University of Technology, Minna, Niger State in 2010, and an M.Sc. degree in Wireless Communication Systems from Brunel University, London, UK in 2011. He earned a Ph.D degree in Electrical Engineering from Jacobs University, Bremen, Germany in February 2015. He served as Lecturer I in the Department of Electrical and Electronics Engineering at Nile University of Nigeria from 2015 to 2016 and completed a Postdoctoral Fellowship in Hong Kong with Hong Kong Baptist University and Hong Kong Polytechnic University from 2016 to 2019. His research interests include estimation theory, signal processing, wireless sensor networks, indoor and outdoor positioning, tracking and navigation, wireless sensing.

Surajo MUHAMMAD earned a Bachelor's of Engineering in Computer Engineering from Bayero University, Kano, Nigeria, in 2004. He completed a Master of Engineering in Electronics and Telecommunications Engineering at Universiti Teknologi Malaysia (UTM), Johor, Malaysia, in 2014, funded by the Kano State Government Overseas Scholarship. Dr. Muhammad earned a Ph.D. at Multimedia University (MMU) in Cyberjaya, Selangor, Malaysia, in 2022 with his doctoral studies funded by a research grant from TM R&D Telekom Malaysia Berhad, where he served as a Research Scholar. In 2023, he expanded his expertise as a Postdoctoral Research Fellow with the Center for Wireless Technology (CWT) at MMU. His research interests include RF energy harvesting (RFEH) for biomedical implants, wireless power transfer systems for biomedical devices, 5G mm-wave antennas, and wearable and implantable antennas. He currently serves as a researcher at the Center for Intelligent Network, Telekom Research & Development (TM R&D), within the TM Innovation Centre in Cyberjaya, Selangor, Malaysia.

Jun Jiat TIANG (corresponding author) received a Bachelor's degree in Electronics Engineering from Multimedia University, Malaysia, a master's degree from the University of Science, Malaysia, and a Ph.D. degree from Universiti Kebangsaan Malaysia (UKM). He worked as a Design Automation Engineer with the Chipset Structural Design Team, Intel Microelectronics (M) Sdn. Bhd., Penang, Malaysia, from September 2004 to July 2005, and an Electronics Engineer with the Global Technology Development Group, Motorola Technology Sdn. Bhd., Penang, from May 2006 to May 2007. He has extensive experience as a Project Leader in various research grants, including, TM Research and Development (2017–2020), the Ministry of Science, Technology and Innovation (MOSTI) Research Grant (2008–2010), and the Mini Fund research grant (2016). He is currently an Assistant Professor and Researcher with the Faculty of Engineering, Multimedia University. His research interests include RFID, microwave circuits, antenna, and propagation. He was awarded the Gold Medal at the 23rd International Invention, Innovation, and Technology Exhibition (ITEX) 2012, Kuala Lumpur, Malaysia, in May 2012, and the Silver Medal at the Malaysian Technology Expo (MTE) 2013, Kuala Lumpur, in February 2013.

Nazih Khaddaj MALLAT (Senior Member, IEEE) received his bachelor's degree in Electrical and Electronics Engineering from Lebanese University, Lebanon, in 2000, a Master's degree in Information Technology from IMT Atlantique, France, in 2002, and a Ph.D. in Telecommunications from the University of Quebec, Canada, in 2010. He served as a Postdoctoral Fellow at École Polytechnique de Montréal until January 2012. In 2013, he joined the College of Engineering at Al Ain University (AAU) in the United Arab Emirates as an Assistant Professor and was promoted to Associate Professor in 2019. At AAU, he served as Head of the Networks and Communication Engineering and Computer Engineering Department (2013–2017), Deputy Dean of the College of Engineering (2014–2015), Dean of the College of Engineering (2015–2018), and Director of the Quality Assurance and Institutional Research Center (2018–2020). Since November 2020, he has served as the Vice President of Accreditation and Quality Assurance. He has gained extensive teaching experience at undergraduate and graduate levels including courses and laboratory components at universities in Montreal such as ETS, TELUQ, and École Polytechnique de Montréal. His research interests encompass passive microwave and millimeter-wave circuits, antennas, and filters with over 60 publications. He is a member of the Ordre des Ingénieurs du Québec, Canada, and the Order of Engineers and Architects Tripoli, Lebanon. He received two doctoral scholarships from the Fonds Québécois de la Recherche sur la Nature et les Technologies (FQRNT) in 2008 and a postdoctoral research grant (2010–2011). He founded the IEEE AAU Student Branch and the IEEE UAE MTT-S Chapter (which later became the IEEE UAE MTT-S, IM-S, and AP-S Joint Chapter). He served as Vice-Chair of the IEEE Montreal Section from 2007 to 2008, Membership Development Chair (2009–2010), and Section Chair (2011–2012). As well as the IEEE UAE Technical Activities Coordinator (2015–2018), and the IEEE Region 8 Chapter Coordination Subcommittee Chair (2015–2016). He chaired organizing committees for three major events hosted by Al Ain University: the 1st IEEE International Workshop at AAU (February 2014), the 11th IEEE UAE Student Day in May 2016, and the 16th Mediterranean Microwave Symposium (MMS2016) in November 2016.

Aliyu Danjuma USMAN is a Professor of Electronics & Telecommunications Engineering from Ahmadu Bello University, Zaria. He earned Bachelor's degree in Computer Engineering from Maryam Abacha American University of Nigeria, an M.Sc in Computer Engineering from Bayero University, Kano, and a Ph.D. in Electrical and Electronics Engineering from Universiti Putra, Malaysia. He is a self-motivated researcher with expertise in communication engineering and information technology, possessing a detail-oriented mindset, analytical skills, collaboration and a proven ability to accomplish multiple tasks. He has published over 180 peer-reviewed journal and conference papers, authored

numerous books and book chapters and held a patent. He has over 600 citations with an h-index of 12 and has received multiple research grants locally and internationally. He was awarded the Grant Fellow of the Year by Ahmadu Bello University in 2025 and has supervised over 65 M.Sc. and 12 Ph.D. students to graduation. He is a visiting scholar at Baze University, Nigeria, a consultant and an external examiner for institutions in Nigeria and internationally. His research interests include teletraffic engineering, satellite communications, antenna radiation, wireless communications, microwave engineering, IoT, EMF & EMC, Terahertz frequencies, 5G and beyond.