DSSZ-SM: A Simplified Chirp Coding Scheme with Inherent Clock Synchronization

Lerson KIRASAMUTHRANON [1], Jeerasuda KOSEEYAPORN [2], Paramote WARDKEIN [2]

[1] Dept. of Electronics Engineering Technology, College of Industrial Technology, King Mongkut's University of Technology North Bangkok, Bangkok 10800, Thailand
[2] School of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand

lersonk@kmutnb.ac.th, {jeerasuda.ko, paramote.wa}@kmitl.ac.th

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Abstract. *This study proposes a novel double-slope chirp symbol, termed double-slope start zero stop minimum (DSSZ-SM), for efficient data communication. Unlike conventional chirp coding, which often involves complex generation and synchronization, the DSSZ-SM provides a simpler structure with inherent clock synchronization using a PWM-based generator. System performance is evaluated through analysis and simulations over additive white Gaussian noise (AWGN) and Rayleigh fading channels. Two asynchronous decoding methods, with and without an integrator, are compared. Results show that the non-integrator approach achieves lower error rates under both channel conditions. The proposed DSSZ-SM offers a simplified and robust alternative for efficient data communication.*

Keywords

Double-slope chirp, chirp encoding, asynchronous decoding; data communication

1. Introduction

Data communications today primarily rely on wireless or fiber optic networks. Regardless of the coding method used, user data travel over the same network, leading to a high demand for bandwidth due to the large volume of data. Consequently, when the number of users or the amount of data increases, bandwidth sharing becomes a limiting factor.

Low-power, low-bandwidth data transmission is essential for long-distance wireless communication. This is typically achieved by mapping digital data into analog sinusoidal waveforms. Conventional modulation techniques, such as amplitude shift keying (ASK), frequency shift keying (FSK), phase shift keying (PSK), and quadrature amplitude modulation (QAM), however, often require relatively high energy per bit and exhibit limited robustness to fading noise [1]. Chirp coding has emerged as a promising alternative, encoding data symbols into linearly and continuously varying frequencies, thereby enabling joint time-frequency modulation (PWM) and improved resistance to fading. Originally developed for radar applications, chirp signals provide long-range operation and low power consumption [2–4]. Chirp signals are widely used in modern wireless communication and sensing applications due to their robustness and low power consumption. LoRa technology uses chirp spread spectrum to enable long-range IoT communication [5], while chirp-based techniques have also been applied to IoT signal processing and denoising [6] and to data transmission in LEO satellite IoT systems [7], [8]. Beyond communication, chirp signals are utilized in sensing applications such as FMCW radar-based hand gesture recognition [9], [10]. Recent works on joint communication and sensing (JC&S) systems have emphasized the need for efficient and hardware-friendly waveform designs, motivating the development of simplified chirp-based schemes [11].

Moreover, chirp spread spectrum has been standardized in IEEE 802.15.4a for low-rate wireless personal area networks [12], [13]. Despite these advantages, the development of chirp coding formats has received limited attention. Existing schemes are mainly based on single-slope (up- or down-chirp) or cyclic-shift chirps [14–18], both of which suffer from synchronization limitations.

Recently, chirp coding schemes known as double-slope frequency shift chirp-down-chirp start zero (DSFSC-DCSZ) and double-slope frequency shift chirp-down-chirp stop minimum frequency (DSFSC-DCSMF) were invented and proposed [19]. A key characteristic of these codes is the double slope within a single symbol, which results in an inherent clock signal embedded in the coded signal. This distinguishes them from existing chirp coding techniques such as single-slope chirp or cyclic-shift chirp. However, the generation process for DSFSC-DCSZ and DSFSC-DCSMF codes is relatively complex.

In this study, a double-slope chirp symbol called Double-Slope Start Zero Stop Minimum (DSSZ-SM) is proposed. While sharing a key characteristic with DSFSC-DCSZ and DSFSC-DCSMF [19], the DSSZ-SM generation process is simpler. The DSSZ-SM code generator has a compact structure consisting of a PWM modulator and a multiplier. A significant advantage of DSSZ-SM is the ease of extracting the reference ramp signal, which facilitates receiver decoding. After retrieving the reference ramp signal, the PWM signal can be recovered using three methods: a com-

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parator, a differentiator, or a clipper. Additionally, this study presents a method for recovering the clock signal from the DSSZ-SM chirp symbols. Furthermore, theoretical analysis and simulation results for two asynchronous decoding techniques demonstrate that asynchronous decoding without an integrator yields lower error than that with an integrator.

In the literature, many studies have implemented chirp-based techniques using FPAA or FPGA platforms [20–23], which are well suited for high-frequency and reconfigurable applications. In this work, however, the proposed DSSZ-SM scheme is first validated both theoretically and experimentally through a preliminary low-frequency analog electronic circuit implementation. This approach is intended to demonstrate the fundamental feasibility and practical realizability of the proposed encoding and decoding principles using simple hardware.

Regarding frequency limitations, the achievable operating frequency of the proposed analog circuits is primarily constrained by the bandwidth, slew rate, and switching characteristics of the selected components, such as operational amplifiers, comparators, A/D, and D/A devices. Consequently, the present prototype is suitable for low- to moderate-frequency operation. For higher-frequency or high-data-rate applications, the proposed DSSZ-SM scheme can be extended to FPAA or FPGA implementations, where digital timing control and high-speed logic resources can significantly enhance performance and scalability.

The organization of this article is as follows. Section 2 provides a brief review of existing chirp coding schemes. Section 3 describes the principles of the proposed DSSZ-SM coding scheme, including the encoding and decoding procedures, and the method for clock signal recovery. Section 4 presents the error performance analysis of the proposed chirp symbols under additive white Gaussian noise (AWGN) and Rayleigh fading conditions. To validate the proposed scheme, Sections 5 and 6 present simulation results obtained in MATLAB and experimental results based on circuit implementation. Finally, Section 7 presents the conclusions.

2. Related Principles

Most chirp coding formats currently in use can be classified into three forms as follows:

- Single-slope chirp coding

In single-slope chirp coding, there are two chirp symbols, which are up-chirp and down-chirp. Each symbol encodes a data bit (1 or 0); e.g., data bit "1" is encoded with an up-chirp symbol, whereas data bit "0" is encoded with a down-chirp symbol or vice versa. The chirp symbol is converted into the form of a sinusoidal signal whose frequency is linearly increased or decreased according to the chirp symbol. The generated chirp signal can be mathematically defined as

$$c(t) = A\cos\left(\omega_c t + \frac{1}{2}\mu t^2\right) \tag{1}$$

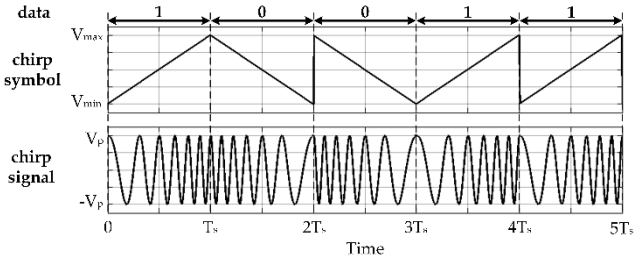


Fig. 1. Example of single-slope chirp symbols and signals.

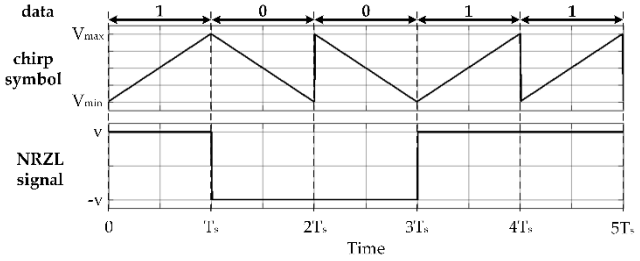


Fig. 2. Example of the decoded data bit from the chirp signal.

where A is the amplitude of the chirp signal (volt), ω_c is the angular frequency of the carrier signal (radian/second), and μ is the chirp rate (radian/second^2). The instantaneous frequency of the chirp signal is achieved by differentiating the angular frequency with respect to time, which is

$$\omega_i(t) = \omega_c + \mu t\,. \tag{2}$$

It is seen that the frequency of the chirp signal is changed upward or downward for $\mu > 0$ or $\mu < 0$, respectively. Consequently, the lowest frequency and highest frequency of the up-chirp signal and the down-chirp signal are the same. An example of single-slope chirp symbols and signals is depicted in Fig. 1. In the decoding process, the chirp symbols are retrieved via FM demodulation of the chirp signal. By differentiating the chirp symbols, the data bits are obtained, for example, in the form of an NRZL signal, as shown in Fig. 2. The limitation of single-slope chirp coding is that it can only be used for 1-bit encoding, and it requires coherent demodulation. The reference clock signal is required for demodulation.

- Quadrature chirp coding [24]

Due to the limitations of single-slope chirp coding, which encodes only 1 bit per symbol, a new method has been developed that allows more than 1 bit per symbol. This is achieved by using 2^{n-1} sets of lowest and highest frequencies for n-bit chirp coding. For example, 2-bit chirp encoding requires two sets of up-chirp and down-chirp symbols, as well as two sets of lowest and highest frequencies for the linearly sweeping frequency of the sinusoidal carrier signals, as illustrated in Fig. 3. As shown, quadrature chirp coding is based on up-chirp and down-chirp symbols modulated with different sinusoidal carrier signals.

- Cyclic-shift chirp coding [14], [15]

Cyclic-shift chirp coding uses only up-chirp or down-chirp symbols, where n-bit coding requires n different up-chirp or down-chirp levels per symbol. The key characteristic

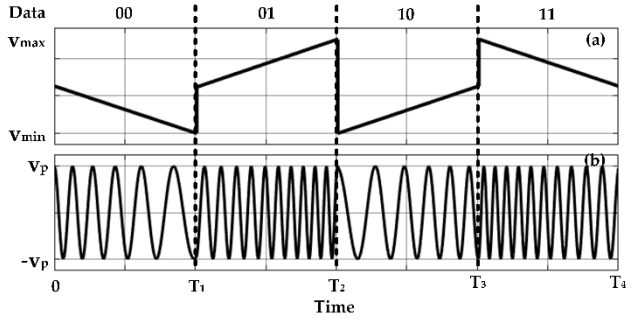


Fig. 3. Example of 2-bit quadrature chirp coding.

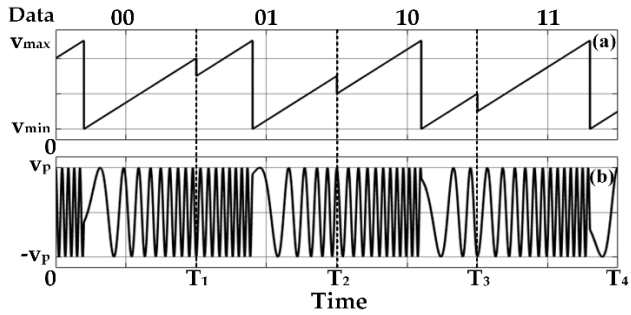


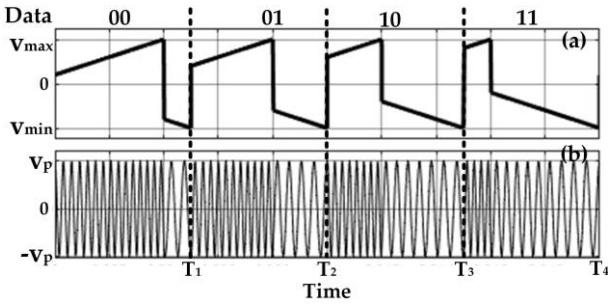
Fig. 4. Example of the 2-bit cyclic shift chirp coding.

of this coding is that the starting and ending frequencies are equal. As shown in Fig. 4, this is a 2-bit cyclic-shift chirp coding. Each cyclic-shift chirp symbol has two up-chirp levels, and the starting frequency is always equal to the ending frequency. Since the bandwidth of each symbol is determined by the difference between its maximum and minimum frequencies, and the coding scheme ensures that this difference is relatively consistent across all symbols, estimating the total bandwidth usage of the proposed coding becomes feasible.

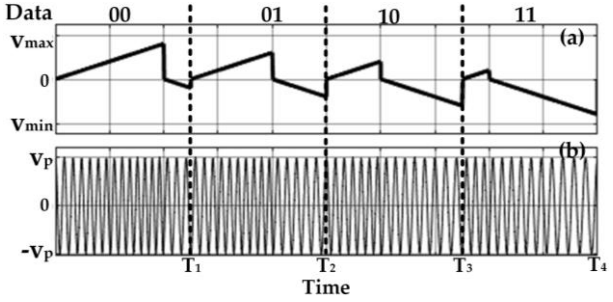
3. The Proposed Double-Slope Start Zero Stop Minimum Chirp Symbol

Given the limitations of conventional chirp coding schemes, this study introduces a novel approach termed double-slope start zero stop minimum (DSSZ-SM) coding. The concept of double-slope chirp coding was first proposed in [19] as the double-slope frequency shift chirp (DSFSC), which is classified into two formats: down-chirp stop minimum frequency (DCSMF) and down-chirp start zero (DCSZ). A key characteristic of DSFSC is the inclusion of both up-chirp and down-chirp within a single symbol, enabling inherent clock embedding for bit synchronization.

The primary distinction between these formats lies in their signal levels. In DSFSC-DCSMF, both the maximum and minimum levels remain constant across symbols, as shown in Fig. 5(a), although the starting levels of the up-chirp and down-chirp may vary. In contrast, DSFSC-DCSZ starts at 0 V for both chirp components, as illustrated in Fig. 5(b), but exhibits varying maximum and minimum levels for each symbol. As a result, despite their synchronization capability, both schemes require relatively complex signal generation due to variations in signal levels and starting points.



(a) DSFSC-DCSMF



(b) DSFSC-DCSZ

Fig. 5. Example of the 2-bit double-slope frequency shift chirp signals.

To address these limitations, this study presents a novel simplified coding scheme for generating double-slope chirp symbols. The proposed DSSZ-SM scheme features a consistent signal structure, in which each symbol starts at 0 V and ends at the minimum level of −Vmax. This design significantly simplifies signal generation while preserving the inherent synchronization capability of double-slope chirp coding. In addition, the embedded reference clock within each symbol enables noncoherent decoding without requiring external synchronization.

The following subsections describe the proposed encoding and decoding schemes in detail, along with the method for clock signal recovery.

3.1 Double-Slope Start Zero Stop Minimum (DSSZ-SM) Encoding

The main feature of the proposed chirp coding is that each symbol consists of two parts. The first part is an up-chirp, starting at 0 V and ending at the voltage level of the instantaneous information signal at that time. The second part is a down-chirp, starting at a level opposite to the ending voltage of the first part and ending at a minimum level minus Vmax. The graphical illustration of the DSSZ-SM chirp symbol for the 2-bit coding is shown in Fig. 6. The mathematical expression of a double-slope start zero stop minimum chirp symbol is given by

$$v(t)=\begin{cases} s(t-T_{i-1}) & ;\ T_{i-1}\le t\le t_{p_i}+T_{i-1} \\ -s(t-T_{i-1}) & ;\ t_{p_i}+T_{i-1}\le t\le T_i \end{cases} \tag{3}$$

where s is the slope of the up–chirp duration, t_{p_i} is the duration of the first part of the chirp symbol relating to the analog level of the data bit, and T_i is the duration of the i^{th}

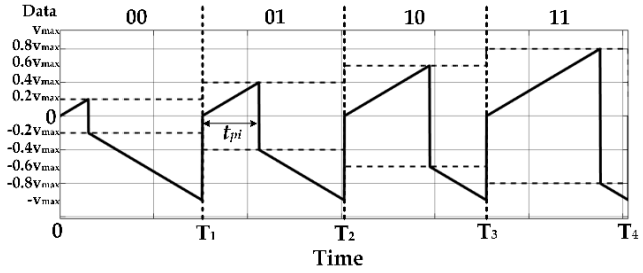


Fig. 6. Example of the double-slope start zero stop minimum chirp symbol for 2-bit coding.

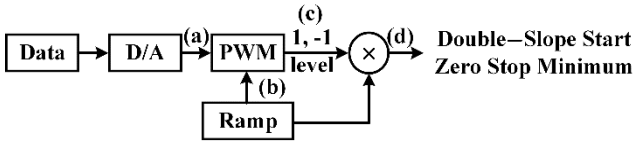


Fig. 7. Procedure for generating the DSSZ-SM chirp symbol.

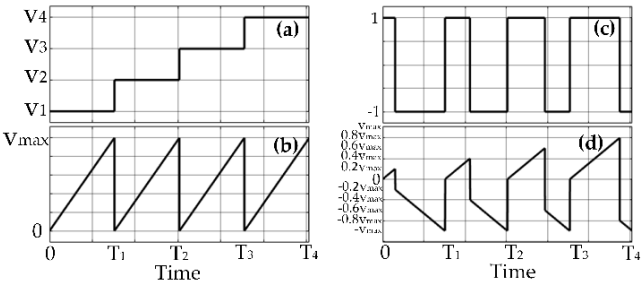


Fig. 8. Example of signals at points (a)–(d) of the DSSZ-SM chirp symbol generating procedure.

chirp symbol. The procedure for generating the proposed DSSZ-SM symbol is demonstrated in Fig. 7. For the 2-bit chirp symbols, the signals at points (a)–(d) are illustrated in Fig. 8. As depicted in Fig. 8, the process of generating a DSSZ-SM chirp symbol commences with pulse-width modulation (PWM) between the analog level of the data symbol (illustrated in Fig. 8(a)) and a ramp signal (shown in Fig. 8(b)). The PWM output, presented in Fig. 8(c), is a signal with a maximum level of 1 V and a minimum level of –1 V. The PWM signal period is controlled by the ramp signal period, while the duty cycle of each period is determined by the duration that the data level exceeds the ramp signal. The resulting PWM signal is then multiplied by the ramp signal, yielding the DSSZ-SM chirp symbol shown in Fig. 8(d). Because the ramp signal is designed to have only positive voltages starting from 0 V, the initial level of each generated chirp symbol is always 0 V. Furthermore, due to the 1 V and –1 V levels of the PWM signal, the obtained DSSZ-SM symbols exhibit both upward and downward chirps within each symbol. The DSSZ-SM symbols are then modulated with a carrier sinusoidal signal to obtain the DSSZ-SM chirp signals.

3.2 Double-Slope Start Zero Stop Minimum (DSSZ-SM) Decoding

The decoding process of the proposed DSSZ-SM chirp signal involves three primary steps, which proceed as follows.

A. FM demodulation

First, the received chirp signal is demodulated using FM, resulting in the DSSZ-SM symbol. Note that the standard FM demodulation technique can be used to obtain the DSSZ-SM chirp symbol.

B. DSSZ-SM symbol decoding

Second, since the proposed method encodes data symbols as PWM signals, the PWM signals must be extracted from the DSSZ-SM symbols before decoding to obtain the data bits. This requires a reference sawtooth signal. The reference sawtooth signal can be retrieved from the DSSZ-SM symbol using an absolute circuit, which reverses the down-chirp portion of the DSSZ-SM symbol to be the up-chirp. Once the reference sawtooth signal is obtained, the PWM signal can be extracted. There are three techniques to extract the PWM signal: 1) a comparator, 2) a differentiator, or 3) a clipper, as shown in Figs. 9(a)–9(c), respectively.

C. Data bit decoding

After the PWM signals are obtained, their widths are converted to a voltage level using an integrator. A sample-and-hold circuit is then used to hold the signal's level and obtain the analog level of the data symbol. Finally, the analog level of each data symbol is converted to digital data bits. The block diagram is shown in Fig. 10(a). However, it was found that the maximum level of the integrator's output in each period of the PWM signal was identical to the maximum level of each DSSZ-SM symbol. Therefore, the integrator is not necessary for decoding. The simplified block

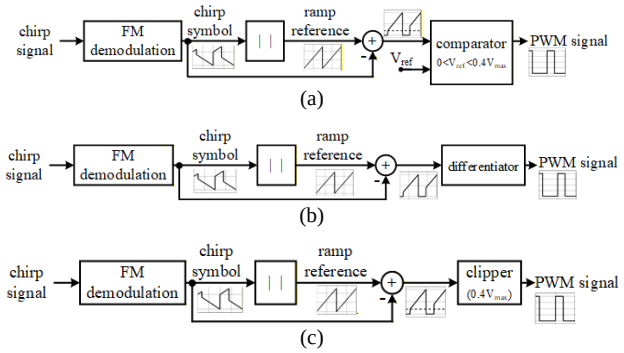


Fig. 9. Techniques of retrieving the PWM signal using (a) a comparator, (b) a differentiator, and (c) a clipper.

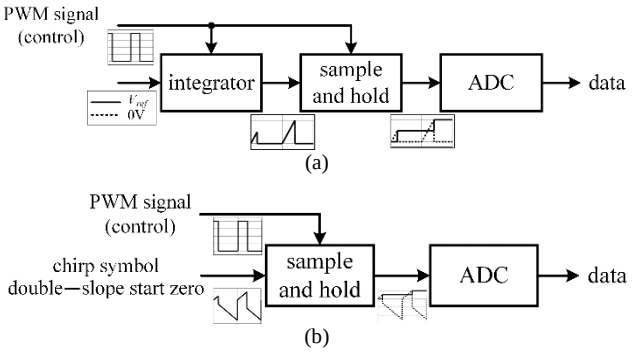


Fig. 10. Decoding data bits of the proposed chirp symbol (a) using an integrator and (b) without an integrator.

diagram of decoding the DSSZ-SM symbols is shown in Fig. 10(b). Both data-decoding techniques are asynchronous, since the reference clock signal is not required.

3.3 Clock Signal Retrieval of the Proposed DSSZ-SM Chirp Signal

The clock signal is crucial for synchronizing data bits. In the proposed chirp signal, the clock signal is embedded within the DSSZ-SM chirp signal. As explained in the previous subsection, the decoding process is a noncoherent scheme. In this subsection, we discuss techniques for retrieving the clock signal from the proposed chirp signal based on the ramp signal. As depicted in Fig. 9, the method for reconstructing the ramp signal is provided. From the given ramp signal, the clock signal can be retrieved as follows:

1. Using a subtractor, an absolute circuit, and a differentiator as shown in Fig. 11(a). The difference between the reference ramp signal and the constant level of 0.5Vmax is the ramp signal, which ranges from –0.5Vmax to 0.5Vmax. Subsequently, the signal passes through an absolute circuit, resulting in a triangular signal. Differentiating the triangular signal yields the clock signal.

2. Using a comparator as shown in Fig. 11(b). This technique is simpler than the first method, requiring only a comparator. As illustrated in Fig. 11(b), the reference signal is compared with the constant level of 0.5Vmax, producing the clock signal with levels of either 0 V or Vmax.

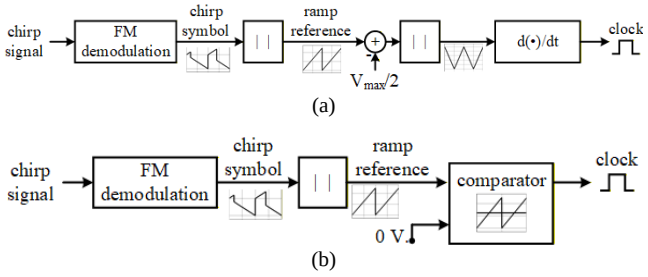


Fig. 11. Techniques for retrieving the clock signal: (a) Using a subtractor, an absolute circuit, and a differentiator and (b) using a comparator.

4. Error Performance Analysis

In this subsection, the mathematical analysis for error performance of the 2-bit per symbol of the proposed coding scheme is presented. In addition, the error performance of the proposed asynchronous decoding scheme is given.

4.1 Error Performance Analysis of the 2-bit Per Symbol Proposed Coding Scheme

A. Under Gaussian noise (AWGN)

The probability of bit error (P_e) of the 2-bit per symbol under Gaussian noise channel (AWGN) is analyzed based on an optimal receiver as depicted in Fig. 12. Since the chirp

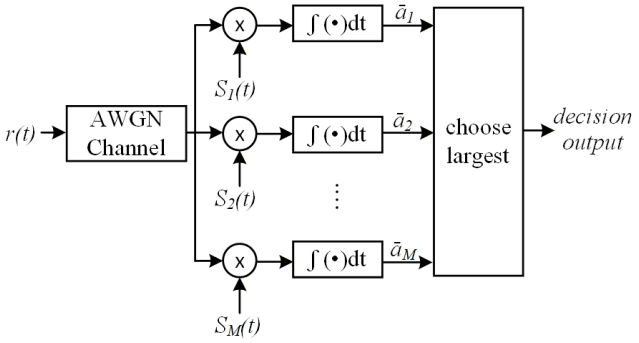


Fig. 12. The structure of an optimal receiver for probability error analysis.

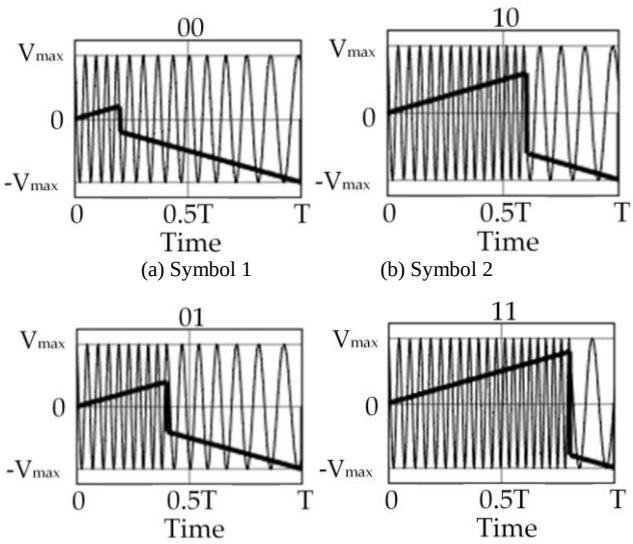


Fig. 13. The chirp symbols and chirp signals for the 2-bit per symbol case of the DSSZ-SM coding scheme.

signal of the proposed chirp symbol has equal energy in every symbol, the probability of bit error is given by [25]

$$P_e = Q\left(\sqrt{\frac{E_s\left(1-\rho\left(s_n, s_m\right)\right)}{N_0}}\right) \tag{4}$$

where E_s is energy of each symbol, and $\rho(s_n, s_m)$ is the normalized correlation between the n^{th} symbol S_n and the m^{th} symbol signal S_m, where n, m is 1,2,3,4, and $\rho(s_n, s_m)$ is defined by

$$\rho\left(s_n, s_m\right) = \frac{1}{E_s}\int_0^{T_s} s_n(t)\, s_m(t)\, \mathrm{d}t. \tag{5}$$

For 2-bit per symbol, there were a total of four symbols for 00, 01, 10, and 11. The chirp symbols and chirp signals for the 2-bit per symbol case of the DSSZ-SM coding scheme are depicted in Fig. 13.

In case the FM modulator is based on the VCO, where ω_c is a free-running frequency and k_{vco} is a modulation sensitivity (Hz/V), the normalized correlation of each symbol pair is given as follows.

Case symbol 1 and 2:

$$\rho(s_1,s_2)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(0.8\pi+0.4k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.2T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(1.6\pi)-\sin(0.8\pi)}{2\omega_c}+\frac{\sin(0.8Tk_{vco})-\sin(0.4Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(1.6\pi-0.8Tk_{vco})}{2\omega_c-2k_{vco}}+0.6T\right] \quad (6)$$

Case symbol 1 and 3:

$$\rho(s_1,s_3)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(0.8\pi+0.4k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.2T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(2.4\pi)-\sin(0.8\pi)}{2\omega_c}+\frac{\sin(1.2Tk_{vco})-\sin(0.4Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(2.4\pi-1.2Tk_{vco})}{2\omega_c-2k_{vco}}+0.4T\right] \quad (7)$$

Case symbol 1 and 4:

$$\rho(s_1,s_4)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(0.8\pi+0.4k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.2T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(3.2\pi)-\sin(0.8\pi)}{2\omega_c}+\frac{\sin(1.6Tk_{vco})-\sin(0.4Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(3.2\pi-1.6Tk_{vco})}{2\omega_c-2k_{vco}}+0.2T\right] \quad (8)$$

Case symbol 2 and 3:

$$\rho(s_2,s_3)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(1.6\pi+0.8k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.4T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(2.4\pi)-\sin(1.6\pi)}{2\omega_c}+\frac{\sin(1.2Tk_{vco})-\sin(0.8Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(2.4\pi-1.2Tk_{vco})}{2\omega_c-2k_{vco}}+0.4T\right] \quad (9)$$

Case symbol 2 and 4:

$$\rho(s_2,s_4)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(1.6\pi+0.8k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.4T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(3.2\pi)-\sin(1.6\pi)}{2\omega_c}+\frac{\sin(1.6Tk_{vco})-\sin(0.8Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(3.2\pi-1.6Tk_{vco})}{2\omega_c-2k_{vco}}+0.2T\right] \quad (10)$$

Case symbol 3 and 4:

$$\rho(s_3,s_4)=\frac{A^2}{2E_s}\left[\left[\frac{\sin(2.4\pi+1.2k_{vco}T)}{2\omega_c+2k_{vco}}\right]+0.6T\right]+\frac{A^2}{2E_s}\left[\frac{\sin(3.2\pi)-\sin(2.4\pi)}{2\omega_c}+\frac{\sin(1.6Tk_{vco})-\sin(1.2Tk_{vco})}{2k_{vco}}\right]+\frac{A^2}{2E_s}\left[\frac{\sin(4\pi-2Tk_{vco})-\sin(3.2\pi-1.6Tk_{vco})}{2\omega_c-2k_{vco}}+0.2T\right] \quad (11)$$

B. Under Rayleigh fading

Error performance analysis for the Rayleigh fading channel of the proposed coding scheme was also considered. The average probability of error P_{e_av} is conventionally evaluated as the integral of the product of the error probability in the AWGN $P_e(\gamma)$ and fading channel probability density function (PDF) $p_\gamma(\gamma)$ as given by [17–23]

$$P_{e\_av}=\int_0^\infty p_\gamma(\gamma)P_e(\gamma)\,d\gamma \quad (12)$$

where $\gamma=\alpha^2E_s/N_0$, and α is the channel fading amplitude.

For the proposed coding scheme, the error probability in the AWGN $P_e(\gamma)$ is evaluated as [24]

$$P_e(\gamma)\le\frac{1}{M}\sum_{j=1}^{M}\sum_{\substack{i=1\\ i\ne j}}^{M}Q\left[\sqrt{\frac{E_s}{N_0}(1-\rho(i,j))}\right] \quad (13)$$

where M is the number of all distinguished symbol patterns, and the Q-function is defined as

$$Q(x)=\frac{1}{\pi}\int_0^{\pi/2}e^{\left(-\frac{x^2}{2\sin^2(\theta)}\right)}d\theta. \quad (14)$$

From (12) and (13), the average probability of error is rewritten as

$$P_{e\_av}=\frac{1}{\pi\bar{\gamma}M}\sum_{j=1}^{M}\sum_{\substack{i=1\\ i\ne j}}^{M}\int_0^{\pi/2}\int_0^{\infty}e^{\left(-\frac{(1-\rho(i,j))\gamma}{2\sin^2(\theta)}-\frac{\gamma}{\bar{\gamma}}\right)}d\gamma\,d\theta. \quad (15)$$

After evaluating the integral over dγ, the average error probability of the Rayleigh fading channel [26–28] for the proposed coding scheme is

$$P_{av}=\frac{1}{\pi\bar{\gamma}M}\sum_{j=1}^{M}\sum_{\substack{i=1\\ i\ne j}}^{M}\int_0^{\pi/2}\left[\frac{2\bar{\gamma}\sin^2(\theta)}{\bar{\gamma}(1-\rho(i,j))+2\sin^2(\theta)}\right]d\theta. \quad (16)$$

4.2 Error Performance Analysis of the Proposed Asynchronous Decoding Techniques

Based on the asynchronous decoding techniques presented in Sec. 3.2, one with an integrator and the other without an integrator, the error performance analysis of the two asynchronous decoding schemes is discussed here.

A. Decoding technique using an integrator

In this case, DSSZ-SM symbols exhibit characteristics similar to those of DSFSC-DCSZ symbols [15]. Specifically, DSSZ-SM symbols can be obtained by vertically flipping and then horizontally flipping DSFSC-DCSZ symbols. Consequently, the energy per bit of both symbol types is equal. Since the decoding of both symbol types results in the same data bits, the error performance analysis of DSSZ-SM is identical to that of DSFSC-DCSZ, as presented in [19]. The error performance of DSSZ-SM decoding using an integrator for additive white Gaussian noise (AWGN) is given by

$$P_{\mathrm{ei}} \simeq Q\left(\sqrt{0.133\frac{E_{\mathrm{bavg}}}{N_0}}\right) \tag{17}$$

and the maximum fading error probability, $P_{\mathrm{ei\,max}}$, of DSSZ-SM decoding using an integrator is given by

$$P_{\mathrm{ei\,max}} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\sin^2(\theta)}{\frac{E_{\mathrm{s}}}{N_0}(0.133)+2\sin^2(\theta)}\,\mathrm{d}\theta\,. \tag{18}$$

B. Decoding technique without using an integrator

The analysis of this technique follows a similar approach to the first technique. However, the time range during which the integration errors occur differs in the first technique, and errors can arise at both the beginning and end of the integration process. In contrast, for this decoding technique, which is based on a sample-and-hold circuit, the error effect is primarily localized to the sampling stage. By assuming that the end of the integration period in the first technique coincides with the beginning of the sampling process in this technique, the noise arises solely from the sampling process, yielding lower noise levels than in the first technique. Assuming that noise in the sampling process is AWGN, it corrupts the data symbols as depicted in Fig. 14.

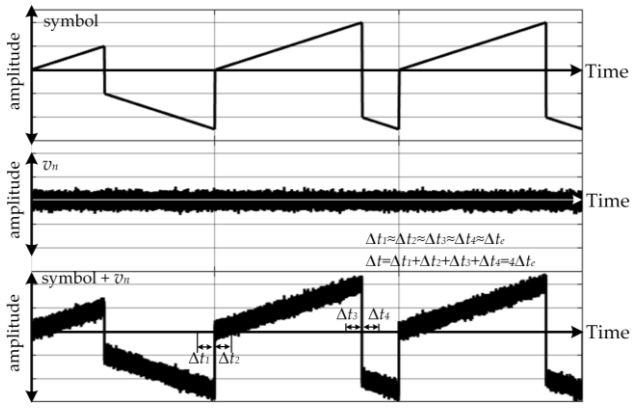


Fig. 14. Illustration of the corrupted data symbols due to the AWGN sampling noise.

Since the deviation in amplitude is related to the timing jitter, and the time jitters occurring within a symbol can be represented as Δt_i for i = 1, 2, 3, 4. These time jitters are approximately equal due to the characteristics of additive white Gaussian noise (AWGN). Let $\Delta t_{\mathrm{e}} = \Delta t_i$ and $\Delta t = 4\Delta t_{\mathrm{e}}$ represent the total time jitter associated with each symbol. During the sampling process, each symbol is sampled at the transition point from the up-slope to the down-slope. If the data symbol is sampled at $t_{\mathrm{s}} + \Delta t_{\mathrm{e}}$, where t_{s} is the actual sampling time, then the sampled voltage is given by

$$\begin{aligned} v_s &= -s\left(t_{\mathrm{s}} + \Delta t_{\mathrm{e}}\right) + v_n \\ &= -st_{\mathrm{s}} - \frac{s\Delta t}{4} + v_n = -st_{\mathrm{s}} - \frac{v_n}{4} + v_n = -st_{\mathrm{s}} + \frac{3v_n}{4}. \end{aligned} \tag{19}$$

From (19), the first term represents the actual sampled value, and the second term represents the additive white Gaussian noise (AWGN) introduced during the sampling process of decoding, which can be expressed as

$$v_{ns} = \frac{3}{4}v_n = \sqrt{2}v_{n\mathrm{sRMS}}. \tag{20}$$

By squaring both sides of (20) and rearranging the expression, we obtain

$$\begin{aligned} \left(\frac{3}{4}\right)^2 v_n^2 &= 2v_{n\mathrm{sRMS}}^2, \\ \frac{N_{0\mathrm{s}}}{N_0} = \frac{2v_{n\mathrm{sRMS}}^2}{v_n^2} &= \left(\frac{3}{4}\right)^2, \\ N_{0\mathrm{s}} &= \left(\frac{3}{4}\right)^2 N_0 \end{aligned} \tag{21}$$

where N_0 and $N_{0\mathrm{s}}$ represent the powers of the AWGN introduced during the integration and sampling processes, respectively.

By substituting N_0 in (17) with $N_{0\mathrm{s}}$ in (21), the error performance of DSSZ-SM decoding without using an integrator for additive white Gaussian noise (AWGN) is given by

$$P_{\mathrm{e}} = Q\left(\sqrt{\frac{0.133E_{\mathrm{b}}}{N_0\left(\frac{3}{4}\right)^2}}\right) = Q\left(\sqrt{\left(\frac{4}{3}\right)^2 0.133\frac{E_{\mathrm{b}}}{N_0}}\right). \tag{22}$$

Similarly, for fading noise [29], [30], the error performance of DSSZ-SM decoding without using an integrator for maximum fading is given by

$$P_{\mathrm{e}\max} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{2\sin^2(\theta)}{\frac{E_\mathrm{s}}{N_0}\left(\left(\frac{4}{3}\right)^2 0.133\right)+2\sin^2(\theta)}\,\mathrm{d}\theta. \quad (23)$$

5. Simulation Results

Following the description of the proposed DSSZ-SM coding and decoding schemes in Sec. 3, these schemes were simulated using MATLAB. The block diagram for encoding and decoding is illustrated in Fig. 15. For the encoding process, frequency modulation is implemented using a VCO with the following parameters: a data bit rate of 75 bits/s, maximum and minimum chirp symbol voltages ($V_{\max}$ and $-V_{\max}$) of 5 V and –5 V respectively, a ramp frequency of 37.5 Hz, a VCO free-running frequency of 25 kHz, and a modulation sensitivity k_{vco} of 2 kHz/V. The simulation result of the encoding process for a 2-bit/chirp symbol is demonstrated in Fig. 16. In Fig. 16, the upper trace shows the analog signal for the four 2-bit data cases (00, 01, 10, and 11), the middle trace displays the resulting DSSZ-SM chirp symbols, and the bottom trace presents the corresponding chirp signals

For the decoding process, the received chirp signals are first demodulated to obtain the DSSZ-SM chirp symbol. Subsequently, the DSSZ-SM symbol is decoded to recover the data as a PWM signal. In this stage, the PWM signal can be retrieved using three techniques, as depicted in the simulated blocks in Fig. 17. The simulation results from each technique are shown in Fig. 18(a)–(c). As shown, the retrieved PWM signals obtained using the three techniques exhibit identical temporal characteristics, differing only in amplitude.

After the PWM signals are retrieved, the data bits are then decoded based on the width of these PWM signals. The proposed techniques for decoding data bits can be implemented with or without an integrator, as shown in the simulated blocks in Fig. 19. The decoded analog levels from both techniques are identical, as illustrated in Fig. 20. These analog levels are subsequently converted to obtain the final data bits. In addition, the two techniques for retrieving clock signals are simulated as shown in Fig. 21, and the simulation results are demonstrated in Fig. 22.

Furthermore, as described in Sec. 4 for the error performance analysis of the proposed schemes, based on the correlation values presented for each symbol pair, the terms involving ω_c and k_{vco} in the denominator of (6)–(11) can be omitted if ω_c and k_{vco} are substantially larger than 1. A summary of the correlation values for each 2-bit symbol pair is provided in Tab. 1. Finally, the relationship between the bit error rate (BER) and energy per bit to noise power spectral density ratio for AWGN and Rayleigh fading is theoretically simulated as shown in Fig. 23.

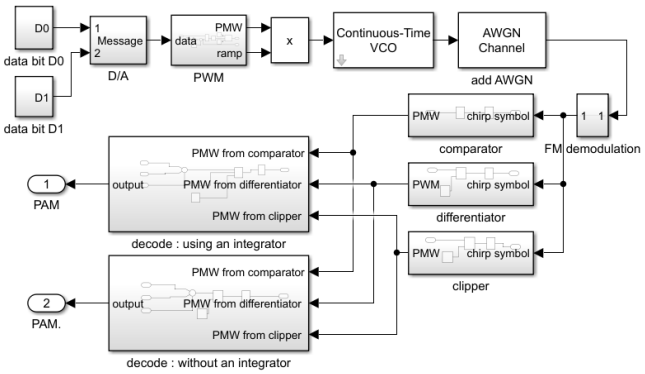


Fig. 15. Block diagram for encoding and decoding the proposed schemes.

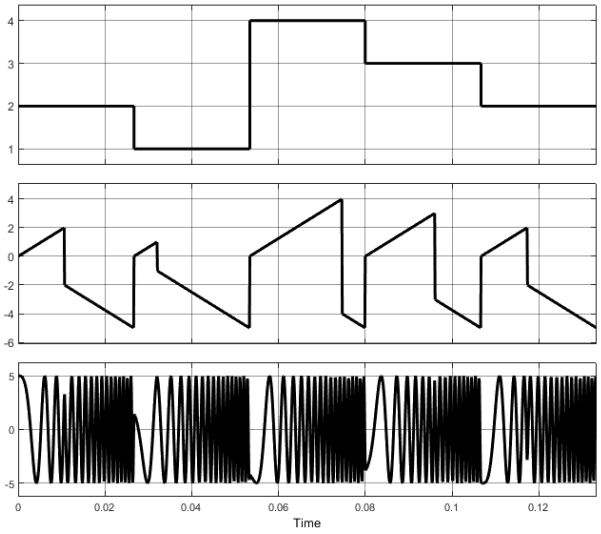


Fig. 16. The simulation result of the encoding part for 2-bit/chirp symbol

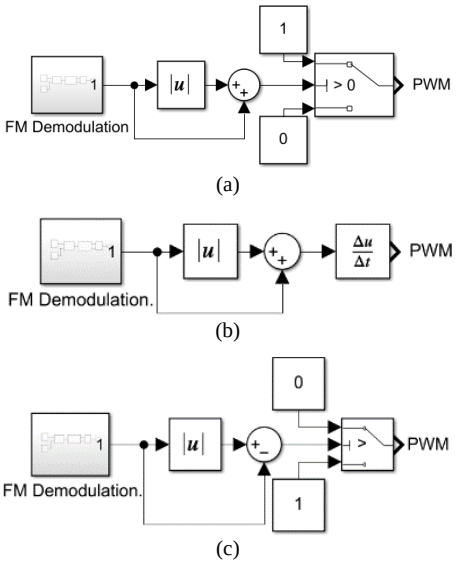
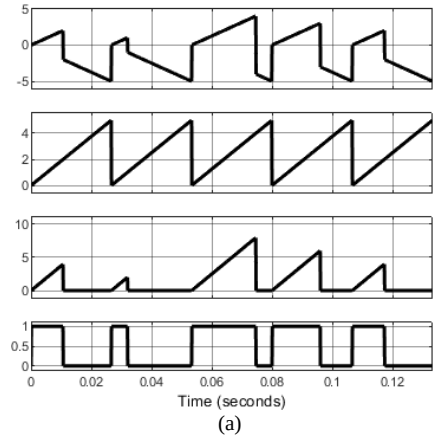
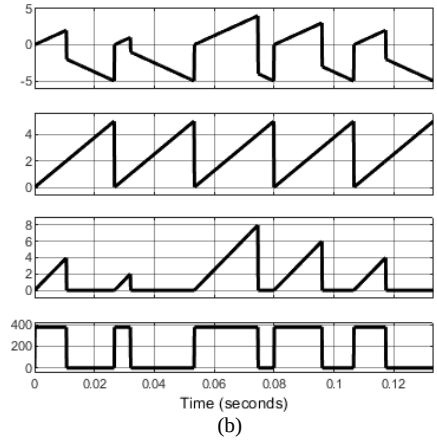


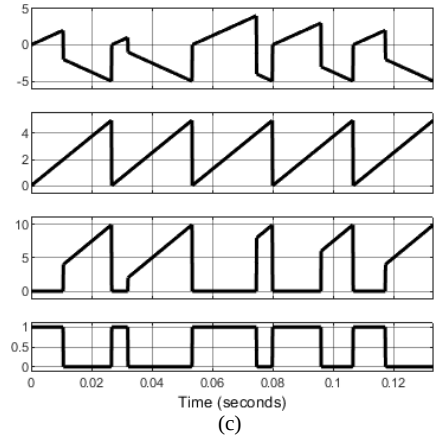
Fig. 17. Block diagram for retrieving the PWM signal using (a) a comparator, (b) a differentiator, and (c) a clipper.



(a)

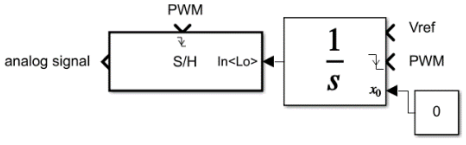


(b)

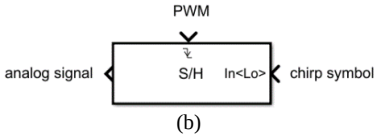


(c)

Fig. 18. The simulation results of the retrieved PWM signal using (a) a comparator, (b) a differentiator, and (c) a clipper.

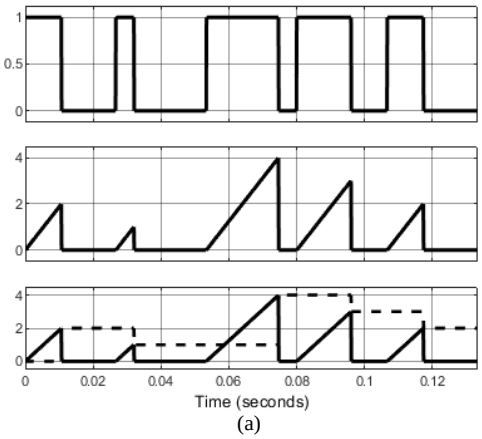


(a)

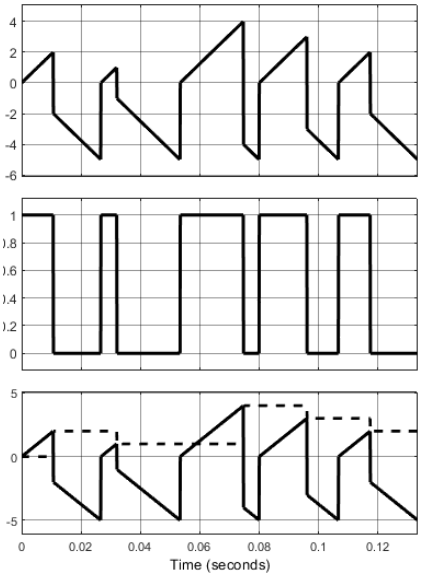


(b)

Fig. 19. Block diagram for decoding data bits of the proposed chirp symbol (a) using an integrator and (b) without an integrator.

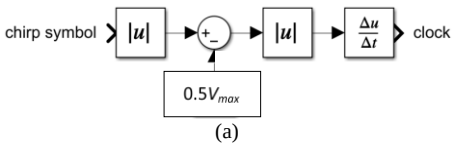


(a)

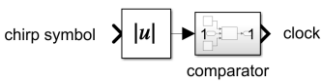


(b)

Fig. 20. The simulation results for decoding data bits of the proposed chirp symbol (a) using an integrator and (b without an integrator.



(a)

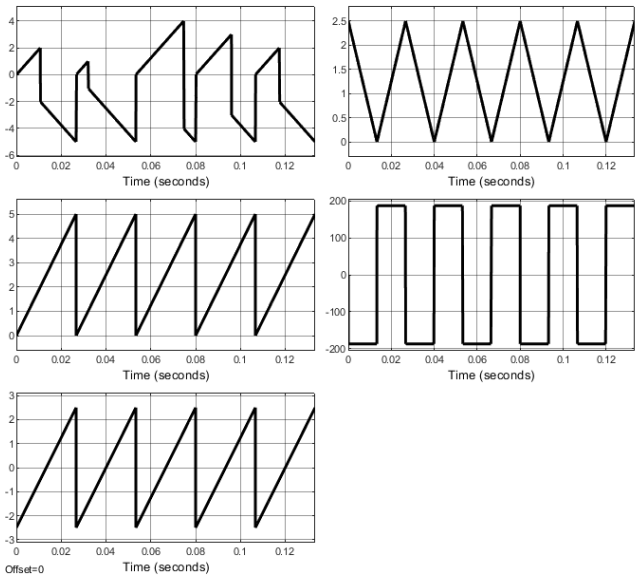


(b)

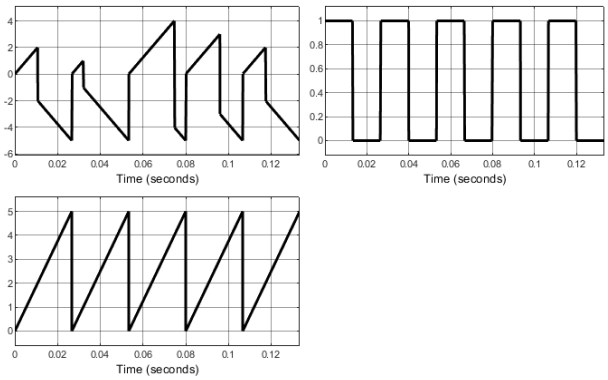
Fig. 21. Block diagram for retrieving the clock signal (a) using a subtractor, an absolute circuit, and a differentiator and (b) using a comparator.

Symbol pairs (s_n, s_m)	$E_s\rho(s_n, s_m)$	$\rho(s_n, s_m)$	$1-\rho(s_n, s_m)$
(s_1, s_2)	$0.4TA^2$	0.8	0.2
(s_1, s_3)	$0.3TA^2$	0.6	0.4
(s_1, s_4)	$0.2TA^2$	0.4	0.6
(s_2, s_3)	$0.4TA^2$	0.8	0.2
(s_2, s_4)	$0.3TA^2$	0.6	0.4
(s_3, s_4)	$0.4TA^2$	0.8	0.2

Tab. 1. The correlation values of each pair of 2-bit symbols.



(a)



(b)

Fig. 22. The simulation results for retrieving the clock signal (a) using a subtractor, an absolute circuit, and a differentiator and (b) using a comparator.

Moreover, Figure 24 presents the numerical results of the bit error rate (2-bit symbol case) for the proposed asynchronous detection techniques, both with and without an integrator, under AWGN and fading noise conditions.

- Fading noise case: The solid line with triangle symbols represents the error performance for the technique using an integrator, while the dashed line with black circles represents the performance for the technique without using an integrator.
- AWGN case: The solid line represents the error performance for the technique using an integrator, and the dashed line represents the performance for the technique without using an integrator.

The results demonstrate that the decoding technique without an integrator exhibits superior error performance compared to the technique that employs an integrator. Furthermore, the error performance of the decoding technique without an integrator, obtained from computer simulation (represented by a curve with circle symbols), was compared with its corresponding numerical result. The numerical and simulation results exhibited good agreement in terms of the error performance.

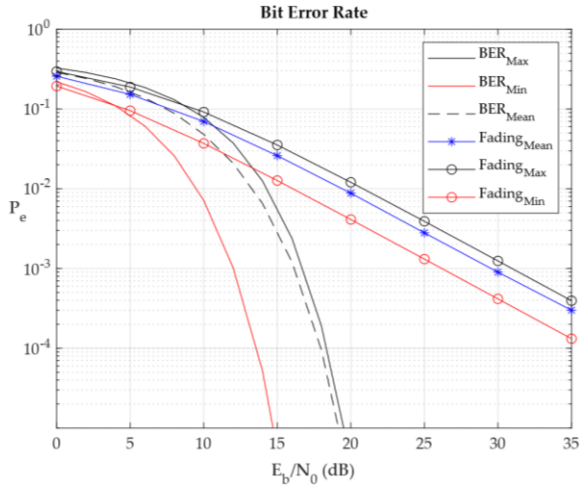


Fig. 23. The theoretical relationship BER versus (E_s/N_0) for AWGN and Rayleigh fading of 2-bit symbols encoding.

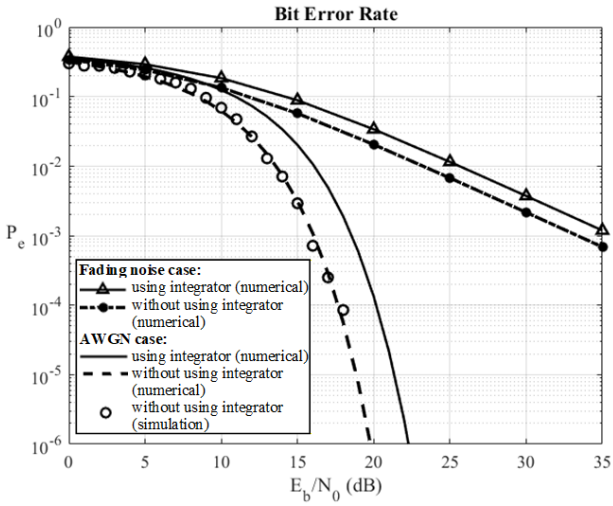


Fig. 24. The numerical results of the BER versus (E_s/N_0) for the proposed asynchronous detection under AWGN and Rayleigh fading of 2-bit symbols encoding.

6. Experimental Results

To validate the proposed DSSZ-SM coding and decoding schemes, circuit experiments are conducted to compare the results with the simulation scenario presented in Sec. 5. It is noted that in the experiment, the LF351 operational amplifiers (op-amps) are powered by a 5V supply, and the resistor R in the circuit has a value of 1 kΩ. The data symbol rate applied to the circuit is 75 bits/s, corresponding to a ramp frequency of 37.5 Hz.

6.1 The DSSZ-SM Encoding

In the encoding process, the DSSZ-SM symbols are generated using the circuit shown in Fig. 25. The circuit consists of a comparator for generating the PWM signal and an inverting amplifier controlled by that PWM signal. The obtained DSSZ-SM chirp symbol compared to the PWM signal are shown in Fig. 26.

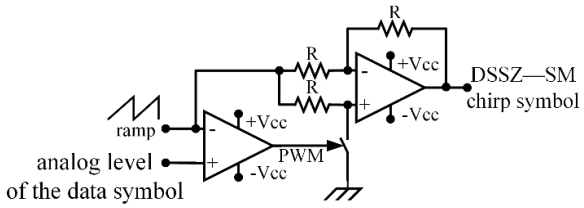


Fig. 25. The DSSM–SM encoding circuit.

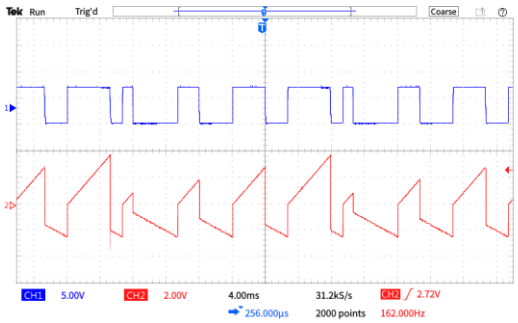
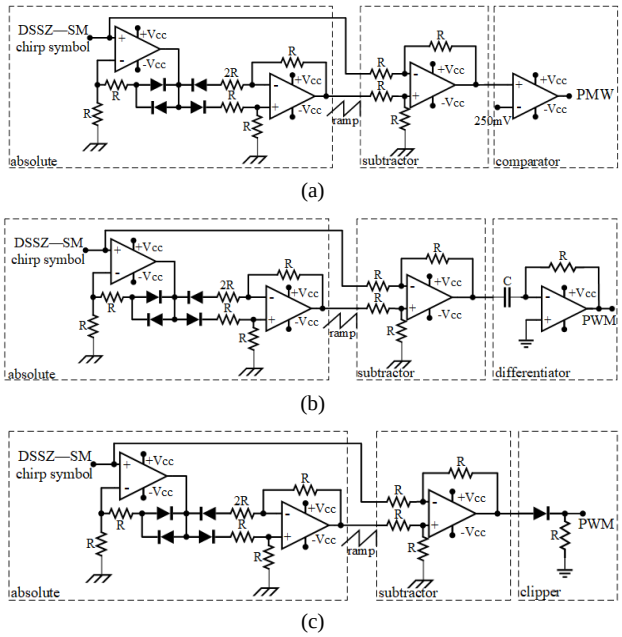


Fig. 26. The experimental results of the DSSM-SM encoding circuit: the PWM signal (upper trace) and the DSSM-SM chirp symbol (lower trace).

6.2 The DSSZ-SM Decoding

In the decoding process, three methods for recovering the PWM signal from the DSSZ-SM chirp symbol, based on a comparator, a differentiator, and a clipper, are tested. The experimental circuits are shown in Figs. 27(a)–27(c), respectively. The diodes used in the depicted circuit are 1N4148, and the R resistors are 10 kΩ. The experimental results comparing the DSSZ-SM chirp symbol and the ramp signal (output of the absolute), and comparing the subtractor output and the PWM signal for the circuits shown in Figs. 27(a)–27(c) are presented in Figs. 28–30, respectively.

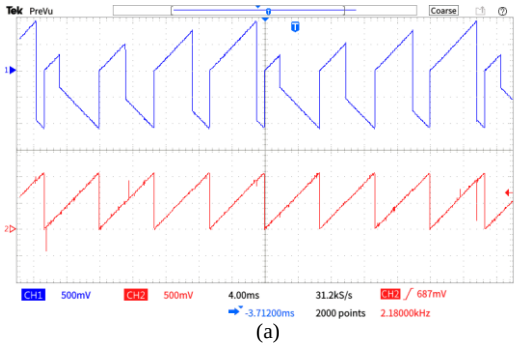


(a)

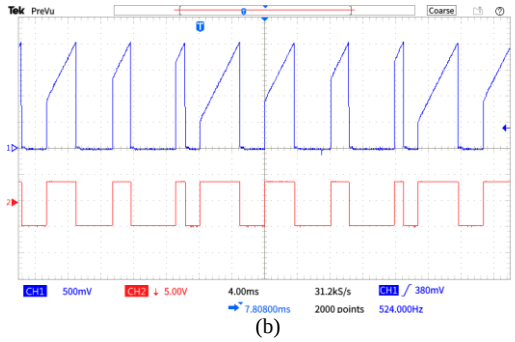
(b)

(c)

Fig. 27. The PWM retrieval circuits (a) using a comparator, (b) using a differentiator, and (c) using a clipper.

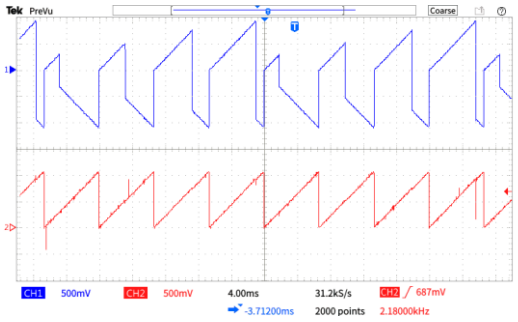


(a)

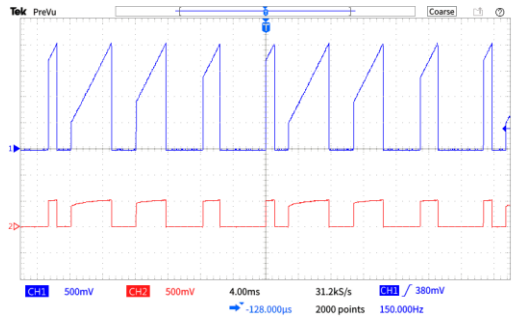


(b)

Fig. 28. The experimental results of the PWM retrieval circuits using a comparator (a) comparing the DSSZ-SM chirp symbol and the ramp signal (output of the absolute) and (b) comparing the output of the subtractor and the PWM signal.



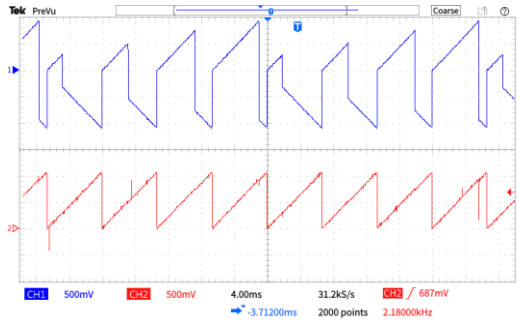
(a)



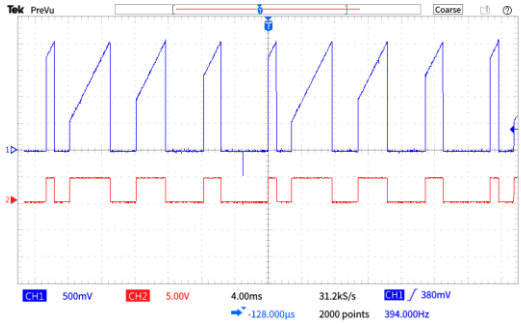
(b)

Fig. 29. The experimental results of the PWM retrieval circuits using a differentiator (a) comparing the DSSZ-SM chirp symbol and the ramp signal (output of the absolute) and (b) comparing the output of the subtractor and the PWM signal.

Later, the data bits are decoded to recover the analog information using two methods, as shown in Fig. 31(a) with an integrator and Fig. 31(b) without an integrator. The experimental results of two decoding methods are presented in Figs. 32 and 33, respectively.

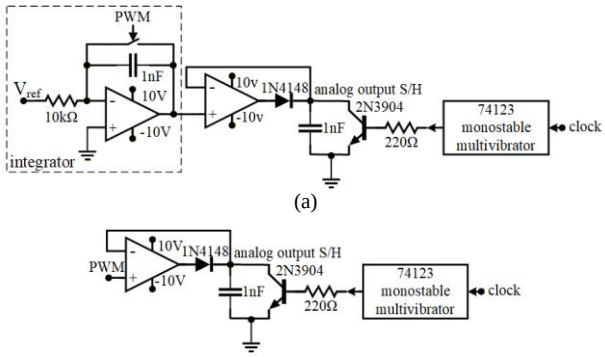


(a)



(b)

Fig. 30. The experimental results of the PWM retrieval circuits using a clipper (a) comparing the DSSZ-SM chirp symbol and the ramp signal (output of the absolute) and (b) comparing the output of the subtractor and the PWM signal.



(a)

(b)

Fig. 31. The data bits decoding circuits (a) using an integrator and (b) without using an integrator.

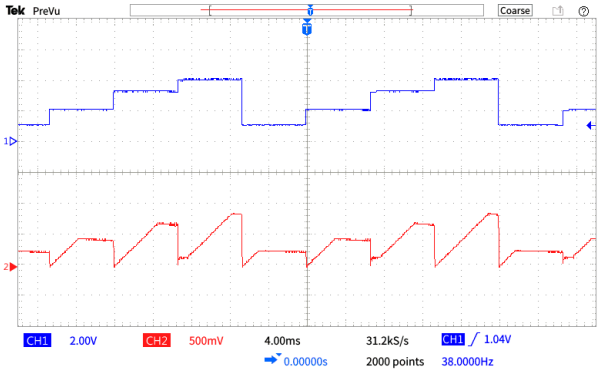
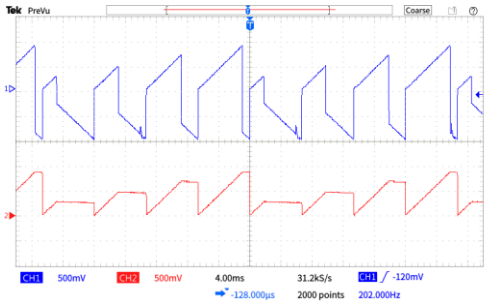
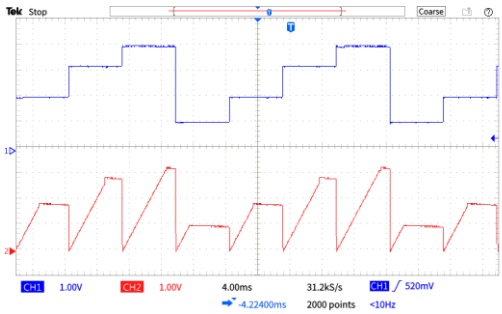


Fig. 32. The experimental results of the data bits decoding circuit using an integrator, comparing the analog data (upper trace) and the sample and hold output, (lower trace), respectively.

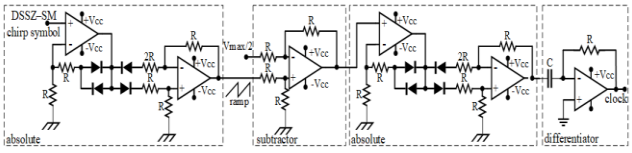


(a)

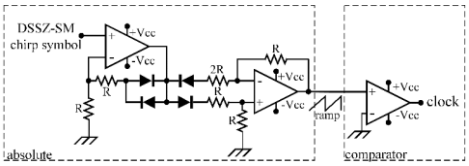


(b)

Fig. 33. The experimental results of the data bits decoding circuit without using an integrator (a) comparing the chirp symbol (upper trace) and the analog data from sample and hold output (lower trace) and (b) comparing the analog data (upper trace) and the analog data from sample and hold output (lower trace).



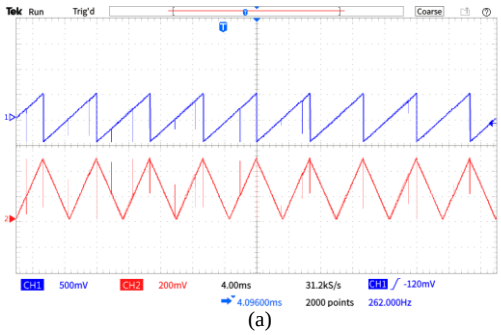
(a)



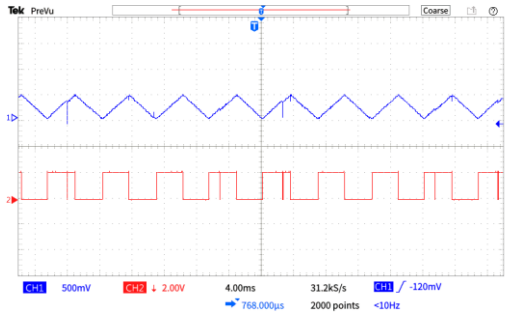
(b)

Fig. 34. The clock retrieval circuits based on (a) an integrator and (b) a comparator.

Moreover, an experiment to retrieve the clock signal is conducted. The clock signal can be recovered using two methods: (a) a differentiator-based circuit and (b) a comparator-based circuit, as shown in Figs. 34(a) and 34(b), respectively.



(a)



(b)

Fig. 35. The experimental results of the clock retrieval circuit based on a differentiator (a) comparing the ramp signal and the absolute output signal and (b) comparing the triangular signal of the absolute output (upper trace) and the retrieved clock signal (lower trace).

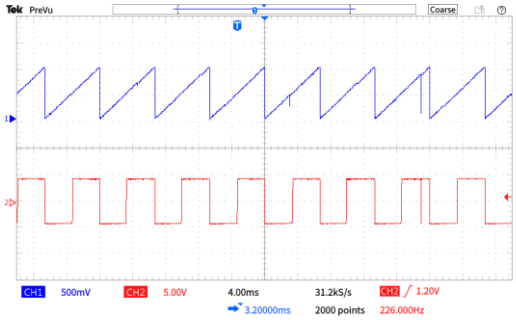


Fig. 36. The experimental results of the clock retrieval circuit based on a comparator, comparing the ramp signal and the retrieved clock signal.

The experimental results of the two clock-retrieval methods are presented in Figs. 35 and 36, respectively.

7. Conclusions

This study proposes a new chirp code, termed Double-Slope Start Zero Stop Minimum (DSSZ-SM), along with a technique for its generation. The proposed coding scheme incorporates a double slope within each chirp symbol, providing inherent synchronization properties. Furthermore, the DSSZ-SM symbol always starts at a zero-voltage level—unlike the scheme presented in [19]—making it simple and low in generation complexity. The proposed symbol has characteristics similar to a semi-PAM-PWM format, where the carrier wave is a sawtooth signal. Decoding of the DSSZ-SM code can be performed using two methods: (1) sampling to detect the peak of each chirp symbol, and (2) integrating to determine its amplitude. Both decoding structures are simple, and data bits are recovered from the extracted PWM signal. In addition, the carrier sawtooth signal can be easily reconstructed using an absolute-value circuit. Theoretical analysis and computer simulations indicate that the decoding method without an integrator achieves superior error performance compared to the integrator-based approach. Moreover, the proposed code is not only simpler and less complex than the method in [19] but also provides comparable performance. The simulation and experimental results are consistent, demonstrating the practical feasibility of the proposed coding and decoding schemes.

The contribution of this work is expected to benefit several real-world applications of chirp coding. For instance, chirp-based signaling is widely employed in modern LoRa-based Industrial IoT systems, where chirp spread spectrum modulation provides robust long-range communication with high noise immunity. In addition, chirp signals are fundamental to FMCW radar systems, which are extensively used in industrial distance measurement, obstacle detection, automotive sensing, and smart manufacturing environments. The proposed DSSZ-SM scheme, with its inherent synchronization property and simple decoding structure, therefore demonstrates strong potential for practical implementation in such contemporary communication and sensing systems.

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About the Authors …

Lerson KIRASAMUTHRANON received B.Eng, M.S. degree in Telecommunication Engineering and D.Eng. degree in Electrical Engineering from King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 2009, 2012 and 2016, respectively. His research interests include analog circuits in telecommunication systems and digital signal processing.

Paramote WARDKEIN received his M.E. and D.Eng. degree in Electrical Engineering from King Mongkut's Institute of Technology Ladkrabang (KMITL), Bangkok, Thailand, in 1990 and 1997, respectively. He is now an Associate Professor of Telecommunications Engineering Department, Faculty of Engineering, (KMITL), Thailand. Thailand. His research interests include analog circuits in telecommunication systems and digital signal processing.

Jeerasuda KOSEEYAPORN graduated M.S. and Ph.D. degrees in Electrical Engineering from Vanderbilt University, Nashville, TN, USA, in 1999 and 2003, respectively. Currently, she is an Associate Professor of Telecommunications Engineering Department, Faculty of Engineering, (KMITL), Thailand. The research interests are in the areas of analog circuits in telecommunication systems and digital signal processing.