Time-to-Digital Converter Combining Multiphase Ring Oscillator and 2-D Vernier Conversion Principle

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Abstract. *This paper presents a novel timestamp-oriented Time-to-Digital Converter (TDC) architecture that combines a continuously running Phase-Locked Loop (PLL)-stabilized multiphase Ring Oscillator (RO) with a Two-Dimensional Vernier Time-to-Digital Converter (2D-VTDC). Unlike conventional continuously running ROs-based TDCs, where the achievable resolution is directly limited by the delay of a single RO stage, the proposed approach preserves continuous PLL-based stabilization while achieving a resolution finer than the intrinsic delay of a single RO stage. The RO provides a low-jitter coarse time base and scalable Dynamic Range (DR) through a counter, whereas the 2D-VTDC performs fine interpolation between oscillator phases. Consequently, the effective timing resolution is decoupled from the intrinsic delay of a single RO stage. This allows significantly slower delay cells to be employed while maintaining fine timing resolution, potentially reducing switching activity and easing the implementation of high-resolution TDCs. The architecture is particularly suitable for timestamp-based Time-of-Flight (ToF) measurements, such as ultrasonic flow metering, where low jitter and single-shot measurement accuracy are critical. A systematic design methodology is presented, and behavioral simulations demonstrate the feasibility of the proposed architecture.*

Keywords

Ring oscillator, time-to-digital converter, two-dimensional Vernier, timestamping, ultrasound flow-meter

1. Introduction

Ultrasound flow meters estimate flow by measuring the difference in Time-of-Flight (ToF) of acoustic pulses travelling with and against the fluid stream, as illustrated in Fig. 1(a). The measurement concept and zero-crossing timestamp extraction are shown in Fig. 1(b). Because the flow estimate is directly proportional to the measured ToF difference, the achievable flow accuracy strongly depends on the resolution (Least Significant Bit (LSB), denoted Δ) and precision of the underlying time measurement. Consequently, picosecond-level timing resolution is required over a Dynamic Range (DR) spanning from the minimum distinguishable time interval to the maximum measurable interval, typically reaching tens of microseconds.

Typical implementation digitizes the received waveform using a High-Speed Analog-to-Digital Converter (HS-ADC) and estimates the ToF using Digital Signal Processing (DSP) techniques such as threshold detection, cross-correlation, or pattern matching [1–3]. This approach is highly flexible because the complete waveform is available for analysis and compensation of signal distortions.

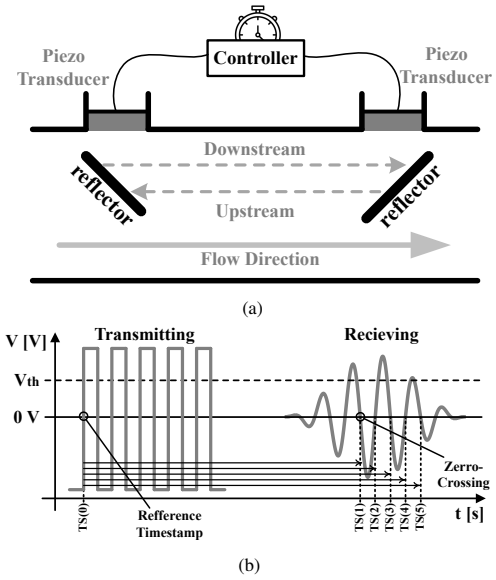


Fig. 1. (a) Longitudinal cross-sectional view of the conceptual ultrasound flow-meter configuration with two transducers and reflectors; (b) Example received waveform showing zero-crossing events and extracted timestamps.

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However, the required sampling rates, memory resources, and DSP computations often result in substantial power consumption, which can become a limiting factor in battery-powered and energy-constrained applications.

Although a Time-to-Digital Converter TDC can significantly reduce the energy required for timestamp extraction, it should be regarded as a low-power alternative rather than a complete replacement for waveform digitization. Accurate ToF estimation requires the identification of a suitable timing reference point, typically defined by a threshold crossing as illustrated in Fig. 1(b). In practical systems, the received waveform may be distorted by transducer nonidealities, attenuation, multipath propagation, temperature variations, reflections from discontinuities, and interference from previous echoes. Consequently, the optimal threshold voltage V_{th} cannot always be predetermined.

For this reason, the received waveform must first be observed using an HS-ADC, allowing the signal shape to be analyzed and a suitable threshold level to be identified. Once an appropriate threshold has been established, subsequent measurements may be performed using a significantly more energy-efficient TDC, provided that the waveform shape remains sufficiently stable over time. The limitations of threshold-based ToF extraction and its combination with cross-correlation techniques are discussed in [4]. In this context, the TDC acts as an efficient timestamping engine that replaces continuous waveform digitization during normal operation while preserving the accuracy established during the calibration or initialization phase.

For ToF applications, a TDC should provide picosecond-level resolution, tens of microseconds of DR scalable to different pipe lengths, a sufficient sampling rate to capture zero crossings, low jitter, and good linearity across the entire measurement range. Ideally, the target resolution should be achieved without relying on aggressive quantization-noise shaping, since the resulting improvement in effective resolution often requires a large number of repeated measurements and subsequent averaging. Such averaging increases latency and overall system energy consumption, which is undesirable in low-power sensing systems.

Among the architectures reported in the literature, Ring Oscillator (RO)-based TDCs offer an attractive combination of scalability, large DR, compact implementation, and compatibility with modern CMOS technologies. However, achieving picosecond-level resolution often requires architectural modifications that increase conversion latency, complicate oscillator stabilization, or reduce timestamping capability.

This paper presents a timestamp-oriented TDC architecture that combines a continuously running Phase-Locked Loop (PLL)-stabilized multiphase RO with a Two-Dimensional Vernier Time-to-Digital Converter (2D-VTDC). The objective is to achieve sub-stage-delay resolution while preserving continuous oscillator stabilization and the advantages of a timestamp-based measurement approach. By separating coarse time generation from fine interpolation, the proposed architecture enables the use of slower delay stages without sacrificing timing resolution, potentially reducing power consumption while maintaining low jitter.

The remainder of this paper is organized as follows. Section 2 reviews representative RO-based TDCs architectures and introduces the motivation for the proposed solution. Section 3 presents the proposed architecture together with its mathematical description and design methodology. Section 4 provides behavioral simulation results, and Section 5 concludes the paper.

2. Ring Oscillator TDCs Overview

This section reviews representative RO-based TDC architectures and outlines their evolution from basic ROs-TDCs to advanced Vernier-based solutions. The discussion is intentionally limited to a brief overview of the most relevant architectures in order to highlight the development path leading to the proposed topology and the associated design trade-offs. A more comprehensive review of RO-based TDCs is available in [5].

2.1 Basic Ring Oscillator TDC

The simplest RO-based TDC [6] consists of a ring oscillator, a counter, and snapshot logic that captures the states of the oscillator nodes together with the counter value upon the arrival of a Start/Stop, as illustrated in Fig. 2. Such a ring oscillator can be driven by a PLL, which significantly reduces its jitter [7]. As the ring is continuously running, first order noise shaping is available.

The main drawback of this approach is the high activity of the continuously running oscillator, where the achievable resolution Δ is fundamentally limited by the delay of a single inverter. At one extreme, the oscillator may consist of only three inverters paired with a high-speed counter. At the other extreme, a larger number of inverter stages can be used, allowing the use of a slower and more energy-efficient counter. Nevertheless, a state transition occurs in one of the oscillator stages every Δ, resulting in considerable power consumption. Such TDCs are particularly suitable for timestamping applications, where timestamps can be acquired at a very high rate over virtually unlimited measurement intervals and subsequently processed in the digital domain, for example by addition, subtraction, or averaging.

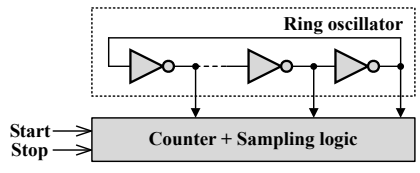


Fig. 2. Ring oscillator-based TDC.

2.2 Gated/Switched-Ring Oscillator TDC

A common approach to reducing power consumption is oscillator gating [8] or supply switching [9], where the oscillator supply voltage is reduced during idle periods to minimize energy consumption. The oscillator is enabled, or switched to its nominal supply voltage, by a Start signal and disabled, or returned to the reduced supply level, by a Stop signal, as illustrated in Fig. 3. Compared to simple gating, supply switching offers additional benefits, including reduced skew, reduced leakage-related effects, and mitigation of several nonidealities associated with the gating process [9]. Depending on the implementation, gated or switched-ring architectures may also exploit first-order noise shaping [8], [9]. However, continuous PLL-based jitter suppression is generally not possible because the oscillator repeatedly starts and stops. The resolution Δ remains limited by the inverter delay of the target technology. Nevertheless, the achievable sampling rate is relatively high, while the DR can be extended straightforwardly by increasing the counter width.

2.3 Vernier Ring Oscillator TDC

To overcome the resolution limitation imposed by the inverter delay, the Vernier RO TDC architecture shown in Fig. 4 was developed. In the literature, similar architectures are referred to as cyclic Vernier TDCs, gateable Vernier RO, or Vernier RO, depending on the particular implementation [10–12]. The architecture consists of two oscillators operating at slightly different frequencies. The effective time resolution is determined by the difference between their oscillation periods and can reach the order of a few picoseconds.

The measurement principle is based on the evolution of the relative phase between the two oscillators. Following the arrival of the Start signal, the oscillators begin propagating phase states, while the Stop signal initiates the fine measurement phase. Owing to the slightly higher oscillation frequency of one oscillator, the phase difference gradually decreases until a predefined alignment condition is detected. The measured time interval is then reconstructed from the oscillator phases and the values stored in the associated counters.

A significant drawback of Vernier RO TDCs is their relatively long conversion time. As the frequency difference between the oscillators decreases, the achievable resolution improves; however, the time required for phase alignment increases accordingly. Consequently, the maximum conversion rate is limited. To further improve the achievable resolution, residue extraction, amplification, and reinjection techniques are often employed [13–15].

2.4 2-D Vernier Ring Oscillator TDC

The conversion time can be reduced by employing a two-dimensional organization of the cyclic Vernier TDC, where the slower RO is arranged along the x-axis and the faster one along the y-axis around the Readout Matrix (RM) [16], as illustrated in Fig. 5. Most reported implementations employ gated oscillators, which complicates continuous PLL-based stabilization and may increase sensitivity to oscillator jitter. As a result, a large number of measurements and subsequent averaging are often required, which may be undesirable in low-power systems.

On the other hand, the delay cells can be significantly slower because the resolution of the two-dimensional Vernier architecture is determined by the difference between delays rather than by their absolute values [17]. This can reduce switching activity during conversion and thus lower power consumption.

2.5 Two Step TDC

Another interesting approach published in [18] combines a RO and a Tapped Delay Line (TDL) in a two-dimensional organization based on the two-dimensional Vernier TDC (2D-VTDC) conversion principle. A more detailed discussion of the 2D-VTDC is provided in the following chapter.

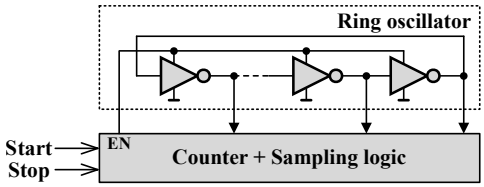


Fig. 3. Gated ring oscillator-based TDC.

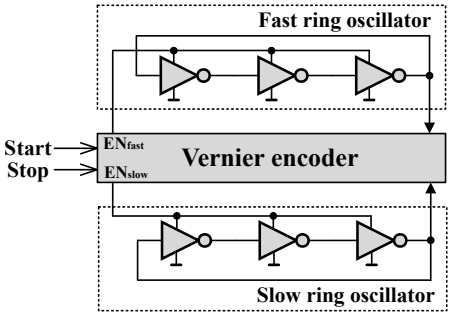


Fig. 4. Vernier ring oscillator TDC.

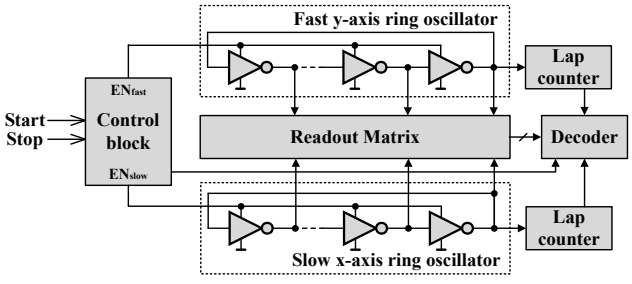


Fig. 5. Two-dimensional Vernier ring oscillator TDC.

In this architecture, the ring oscillator forms the coarse-conversion stage, while a Tapped Delay Line (TDL) together with a two-dimensional Vernier provides fine interpolation as illustrated in Fig. 6. At the beginning of a conversion, the Start signal generates a pulse that is injected into the ring structure. The pulse continuously propagates through the delay ring and its circulation is tracked by a counter, providing coarse time quantization and dynamic-range extension.

Once the measured interval residue falls within the range of the fine converter, a dedicated RO/2D control signal reconfigures the architecture. The circulating pulse is then allowed to propagate into an additional delay chain through a multiplexer, effectively transforming the RO into a TDL structure. Upon the arrival of the Stop signal, a second pulse is launched into the y-axis TDL. Fine time conversion is subsequently performed using the two-dimensional Vernier principle, where the position of the pulse originating from the ring path is resolved relative to the pulse propagating through the y-axis delay line.

As a result, the coarse measurement range is determined by the ring period and the counter value, whereas the fine resolution is provided by the TDL-based 2D-VTDC conversion principle. The architecture further incorporates a reconfigurable RM. Periodic modification of its configuration effectively averages the characteristic Differential Non-Linearity (DNL) peaks typically observed in two-dimensional Vernier architectures [19].

The most apparent drawback remains the need to stop and restart the oscillator, which prevents PLL locking and therefore does not mitigate oscillator jitter.

The topology proposed in the following chapter was designed with these advantages and disadvantages in mind. It targets low-power applications where extensive averaging through repeated measurements is not feasible. Such systems require low self-jitter, sufficiently fine resolution, and an adequate sampling rate. Unlike many previously discussed architectures, the proposed solution prioritizes low intrinsic jitter over noise shaping, making it particularly suitable for applications where single-shot measurement performance is critical.

One promising application is an ultrasonic flow meter, where the proposed architecture can exploit its combination of high precision, low power consumption, and moderate sampling-rate requirements. A comparison of the key characteristics of the reviewed architectures and the proposed topology is summarized in Tab. 1.

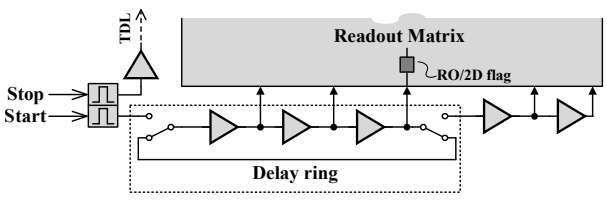


Fig. 6. Two step TDC, adopted from [18].

3. Timestamp-Based Architecture

This section first reviews the well-established TDL-based 2D-VTDC in order to provide the mathematical background necessary for understanding the proposed architecture. Subsequently, a novel timestamp-oriented TDC architecture combining a continuously running multiphase RO with the 2D-VTDC principle is presented. The proposed approach preserves the total dynamic range (DR_{tot}) determined by the counter width while achieving a fine resolution defined by the Vernier principle. Finally, two complementary design methodologies are introduced to facilitate practical implementation of the architecture under different design constraints.

3.1 2-D Vernier TDC Fundamentals

The 2D-VTDC is derived from the One-Dimensional Vernier TDC and belongs to the same family of sampling TDCs capable of achieving sub-gate resolution (for details, see [20]). Compared to its predecessor, it offers higher sampling rates, potentially lower power consumption during measurement, and higher DR while maintaining both TDL lengths.

A representative configuration is shown in Fig. 7. Let the length (number of taps) of the x-axis slow TDL (x-axis Tapped Delay Line (X-TDL)) be denoted as n_{x} and the length of the y-axis fast TDL (y-axis Tapped Delay Line (Y-TDL)) as k. To ensure proper operation, the delays within the y-axis delay line (τ_{y}) must satisfy the relationship with x-axis delay-line delays (τ_{x}) given by

$$(k-1)\cdot\tau_{\text{x}} = k\cdot\tau_{\text{y}}, \tag{1}$$

which is readily achievable with the aid of an arbiter within the RM, enumerated as 0. Both active edges should be aligned when both inputs Start and Stop are shorted together and excited by a pulse source.

The linear DR of the resulting RM (in thermometric code format) can be expressed as

$$DR_{\text{RM}} = \tau_{\text{x}}\cdot(n_{\text{x}}-1) + \tau_{\text{y}}\cdot(3-k), \tag{2}$$

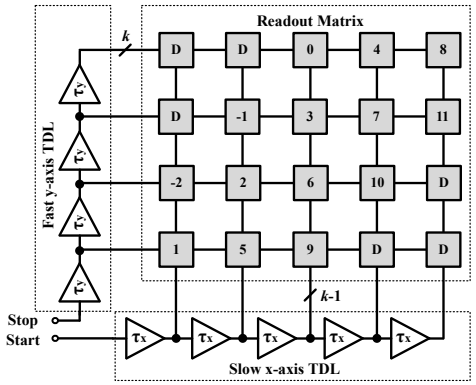


Fig. 7. Tapped Delay Line-based conventional Two-Dimensional Vernier Time-to-Digital Converter with $k = 4$ and $n_{\text{x}} = 5$, showing linear dynamic range from -2Δ to 11Δ.

Architecture	Resolution	PLL lockable	Conversion latency	Key improvement	Ref.
Ring oscillator	Inverter delay limited	Yes	Short	Baseline architecture.	[6], [7]
Gated/Switched RO	Inverter delay limited	No	Short	Reduced power consumption.	[8], [9]
Vernier RO	Sub-inverter	No	Long	Resolution beyond inverter delay.	[10–15]
2-D Vernier RO	Sub-inverter	No	Moderate	Reduced Vernier RO conversion latency.	[16]
Two-step from [18]	Sub-inverter	No	Moderate	Combines RO and 2D-VTDC with RO-to-TDL conversion.	[18]
Proposed architecture	**Sub-inverter**	**Yes**	**Moderate**	**Combines RO and 2D-VTDC without RO-to-TDL conversion.**	**This work**

Tab. 1. Evolution of representative ring oscillator-based TDC architectures highlighting the key improvements leading to the proposed topology.

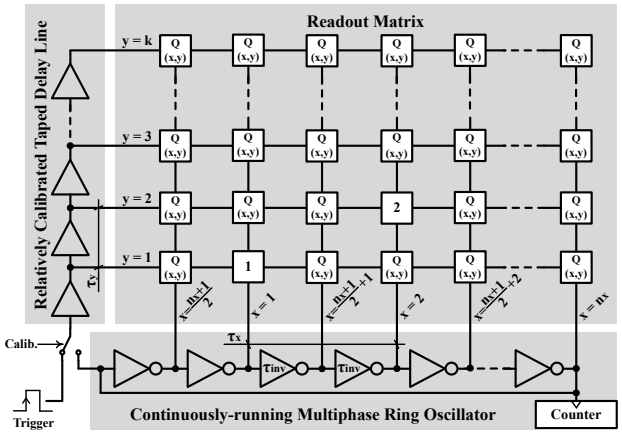


Fig. 8. Proposed time-to-digital converter architecture combining a ring oscillator and the two-dimensional Vernier principle.

while the resolution (LSB) is given by

$$\Delta = \tau_x - \tau_y. \tag{3}$$

Consequently, the maximum measurable interval within a single readout matrix is determined by (2), while the resolution is determined by (3). This enables the 2D-VTDC to achieve a larger linear range than its one-dimensional counterpart without sacrificing resolution.

3.2 Proposed Novel TDC Architecture

The proposed architecture, shown in Fig. 8, combines direct latching of the states of a continuously running RO with the 2D-VTDC conversion principle described in the previous subsection. The key innovation consists in replacing the conventional X-TDL of the 2D-VTDC with a multiphase RO synchronized to a PLL. Consequently, the architecture enables direct RO phase sampling while retaining the fine resolution of the Vernier principle and preserving a total dynamic range (DR_{tot}) determined solely by the counter width.

In the proposed implementation, one tap with delay τ_x is realized using two inverters with delays

$$\tau_{\text{inv}} = \frac{\tau_x}{2} \tag{4}$$

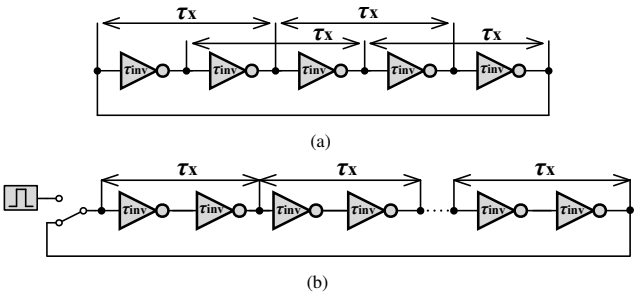


Fig. 9. Comparison of ring-oscillator topologies. (a) Proposed multiphase ring oscillator. (b) Conventional delay-based ring oscillator.

where one inverter is shared by two adjacent taps. The resulting topology, referred to as a multiphase RO, is illustrated in Fig. 9(a).

This arrangement effectively doubles the number of observable phases for a given physical ring length. Consequently, the oscillation period increases only half as fast as in a conventional delay-based RO used in [18], illustrated in Fig. 9(b). As will be demonstrated below, this property is the key enabler of a feasible design while preserving the resolution of the Vernier converter.

For comparison, consider a RO formed by connecting the output of a delay line back to its input and excited by a pulse of appropriate width, as shown in Fig. 9(b). This configuration, previously employed in [18], is referred to here as a delay-based RO.

The fundamental requirement of the proposed architecture is the ability to capture at least one propagating RO edge and thereby determine the oscillator phase with the resolution established by (3). Consequently, the dynamic range of the RM (DR_{RM}) must cover at least one half of the RO period,

$$DR_{\text{RM}} \geq \frac{T_{\text{RO}}}{2}. \tag{5}$$

For the delay-based RO, the oscillation period is

$$T_{\text{RO,db}} = 2 \cdot n_x \cdot \tau_x = 4 \cdot n_x \cdot \tau_{\text{inv}} \tag{6}$$

whereas for the proposed multiphase RO

$$T_{\text{RO,mp}} = 2 \cdot n_x \cdot \tau_{\text{inv}}. \tag{7}$$

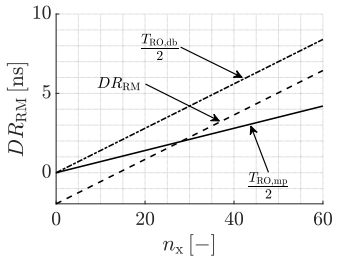


Fig. 10. Representative example for $\tau_{\mathrm{x}} = 140\,\mathrm{ps}$ and $\Delta = 10\,\mathrm{ps}$. DR_{RM}, $T_{\mathrm{RO,db}}/2$ and $T_{\mathrm{RO,mp}}/2$ as a function of n_{x}.

Therefore, for the same number of observable taps n_{x}, the multiphase topology reduces the oscillation period by a factor of two.

For the delay-based RO, one half of the oscillation period is

$$\frac{T_{\mathrm{RO,db}}}{2} = n_{\mathrm{x}} \cdot \tau_{\mathrm{x}}. \tag{8}$$

Both quantities are linear functions of n_{x} with an identical slope

$$\frac{\partial DR_{\mathrm{RM}}}{\partial n_{\mathrm{x}}} = \frac{\partial (T_{\mathrm{RO,db}}/2)}{\partial n_{\mathrm{x}}} = \tau_{\mathrm{x}}. \tag{9}$$

Consequently, the DR_{RM} characteristic and the $T_{\mathrm{RO,db}}/2$ characteristic are parallel and therefore never intersect. Since condition (5) can only be satisfied at their intersection, no valid solution exists for a delay-based RO while preserving the Vernier resolution. This represents a fundamental limitation of this topology.

In contrast, the half-period of the multiphase RO increases with only one half of the slope of the delay-based RO. Therefore, for sufficiently large values of n_{x}, an intersection with the DR_{RM} characteristic always exists, yielding a feasible design point. A representative example for $\tau_{\mathrm{x}} = 140\,\mathrm{ps}$ and $\Delta = 10\,\mathrm{ps}$ is shown in Fig. 10.

Because the RO operates continuously, D Flip-Flop (D-FF)-based arbiters must be employed. Their ability to retain the sampled state regardless of subsequent activity at their data inputs makes them suitable for this application. The active edge propagating through the Y-TDL drives the clock inputs of the D-FFs within the RM and samples the instantaneous states of the RO taps. The sampled values remain unchanged until they are read by the digital back-end.

Conventional RS-latch-based arbiters used in TDL-based TDCs cannot be employed in this architecture. In conventional TDL implementations, both delay lines remain static during readout. In the proposed architecture, however, the RO continues oscillating after sampling. Consequently, the outputs of RS-latches may change due to ongoing RO activity, leading to loss of the captured timing information.

As a consequence of the multiphase RO topology, the RM organization differs from that of the conventional 2D-VTDC shown in Fig. 7. The required ordering of quantization bins can nevertheless be restored digitally according to

$$Q(x, y) = x \cdot k - y \cdot (k - 1) \tag{10}$$

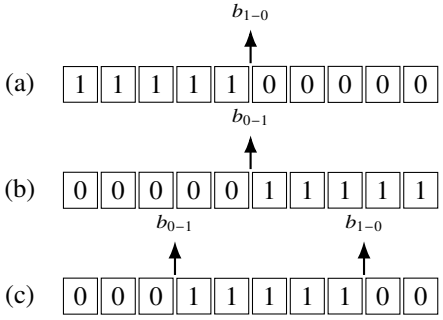


Fig. 11. Possible output-bus patterns after reordering of the readout matrix: (a) a single $1 \rightarrow 0$ transition; (b) a single $0 \rightarrow 1$ transition; and (c) simultaneous occurrence of both transitions.

where Q denotes the quantization step assigned to the arbiter located at coordinates (x, y) within the RM.

The measurement principle is based on sampling the RO states with precision determined by the 2D-VTDC through the Y-TDL excited by the trigger edge. After proper calibration of the Y-TDL, several output-bus patterns may occur depending on the relative timing between the trigger edge and the RO phase as shown in Fig. 11.

For dead-zone-free operation, the most important cases are those containing a single 1-to-0 transition or a single 0-to-1 transition. Assuming the rising edge is used as the counter reference, the timestamp associated with a detected 1-to-0 transition is

$$TS_{1-0} = CNTR \cdot T_{\mathrm{RO,mp}} + b_{1-0} \cdot \Delta \tag{11}$$

where $CNTR$ denotes the counter value at the arrival of the trigger edge and b_{1-0} represents the detected transition position.

For a detected 0-to-1 transition, an additional half-period offset must be included,

$$TS_{0-1} = (CNTR + 0.5) \cdot T_{\mathrm{RO,mp}} + b_{0-1} \cdot \Delta. \tag{12}$$

If the resulting DR_{RM} exceeds one half of the RO period, both transitions may be observed simultaneously. Such cases can potentially be exploited for metastability detection or timestamp averaging.

Despite its advantages, the proposed architecture introduces several design challenges. Using slower delay cells can reduce power consumption, but may also produce slower signal edges whose transition times become comparable to several LSBs. These slow edges can increase cross-currents in the front-end inverters of the readout D-FFs, causing supply-voltage fluctuations that may adversely affect the timing stability of the RO. Furthermore, because the readout D-FFs are not individually threshold-calibrated, the architecture is susceptible to threshold mismatch and noise, which can cause additional DNL. This effect becomes more pronounced with slow edges, as the sampling decision becomes increasingly sensitive to threshold variations. Consequently, neighboring sampling elements may occasionally resolve the same signal edge in the wrong order, resulting in non-monotonic code

transitions and degraded linearity. Finally, achieving uniform phase spacing in the multiphase RO requires careful physical implementation because the feedback interconnect is inherently longer than the local interconnects between adjacent stages. The resulting delay imbalance may introduce phase non-uniformity and further degrade linearity. Careful circuit design and layout optimization are therefore required to fully exploit the benefits of the proposed approach.

A detailed design methodology is presented in the following subsection.

4. Novel TDC Design Methodology

In this section, two complementary design methodologies are introduced. Both approaches aim to determine the missing architectural parameter, such as n_x, based on the fundamental design constraint expressed by (5) while simultaneously satisfying the additional condition

$$\frac{T_{RO,mp}}{2 \cdot \Delta} \in \mathbb{N} \tag{13}$$

in order to prevent DNL from exceeding half the LSB when an inactive edge, from a counter point of view, is captured.

4.1 Resolution-Constrained Design

The first methodology assumes that the achievable RO frequency is practically unconstrained, for example due to a finely tunable PLL reference clock or sufficiently fine PLL division ratios. Consequently, the oscillation frequency is not treated as a design input. Instead, the primary design parameters are the target resolution Δ and the achievable delay of one x-axis stage τ_x.

The first step is the determination of parameter k from (1) and (3) as

$$k = \frac{\tau_x}{\Delta}. \tag{14}$$

Subsequently, the corresponding y-axis delay can be obtained as

$$\tau_y = (k-1) \cdot \Delta. \tag{15}$$

By rearranging (5) with the aid of (2) and using the relation

$$T_{RO,mp} = n_x \cdot \tau_x = n_x \cdot k \cdot \Delta, \tag{16}$$

the minimum required value of n_x, while simultaneously satisfying (13), can be expressed as

$$n_x = \left\lceil 2 \cdot k - 6 - \frac{6}{k} \right\rceil + \mathrm{mod}(k, 2) \tag{17}$$

where $\lceil a \rceil$ denotes the ceiling function and the term $\mathrm{mod}(k, 2)$ ensures satisfaction of (13). Once k, τ_y, and n_x have been determined, the resulting RO frequency can be calculated directly from (7) as

$$f_{RO,mp} = \frac{1}{n_x \cdot \tau_x}. \tag{18}$$

4.2 Frequency-Constrained Design

In practical implementations, only a fixed reference frequency (e.g., provided by a crystal oscillator) is typically available, and the PLL division ratios are limited. For such scenarios, a frequency-constrained design methodology is proposed, where the primary input parameter is the RO frequency $f_{RO,mp}$.

With this approach, the exact target resolution Δ may not be achievable; however, the resulting resolution may be equal to or better than the specified requirement. The architecture parameters n_x and k are determined using a simple iterative algorithm based on two governing equations.

The first equation follows from (3), where $\tau_x = \frac{1}{n_x \cdot f_{RO,mp}}$, and τ_y is obtained by rearranging (1). After algebraic manipulation, the resulting expression is

$$n_{x1} = \left\lceil \frac{1}{k \cdot f_{RO,mp} \cdot \Delta} \right\rceil. \tag{19}$$

The second equation is derived from (5), analogously to the resolution-constrained case, yielding

$$n_{x2} = \left\lceil 2 \cdot k - 6 - \frac{6}{k} \right\rceil, \tag{20}$$

and the final value of n_x is determined as

$$n_x = \max(n_{x1}, n_{x2}). \tag{21}$$

The iterative algorithm can further incorporate constraints related to conversion time (linked to k and τ_y), power consumption (by imposing a lower bound on τ_x to avoid excessively high activity within the RO), or upper/lower bounds on k. After applying such constraints, the set of equations (19)–(21) is repeatedly evaluated while incrementing k, and condition (13) together with the rest of input requirements are verified at each iteration.

The algorithm yields the achieved resolution Δ' (better than the required Δ), the architectural parameters k and n_x, and consequently the delays τ_x and τ_y.

4.3 Process Variation Scaling

Once a valid solution is obtained, e.g., using the frequency-constrained methodology, conditions (5) and (13) remain satisfied for any scaled operating frequency. This enables straightforward adaptation to fabrication process variations.

If the realized process is slower than expected, the TDC remains operational with proportionally relaxed performance. An example of such scaling is shown in Fig. 12.

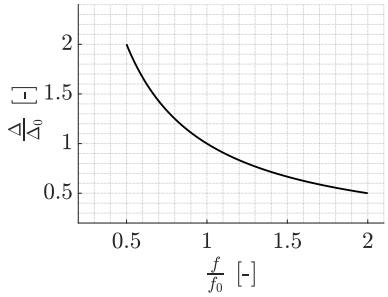
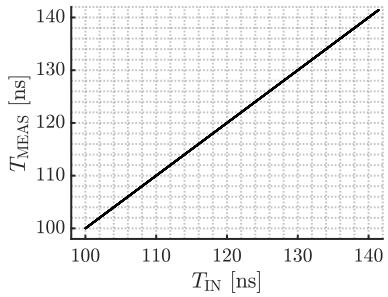
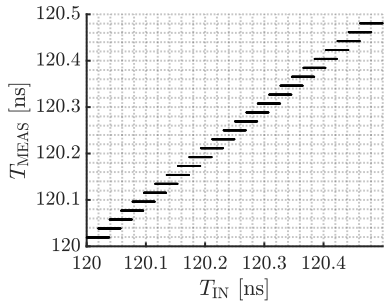


Fig. 12. Normalized resolution as a function of normalized frequency for $n_x = 13$ and $k = 8$, with $f_0 = 500\,\text{MHz}$ and $\Delta_0 = 19.23\,\text{ps}$.



(a)



(b)

Fig. 13. Simulation results for configuration obtained by Frequency-Constrained Approach described in Tab. 2: (a) Simulated conversion characteristic proving no dead-zone; (b) Detail of simulated conversion characteristic proving Δ'

5. Simulation Results

An example architecture was generated using the Frequency-Constrained design approach. The design inputs were a target resolution of at least 20 ps, a ring oscillator frequency of 500 MHz, and a maximum delay-cell speed τ_x limited to 150 ps. The resulting configuration is summarized in Tab. 2.

The architecture was implemented as a behavioral SystemVerilog model and evaluated in a testbench emulating realistic operating conditions. The TDC was stimulated by asynchronous strobing pulses with an incrementally increasing period (0.1 ps step) over a range of approximately 100–140 ns. The conversion characteristic was obtained by differencing consecutive timestamps.

Parameter	Value
k	8
n_x	13
Δ	19.2 ps
τ_x	153.8 ps
τ_y	134.6 ps
n of Q	62

Tab. 2. Proposed TDC Architecture Example

Figures 13(a) and 13(b) show the relationship between the injected delay T_{IN} and the corresponding delay T_{MEAS} produced by the behavioral model, with the latter providing a magnified view of the quantization-induced staircase characteristic.

The resulting characteristic is shown in Fig. 13(a). No dead zone is observed, confirming the correctness of the proposed design methodology. A detailed view in Fig. 13(b) reveals the expected staircase behavior caused by the finite timestamp precision of the Start and Stop events.

6. Conclusion

This paper has presented a novel RO-based TDC architecture that combines a continuously running PLL-stabilized multiphase RO with a 2D-VTDC. The proposed approach addresses the fundamental trade-off between oscillator stabilization and fine time interpolation by achieving sub-stage-delay resolution without interrupting oscillator operation.

The RO simultaneously provides coarse time quantization and DR_{tot} extension through a counter, while the 2D-VTDC resolves the oscillator phase with a precision finer than the intrinsic delay of a single RO stage. As a result, the required delay-stage speed can be reduced, potentially lowering power consumption while preserving high timing resolution.

Unlike many previously reported Vernier-based architectures, the proposed topology operates as a continuous timestamping engine rather than a dedicated interval-measurement circuit. Continuous PLL-based stabilization reduces oscillator-induced timing uncertainty and may reduce the need for extensive measurement averaging, which is particularly beneficial in low-power ToF systems such as ultrasonic flow meters.

A systematic design methodology for both resolution-constrained and frequency-constrained implementations has been derived. Behavioral simulations confirm dead-zone-free operation and validate the feasibility of the proposed concept. Future work will focus on transistor-level implementation, jitter analysis and experimental silicon verification.

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