Fast-Response Near-Threshold Self-Starting Low-Voltage Interleaved Boost DC-DC Converter for IoT Systems

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Abstract. *This article presents a self-starting switched-capacitor (SC) boost converter for battery-less Internet-of-Things (IoT) sensor nodes operating from ultra-low input voltages. An interleaved regulation architecture combined with a pre-charge node technique is employed to reduce output-voltage ripple and improve transient performance. To enable reliable operation under limited supply conditions, dynamic body biasing is utilized to lower the effective threshold voltage of the switching devices. Furthermore, a bootstrap-assisted clock-driving scheme is introduced to strengthen clock drive during startup and shorten the settling time. The proposed converter is implemented in a 180-nm CMOS process and evaluated through post-layout simulations. The results demonstrate reliable self-startup at ultra-low input voltages and a peak voltage conversion efficiency of 97.14%. These characteristics make the proposed converter well suited for energy-harvesting and self-powered IoT sensing applications.*

Keywords

Bootstrap driver, dynamic body biasing, interleaving regulation, Multi-Phase Non-overlapping Clock (MPNOC) generator, DC-DC converter, Internet of Things (IoT).

1. Introduction

The Internet of Things (IoT) facilitates the interconnection and interaction of smart devices, with applications in agriculture, healthcare, industrial monitoring, machine learning, and smart homes. The compactness of IoT devices requires tiny and durable batteries for optimal performance. However, the use of batteries may not be feasible in certain cases. Energy harvesting is a compelling and viable solution to these challenges, as it transforms minimal amounts of renewable energy into electrical voltage to operate the power management unit (PMU) [1]. A major challenge in energy-harvesting systems is the extremely low output voltage generated by many energy sources, which may be lower than the threshold voltage of CMOS transistors. Therefore, power management units (PMUs) must operate efficiently at ultra-low input voltages while providing sufficient output voltage to activate subsequent circuitry. Achieving reliable self-startup under these conditions is difficult because of limited transistor drive capability in the sub-threshold region, as well as leakage currents and voltage fluctuations that degrade conversion efficiency.

To address these challenges, this paper proposes a self-starting switched-capacitor Two-Branch Cross-Coupled Charge Pump (TBCCCP) with an interleaved architecture for ultra-low-voltage energy-harvesting applications. The interleaved operation reduces output-voltage ripple and improves load regulation, while a Dynamic Body Biasing (DBB) technique suppresses leakage current and enhances charge-transfer efficiency. In addition, a pre-charge node technique accelerates startup and improves overall power conversion efficiency. The proposed converter is capable of self-starting in the sub-threshold region without requiring an auxiliary power source.

Despite significant advances in low-voltage power conversion, achieving self-startup capability, high efficiency, low output ripple, and reliable sub-threshold operation simultaneously remains challenging. Existing solutions often involve trade-offs among efficiency, startup voltage, circuit complexity, and silicon area. Therefore, a review of state-of-the-art startup and charge-pump architectures is presented to identify existing limitations and motivate the proposed converter.

2. Related Work

Various methods have been developed to initiate start-up, including the use of additional storage devices, RF technology, and switch-based mechanisms. The work described in [2] uses a transformer-based start-up circuit, which requires a significantly high conversion ratio. In addition, these circuits suffer from higher resistance in the secondary coil and require external off-chip elements that limit their usage in real-time applications [3], [4].

Low-voltage DC-DC converters, such as capacitive and inductive DC-DC converters [5], are commonly used for charge transfer. The inductive converters employ various

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low-voltage start-up methods to initiate the entire circuit, reducing the required operational voltage and ensuring good conversion efficiency. Despite this, the downside of this method is the substantial increase in the on-chip area required to implement inductors.

To address this limitation, capacitive converters, also known as charge pumps (CPs), are employed due to their optimum integration capabilities. The first monolithic capacitive DC-DC converter was invented by Dickson in 1976 [6]. The design uses a series of diode-connected MOS transistors operating either in cut-off or saturation regimes. Reference [7] discusses the use of improved Charge Transfer Switches (CTSs) in applications that require minimal power supply. The CTS provides a higher pumping voltage gain in contrast to the Dickson CP. The linear charge pump (LCP) described in [8] is an enhanced version of [7] but is unsuitable for low-voltage operation.

A two-branch cross-coupled charge pump (TBCCCP) that includes two CTS arms with a compensation capacitor at every phase is described in [9]. This design enhances efficiency and minimizes output ripples by improving charge distribution across the two branches, yet it remains unsuitable for low-voltage applications. A method of integrating energy from various sources using a switch matrix is presented in [10]. This approach employs a dual-path design for energy harvesting, improving efficiency through an inductor. In [11], a six-stage TBCCCP with a reversible control technique is designed. This system utilizes two branches to regulate the gate of the CTS by applying increased internal voltage of the subsequent stages, thereby controlling transistor switching.

Threshold-Based Current Steering Logic (TBCP) with a three-stage configuration is introduced in [12], whereas the body of PMOS and NMOS is connected to the input of the preceding stage and output of the succeeding stage, respectively. This circuit configuration requires a four-stage CP architecture with small capacitors to improve performance by producing the body bias voltage needed for the NMOS transistors of the final stage. Reference [13] presents a charge pump that includes a progressive dead-time circuit, maximizing efficiency in comparison to a regular dead-time architecture. Moreover, dynamic body bias (DBB) with improved switch conductivity is utilized to enhance the output current.

Ref.	Architecture	Main advantage	Limitation
[2–4]	Transformer-based startup circuits	High voltage conversion gain and startup capability	Requires off-chip components and suffers from transformer losses
[5]	Inductive DC–DC converter	High conversion efficiency and low-voltage startup operation	Large silicon area due to integrated inductors
[6]	Dickson charge pump	Simple architecture and easy implementation	Threshold-voltage losses reduce efficiency at low supply voltages
[7]	CTS charge pump	Improved charge-transfer efficiency and pumping gain	Limited ultra-low-voltage operation
[8]	Linear charge pump (LCP)	Higher pumping capability compared with conventional CTS architectures	Unsuitable for sub-threshold operation
[9]	TBCCCP with compensation capacitors	Reduced output ripple and improved charge sharing	Limited low-voltage capability
[11]	Reversible-control TBCCCP	Improved switching efficiency and charge-transfer capability	Increased circuit complexity
[12]	Threshold-Based Current Steering Charge Pump (TBCP)	Enhanced transistor conduction and charge transfer	Additional stages and control circuitry required
[13]	Dynamic Body Biasing (DBB) charge pump	Improved output current and power conversion efficiency	Higher control complexity
[14–16]	Interleaved switched-capacitor converters	Reduced output-voltage ripple and improved transient response	Higher supply-voltage requirement
[17]	Adiabatic charge pump	Reduced power dissipation through energy recovery	Longer settling time and increased implementation complexity
[18]	Latched charge pump	High pumping efficiency and compact implementation for energy-harvesting systems	Startup voltage limited to approximately 400 mV and relatively longer startup duration
[19]	Low-voltage latched charge pump	Good conversion efficiency with small capacitor overhead	Limited operation below 400 mV and moderate startup performance
[20]	Scaled CMOS latched charge pump	High output power density and area efficiency enabled by advanced CMOS technology	Reduced voltage conversion efficiency compared with state-of-the-art designs
This Work	Interleaved TBCCCP with DBB and pre-charge node	Self-startup capability, low output ripple, fast settling time, reliable sub-threshold operation, and 97.14% peak power conversion efficiency	–

Tab. 1. Comparison of state-of-the-art startup and charge pump architectures.

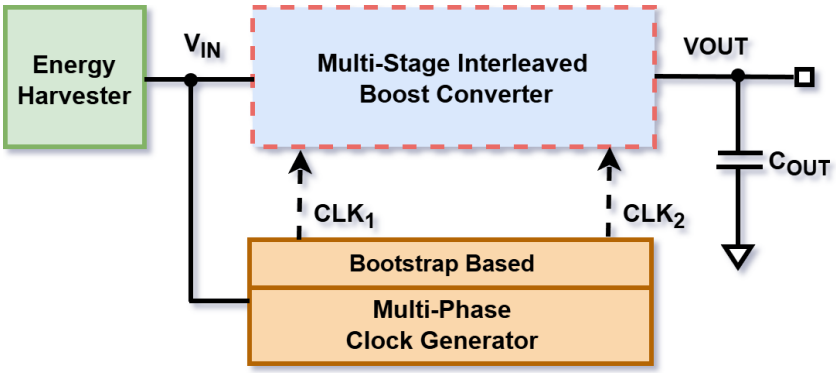


Fig. 1. Proposed architecture of the boost converter.

Switched-capacitor (SC) circuits with interleaving regulation are employed in [14–16] to reduce output-voltage ripple and improve settling time; however, their operation is typically limited to relatively higher supply voltages. In [17], an adiabatic charge-pump architecture utilizes a ramp-generator circuit to reduce power dissipation and improve energy efficiency, although a longer settling time is required to reach the target output voltage. More recently, the low-voltage latched charge pump reported in [18] achieves a peak pumping efficiency of 99%; however, it requires a 400-mV input voltage and exhibits a startup time of 33 µs. Similarly, the design in [19] demonstrates good conversion efficiency using a latched charge-pump topology, but still requires a 400-mV input voltage and a startup time of 30 µs. In [20], a 65-nm CMOS implementation improves power density and area efficiency through technology scaling; however, its voltage conversion efficiency is limited to 87.8%. As summarized in Tab. 1, existing charge-pump architectures employ various techniques to improve startup capability, charge-transfer efficiency, and output regulation. Nevertheless, none of these approaches simultaneously combines interleaved operation, dynamic body biasing, and pre-charge-assisted startup to enable reliable operation under ultra-low input-voltage conditions. To address these limitations, this work proposes a self-starting interleaved Two-Branch Cross-Coupled Charge Pump (TBCCCP) architecture incorporating dynamic body biasing, a pre-charge node technique, and a bootstrap-assisted clock generator to achieve enhanced startup capability, reduced ripple, and improved charge-transfer efficiency for energy-harvesting applications.

This work presents a self-starting switched-capacitor TBCCCP circuit with an interleaved structure. Interleaving regulation effectively reduces output voltage ripples while enhancing transient response and load regulation by distributing current flow sequentially. The proposed design operates in the sub-threshold region without an additional power supply. To address CMOS leakage challenges at low voltages, the DBB technique is chosen, allowing adaptive tuning of body bias voltage in both active and inactive cases through auxiliary transistors. In addition, a pre-charge node technique is introduced to further improve the settling time and overall power conversion efficiency.

Efficient operation of the proposed converter critically depends on a suitable clock generation scheme capable of producing non-overlapping multi-phase clock signals under sub-threshold voltage conditions. To meet this requirement, a multi-phase clock generator (MPCG) with bulk biasing is adopted, which is specifically designed to operate reliably at ultra-low supply voltages. Furthermore, to accelerate the settling behavior of the charge pump, a bootstrap driver combined with dynamic body biasing is employed at the output of the ring oscillator to drive the phase generator. This approach significantly enhances the clock driving strength while achieving an extended rail-to-rail output voltage swing, thereby improving the overall performance of the interleaved TBCCCP.

The remainder of this paper is organized as follows. Section 3 describes the structure of the proposed boost converter and its operation. Section 4 presents post-layout simulation results of the implemented prototype. Finally, Section 5 concludes the paper.

3. The Structure of the Proposed Boost Converter and its Operation

The proposed DC–DC boost converter employing an interleaving technique is illustrated in Fig. 1. To effectively suppress output voltage and current ripples in switched-capacitor (SC) power converters, multi-phase interleaving is widely adopted. This technique not only reduces ripple components but also significantly improves transient response and load regulation. To establish the foundation for the proposed architecture, the operation of the basic cross-coupled voltage doubler (CCVD) and the formation of its output voltage are first reviewed.

A cross-coupled voltage doubler (CCVD), shown in Fig. 2, employs complementary, non-overlapping clock phases (CLK and CLKB) to alternately charge and discharge two pumping capacitors. During phase 2, capacitor C_{S2} is charged to V_{IN}, while C_{S1} transfers its stored charge to the output, generating internal node voltages close to $2V_{IN}$ and V_{IN}. In phase 1, the roles of C_{S1} and C_{S2} are interchanged, again producing an output voltage near $2V_{IN}$.

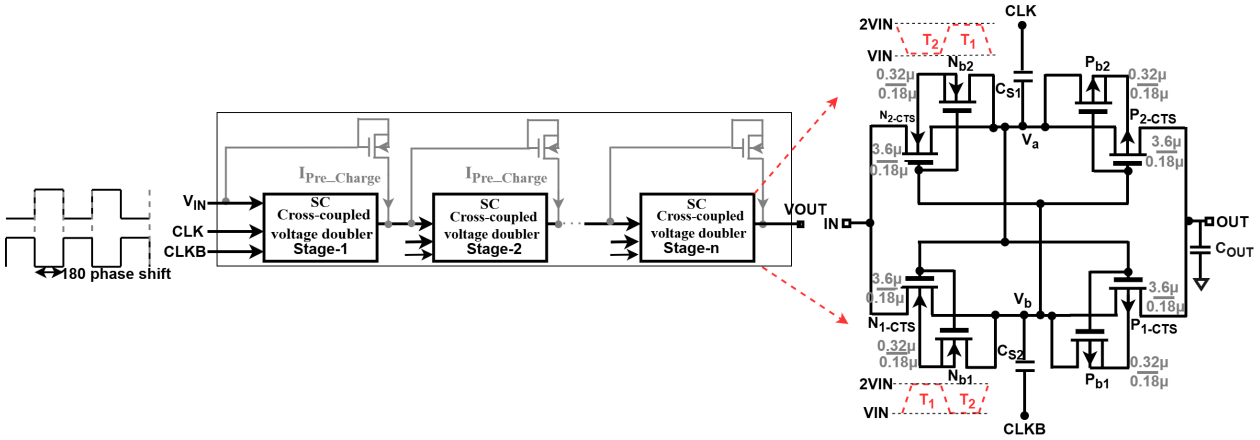


Fig. 2. N-stage Two-Phase charge pump.

To enhance charge-transfer efficiency, a pre-charge node is introduced at the input of each CCVD stage to initialize the pumping capacitors to a defined intermediate voltage prior to charge transfer. This reduces the voltage swing across the transfer switches, thereby mitigating threshold-voltage loss, suppressing charge sharing between adjacent stages, and improving output settling. Although charge redistribution inherently causes output ripple, the proposed pre-charge scheme stabilizes internal node voltages and effectively reduces ripple while improving overall pumping efficiency.

Assuming ideal components, the charge delivered to the load during one switching cycle is

$$Q_{\text{load}} = i_{\text{L}} \frac{T}{2}, \tag{1}$$

and the corresponding output-voltage ripple is

$$\Delta V_{\text{o}} = \frac{i_{\text{L}} T}{2(C_{\text{S2}} + C_{\text{out}})}. \tag{2}$$

Charge conservation between C_{S2} and C_{out} at phase boundaries gives the output voltages

$$V_{\text{out1}} = 2V_{\text{IN}} - \frac{C_{\text{out}} i_{\text{L}}}{2fC(C + C_{\text{out}})}, \tag{3}$$

$$V_{\text{out2}} = 2V_{\text{IN}} - \frac{i_{\text{L}}}{2fC}, \tag{4}$$

for a symmetric structure with $C_{\text{S1}} = C_{\text{S2}} = C$.

Figure 3 depicts the proposed four-cell interleaved transmission-based complementary clocked charge pump. The architecture comprises four identical TBCCVD cells connected in parallel at the output node, with each cell implemented using multiple cascaded charge-pump stages. Each stage employs complementary NMOS–PMOS transmission paths and flying capacitors, which enable efficient charge transfer while reducing threshold-voltage degradation and mitigating reverse charge sharing.

Interleaved operation is realized using eight non-overlapping clock phases uniformly distributed over one clock period, corresponding to a phase spacing of $360°/8 = 45°$. Each TBCCVD cell is driven by a dedicated pair of complementary clock phases, resulting in time-shifted operation of the four cells while sharing a common output capacitor C_{out}. Consequently, charge transfer events are distributed over the switching cycle, leading to time-interleaved energy delivery and improved output continuity.

By distributing switching activity across n uniformly phase-shifted clocks with $360°/n$ separation, the proposed architecture reduces both input and output current ripple, suppresses switching-induced noise, and improves transient behavior. In addition, the multi-cell structure inherently enhances robustness, as output regulation can be maintained by the remaining $n-1$ cells in the event of a single-cell malfunction. Interleaving is achieved through complementary gate-drive signals that coordinate the charging and discharging phases of each cell. As a result, while one cell is electrically isolated from the output during its charging interval, another cell concurrently operates in the discharge phase and sustains V_{out}, thereby eliminating idle intervals typical of two-phase converters and ensuring continuous energy transfer throughout the clock period.

To further increase the granularity of charge transfer, the proposed design extends the four-phase interleaving concept to an eight-phase TBCCVD structure. In the eight-phase configuration, the switching period T is divided into eight equal intervals separated by 45°. The k-th phase is expressed as

$$\phi_k(t) = \phi_1\left(t - \frac{(k-1)T}{8}\right), \qquad k = 1, \ldots, 8. \tag{5}$$

With this sequencing, each cell completes one charging (ϕ_1) and one discharging (ϕ_2) operation for every $T/8$ period. At any instant, two cells are discharging while another two are charging, creating highly overlapped charge-transfer intervals. The instantaneous output charge is

$$Q_{\text{out}}(t) = Q_{\phi_2,k}(t) + Q_{\phi_2,k+4}(t) \tag{6}$$

where the active discharge cells are offset by four phases.

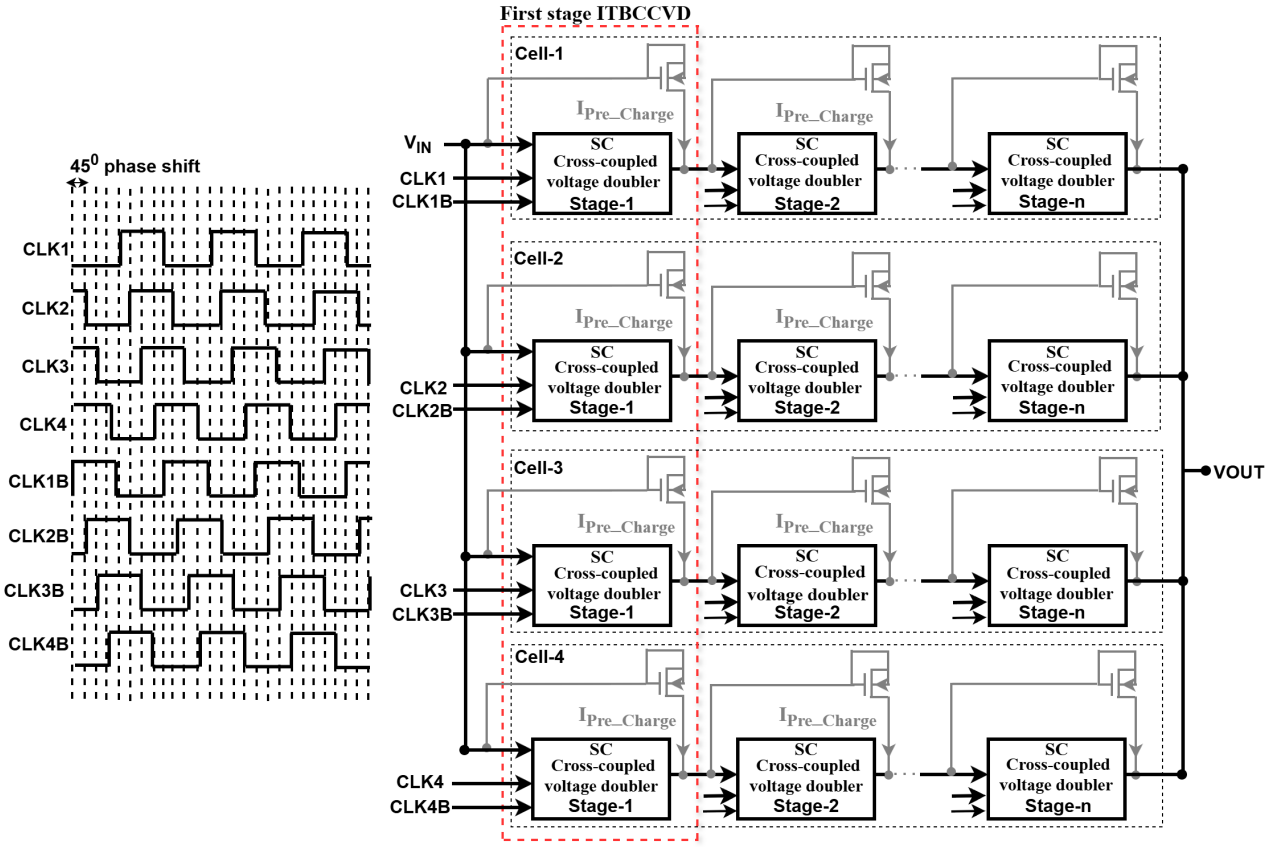


Fig. 3. N-stage Eight-Phase charge pump.

Each pumping capacitor transfers

$$\Delta Q = C_{\mathrm{P}} \left(V_{\mathrm{CP}} - V_{\mathrm{out}}\right), \tag{7}$$

yielding an average output current

$$I_{\mathrm{out}} = \frac{2\Delta Q}{T/8} = 16 C_{\mathrm{P}} \frac{V_{\mathrm{CP}} - V_{\mathrm{out}}}{T}. \tag{8}$$

Ripple reduction in an N-phase interleaved converter follows

$$\Delta V_{\mathrm{out}} \propto \frac{1}{N}, \tag{9}$$

so increasing the number of phases from $N = 2$ to $N = 8$ significantly reduces the ripple amplitude and capacitor stress. The generalized conversion gain for an N-phase TBCCVD topology is

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \simeq 2 - \frac{T}{2R_L(2C_{\mathrm{P}} - C_{\mathrm{out}})} \cdot \frac{1}{N}, \tag{10}$$

and for the eight-phase implementation becomes

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \simeq 2 - \frac{T}{16R_L(2C_{\mathrm{P}} - C_{\mathrm{out}})}. \tag{11}$$

Thus, the finer granularity of the eight-phase TBCCVD improves transient response, reduces inrush current, and brings the achieved conversion ratio closer to the ideal 2× gain.

3.1 Stability Analysis

The proposed eight-phase TBCCVD can be modeled as an equivalent switched-capacitor converter whose charge-transfer process is represented by an effective output resistance R_{eq}. Based on the charge transferred by each pumping capacitor during a switching cycle,

$$R_{\mathrm{eq}} \approx \frac{1}{16 f_{\mathrm{s}} C_{\mathrm{P}}} \tag{12}$$

where $f_{\mathrm{s}} = 1/T$ is the switching frequency and C_{P} is the pumping capacitance. The output-node dynamics are governed by

$$C_{\mathrm{out}} \frac{dV_{\mathrm{out}}}{dt} = \frac{V_{\mathrm{THCCP}} - V_{\mathrm{out}}}{R_{\mathrm{eq}}} - \frac{V_{\mathrm{out}}}{R_{\mathrm{L}}} \tag{13}$$

where V_{THCCP} denotes the Thevenin equivalent voltage of the charge-pump network. Linearizing around the steady-state operating point yields

$$C_{\mathrm{out}} \frac{dV_{\mathrm{out}}}{dt} + \left(\frac{1}{R_{\mathrm{eq}}} + \frac{1}{R_{\mathrm{L}}}\right) V_{\mathrm{out}} = 0, \tag{14}$$

which produces the dominant pole

$$p_1 = -\frac{1}{C_{\mathrm{out}}} \left(\frac{1}{R_{\mathrm{eq}}} + \frac{1}{R_{\mathrm{L}}}\right). \tag{15}$$

Substituting (12),

$$p_1 = -\frac{1}{C_{\mathrm{out}}} \left(16 f_{\mathrm{s}} C_{\mathrm{P}} + \frac{1}{R_{\mathrm{L}}}\right). \tag{16}$$

Equation (16) indicates that increasing the number of interleaved phases effectively reduces R_{eq}, thereby shifting the dominant pole toward higher frequencies and improving dynamic stability. Compared with a conventional two-phase architecture, the eight-phase implementation exhibits approximately four times lower equivalent output resistance, resulting in faster settling and reduced output-voltage overshoot during startup.

3.2 Output Noise and Ripple Sensitivity

The output ripple is generated by discrete charge-transfer events. For an N-phase interleaved converter,

$$\Delta V_{out} \approx \frac{I_{load}}{N f_s C_{out}}, \tag{17}$$

demonstrating an inverse dependence on the number of phases.

For the proposed architecture ($N = 8$),

$$\Delta V_{out,8} = \frac{I_{load}}{8 f_s C_{out}}, \tag{18}$$

whereas for a conventional two-phase implementation,

$$\Delta V_{out,2} = \frac{I_{load}}{2 f_s C_{out}}, \tag{19}$$

Therefore,

$$\frac{\Delta V_{out,8}}{\Delta V_{out,2}} = \frac{1}{4}, \tag{20}$$

indicating a theoretical 75% reduction in ripple amplitude.

The spectral density of switching noise is similarly reduced because the dominant ripple frequency shifts from $2f_s$ to $8f_s$, moving switching harmonics further away from the signal band and easing output filtering requirements.

3.2.1 Thermal Noise Analysis

The thermal noise associated with the MOS switches is characterized by the well-known kT/C relation

$$\overline{v_n^2} = \frac{kT}{C_P}, \tag{21}$$

where k is Boltzmann's constant and T is the absolute temperature.

The corresponding rms noise voltage is

$$v_{n,rms} = \sqrt{\frac{kT}{C_P}}. \tag{22}$$

Because the charge-transfer events are distributed among multiple phases, the total output noise becomes

$$v_{n,out} \approx \frac{1}{\sqrt{N}} \sqrt{\frac{kT}{C_P}}, \tag{23}$$

which predicts for the proposed eight-phase architecture

$$v_{n,out,8} = 0.5\, v_{n,out,2}, \tag{24}$$

indicating approximately a 50% reduction in thermal-noise fluctuations compared with a conventional two-phase implementation. The reduction arises from the averaging effect of the interleaved charge-transfer process, which distributes noise contributions across multiple phases and suppresses low-frequency output noise components.

3.3 Parasitic Capacitance Effects

Parasitic capacitances associated with MOS switches, routing interconnects, overlap capacitances, and junction capacitances reduce the effective transferred charge and degrade the achievable voltage conversion gain. The effective pumping capacitance can be expressed as

$$C_{eff} = C_P - C_{par} \tag{25}$$

where C_{par} denotes the total parasitic capacitance.

The actual conversion gain can therefore be approximated as

$$G_{eff} = \frac{V_{out}}{V_{in}} = 2\left(\frac{C_P}{C_P + C_{par}}\right), \tag{26}$$

which shows that parasitic capacitances reduce the attainable voltage gain from its ideal value.

The sensitivity of the conversion gain to parasitic capacitance is given by

$$S_{C_{par}} = \frac{\partial G_{eff}}{\partial C_{par}} = -\frac{2C_P}{(C_P + C_{par})^2}, \tag{27}$$

indicating that gain degradation becomes increasingly significant as C_{par} approaches C_P.

In addition to gain reduction, parasitic capacitances introduce dynamic power losses due to repeated charging and discharging during switching operation. The corresponding parasitic power loss is

$$P_{par} = N C_{par} V_{DD}^2 f_s \tag{28}$$

where N is the number of interleaved phases and f_s is the switching frequency.

Consequently, increasing the number of phases improves ripple performance but also increases parasitic switching losses, creating an important trade-off between efficiency and output-voltage quality.

Furthermore, the equivalent output resistance including parasitic effects can be approximated as

$$R_{eq,par} = \frac{1}{N f_s (C_P - C_{par})}, \tag{29}$$

demonstrating that larger parasitic capacitances increase the effective output resistance and degrade load regulation.

3.3.1 Robustness to Process Variability

At ultra-low input voltages, threshold-voltage variation represents one of the dominant sources of performance degradation. Since the charge-pump switches operate close to the

subthreshold region during startup, their current can be approximated as

$$I_{\mathrm{D}} = I_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{nV_{\mathrm{T}}}\right) \tag{30}$$

where I_0 is a process-dependent current, n is the subthreshold slope factor, and $V_{\mathrm{T}} = kT/q$ is the thermal voltage.

The sensitivity of the drain current to threshold-voltage variation is

$$S_{V_{\mathrm{TH}}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{TH}}} = -\frac{I_{\mathrm{D}}}{nV_{\mathrm{T}}}, \tag{31}$$

which indicates an exponential dependence of charge-transfer capability on device threshold voltage.

For a threshold-voltage mismatch ΔV_{TH}, the relative current variation becomes

$$\frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}} \approx -\frac{\Delta V_{\mathrm{TH}}}{nV_{\mathrm{T}}}. \tag{32}$$

Similarly, process-induced capacitance variation affects the transferred charge according to

$$\frac{\Delta Q}{Q} = \frac{\Delta C_{\mathrm{P}}}{C_{\mathrm{P}}}, \tag{33}$$

which directly impacts the output current and startup behavior.

The resulting output-voltage variation can be approximated as

$$\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{out}}} \approx \frac{\Delta C_{\mathrm{P}}}{C_{\mathrm{P}}} + \frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}}, \tag{34}$$

demonstrating the combined influence of capacitance mismatch and transistor variability.

Because the proposed architecture employs eight interleaved branches, mismatch effects are statistically averaged. The output-voltage standard deviation therefore follows

$$\sigma_{V_{\mathrm{out}}} \propto \frac{1}{\sqrt{N}} \tag{35}$$

where N is the number of interleaved phases.

For the proposed eight-phase implementation,

$$\sigma_{V_{\mathrm{out},8}} = \sqrt{\frac{2}{8}}\,\sigma_{V_{\mathrm{out},2}} = 0.5\,\sigma_{V_{\mathrm{out},2}}, \tag{36}$$

indicating approximately a 50% reduction in mismatch-induced output variation compared with a conventional two-phase architecture.

Therefore, the proposed eight-phase TBCCVD not only improves charge-transfer granularity and ripple performance but also enhances robustness against process-induced threshold-voltage, capacitance, and device-mismatch variations, making it suitable for reliable ultra-low-voltage energy-harvesting applications.

Sizing of the charge transfer switch is discussed in the next section.

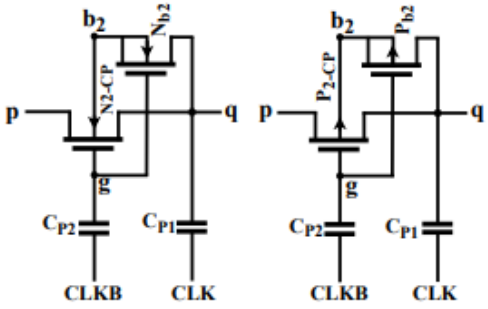


Fig. 4. CTS transistor body-biasing schematic.

3.4 Sizing of CTS

The bodies of the CTS transistors ($N_{2\text{-CP}}$ and N_{b2}) in Fig. 4 are biased through a single auxiliary device. When CLK = high and CLKB = low, $N_{2\text{-CP}}$ turns on and node g is boosted. During the same interval, N_{b2} also turns on, shorting nodes p, q, and b_2, giving

$$V_{b2} = V_q \le V_p. \tag{37}$$

When CLK = low and CLKB = high, both $N_{2\text{-CP}}$ and N_{b2} turn off. The resulting body voltage V_{b2} is determined by the device capacitances:

$$V_{b2} = \frac{V_g\left(C_{gb,N2} + C_{gb,Nb2}\right)}{C_{\mathrm{T}}} + \frac{V_q\left(C_{sb,N2} + C_{db,Nb2}\right)}{C_{\mathrm{T}}} + \frac{V_p C_{db,N2}}{C_{\mathrm{T}}} \tag{38}$$

where

$$C_{\mathrm{T}} = C_s + C_{gb,N2} + C_{db,N2} + C_{sb,N2} + C_{db,Nb2} + C_{gb,Nb2}. \tag{39}$$

Given $V_q < V_p \le V_g$ when $N_{2\text{-CP}}$ is on, and noting that $C_{sb,N2} + C_{db,Nb2} \ll C_{\mathrm{T}}$, the expression simplifies to:

$$V_{b2} \approx \frac{C_{gb,N2} + C_{gb,Nb2} + C_{db,N2}}{C_{\mathrm{T}}} V_p. \tag{40}$$

Defining a compact parameter

$$\alpha = \frac{C_{sb,N2} + C_{db,Nb2} + C_s}{C_{gb,N2} + C_{gb,Nb2} + C_{db,N2}}, \tag{41}$$

we obtain a single-column-friendly form:

$$V_{b2} = \frac{1}{1+\alpha} V_p. \tag{42}$$

Since $C_{gb,N2} \gg C_{db,Nb2}, C_s, C_{sb,N2}$, a moderate device size for N_{b2} (10% of $N_{2\text{-CP}}$) yields $\alpha \ll 1$. When CLK = low and CLKB = high, the node relation becomes:

$$V_{b2} = V_q > V_p. \tag{43}$$

3.5 Multi-Phase Clock Generator

Figure 5 illustrates the proposed multi-phase clock generator, which produces non-overlapping clock waveforms. It consists of a bootstrap driver, a eight-phase ring oscillator

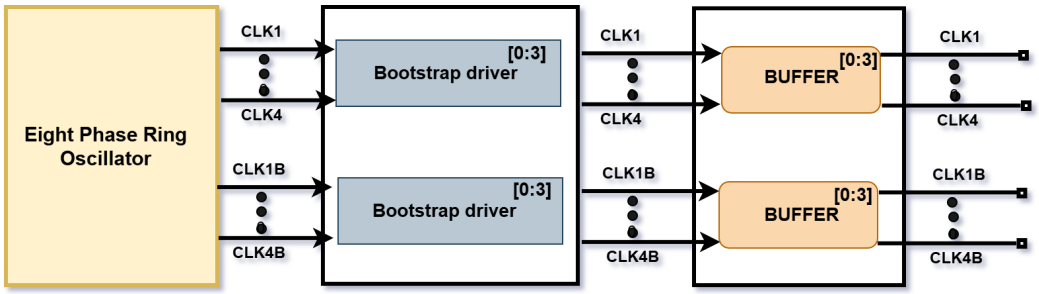


Fig. 5. Bootstrap-based multi-phase oscillator.

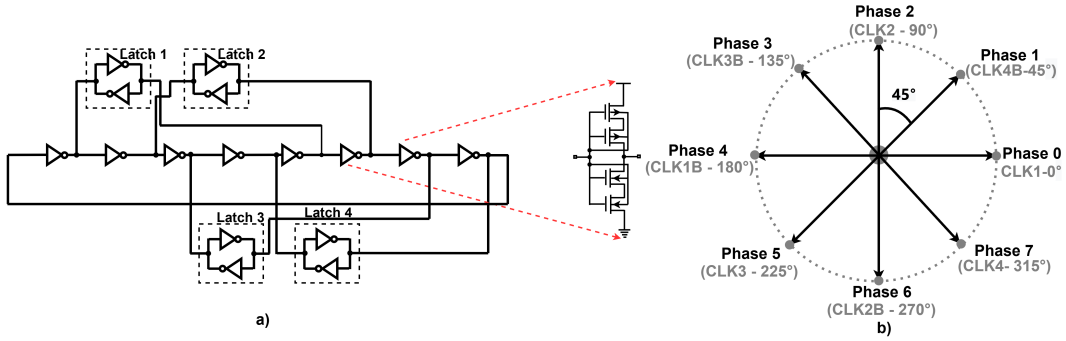


Fig. 6. a) 8-phase ring oscillator; b) 8-Phase Phasor Diagram (45° Spacing).

(RO), and a phase generator. Conventional low-power clock-generation circuits [21] often suffer from limited duty-cycle accuracy and restricted operating range, whereas the proposed architecture alleviates these limitations and improves overall low-power performance.

Designing an oscillator capable of generating non-overlapping clock phases with sufficient current drive is challenging in low-voltage systems. In LV energy-harvesting applications, the supply voltage is often comparable to or lower than the MOSFET threshold. For example, in a 0.18 µm CMOS process, harvested voltages around 0.5 V force the RO to operate in the weak-inversion or subthreshold region, severely limiting drive current and degrading oscillation amplitude, delay uniformity, and startup reliability.

Body-biasing enables reliable MOSFET operation under such constrained voltages by tuning the threshold, suppressing leakage, and improving conduction. The NMOS threshold with body effect is:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s} \right) \tag{44}$$

where V_{TH0} is the zero-bias threshold, γ the body-effect coefficient, ϕ_s the surface potential, and V_{SB} the source-to-body voltage. Forward body bias (FBB) reduces V_{TH}, improving on-current; reverse body bias increases V_{TH}, reducing leakage.

Advanced RO architectures [18, 22–24] employ auxiliary devices to generate strong, well-regulated bulk voltages, enabling higher subthreshold current and robust low-voltage CP operation. Figure 6 illustrates an eight-stage stacked inverter chain incorporating latch-based gating. The corresponding phase diagram demonstrates the generation of

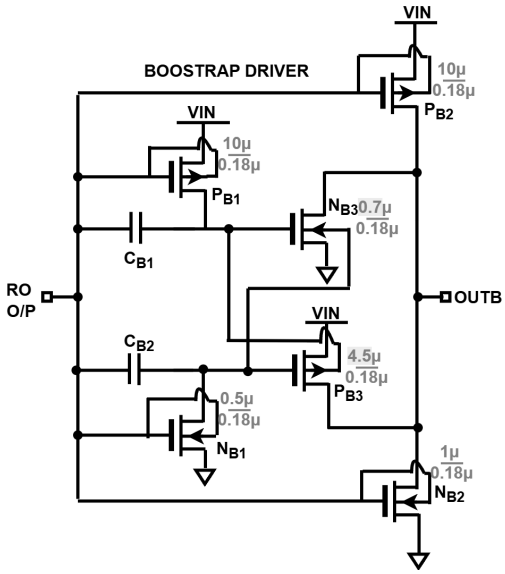


Fig. 7. Boostrap driver.

eight-phase clock signals, uniformly spaced at 45° intervals. Minimum-sized inverters reduce effective V_{th} and power consumption, with transistor stacking mitigating leakage.

A bootstrap driver as shown in Fig. 7 is inserted between the RO and the phase generator to enhance load drive and ensure rail-to-rail clock swing. It uses bootstrap capacitors (C_{B1}, C_{B2}) and NMOS/PMOS devices (N_{B1}–N_{B3}, P_{B1}–P_{B3}) with dynamic body biasing (DBB) to overcome low gate-overdrive limitations. The driver improves switching speed, especially when input voltages are below the threshold. Up-sized output buffers suppress glitches and ensure clean, rail-to-rail transitions.

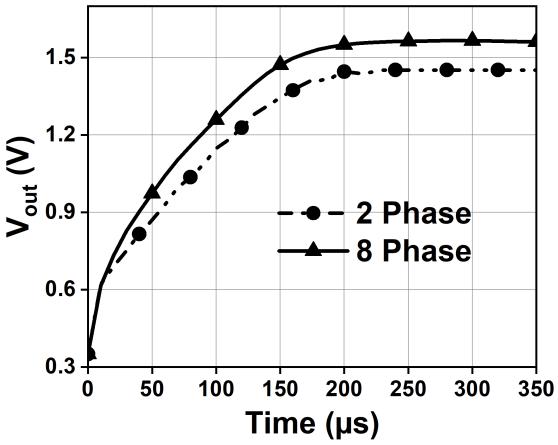


Fig. 8. Transient response of the output voltage with two-phase and eight-phase at 320 mV.

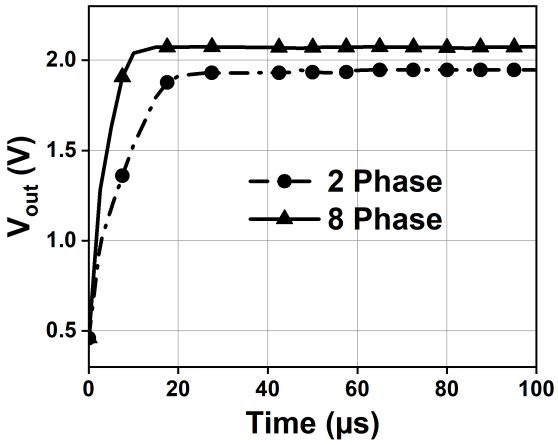


Fig. 9. Transient response of the output voltage with two-phase and eight-phase at 420 mV.

4. Results and Discussions

The proposed charge pump (CP) circuits were implemented in a 0.18 µm CMOS process and verified using Cadence Spectre simulations. All designs employ 1 pF pumping capacitors (C_1–C_8) and a 1 pF load capacitor (C_{out}), operating at a nominal switching frequency of 7.8 MHz. Both the two-phase and eight-phase CP architectures utilize dynamic body biasing (DBB) to enhance subthreshold conduction and improve charge transfer efficiency under low-voltage operation.

The pumping efficiency, which serves as a key performance metric for evaluating the effectiveness of charge transfer, is defined as the ratio of the measured output voltage to the ideal output voltage:

$$\eta_{\text{pump}} = \frac{V_{\text{out}}}{V_{\text{ideal}}} \times 100\% \tag{45}$$

where V_{out} denotes the measured output voltage across the load capacitor and V_{ideal} represents the theoretical output voltage assuming perfect charge transfer without losses.

In these CP architectures, DBB plays a pivotal role by dynamically adjusting the transistor threshold voltage during switching events. This mechanism improves conduction when the transistors operate in the subthreshold region, thereby increasing the effective charge delivered per clock cycle. Furthermore, the deployment of multiple pumping phases (such as in four-stage CP) contributes to reduced voltage ripple, improved load regulation, and reduced startup time to achieve the target output voltage. Figures 8 and 9 compare the transient responses of clock-driven 2-phase (180°) and 8-phase (45°) charge pumps (CP) at supply voltages of 0.32 V and 0.42 V.

The results clearly show that the proposed 8-phase CP exhibits substantially faster ramp-up behavior. Specifically, the multi-phase operation improves the effective charge transfer per cycle and minimizes the instantaneous voltage droop between successive pumping events.

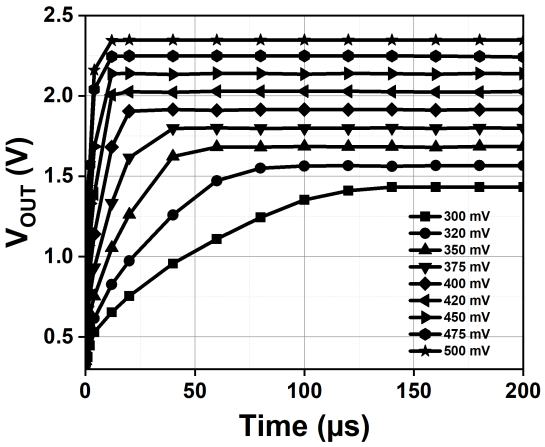


Fig. 10. Transient response of the output voltage for various supply voltages (300 mV, 320 mV, 350 mV, 375 mV, 400 mV, 420 mV, 450 mV, 470 mV, and 500 mV).

As a result, the 8-phase architecture achieves a 62% reduction in startup time at 0.32 V and a 72% reduction at 0.42 V compared to the conventional 2-phase design.This improvement is primarily attributed to the increased pumping frequency and reduced ripple-induced delay. Figure 10 illustrates the transient response of the eight-phase converter's output voltage with a bootstrap driver under various supply voltages (300 mV, 320 mV, 350 mV, 375 mV, 400 mV, 420 mV, 450 mV, 470 mV, and 500 mV) at no-load conditions. As observed, the start-up speed improves with increasing supply voltage, with the start-up time decreasing from 153 µs at 0.3 V to approximately 3.84 µs at 0.5 V. Concurrently, the steady-state output voltage rises from 1.44 V to 2.41 V as the supply voltage increases.

Figure 11 illustrates the relationship between the output voltage and ramp-up time as a function of the input voltage for both two-phase and eight-phase charge pump (CP) circuits, with identical switching frequency and load capacitance. The eight-phase CP exhibits a 50% faster start-up compared to the two-phase architecture at a supply voltage

of 0.3 V, whereas the difference becomes negligible at higher supply voltages. Furthermore, the eight-phase CP achieves a higher output voltage than the two-phase CP over the input voltage range from 0.3 V to 0.7 V. This behavior underscores the advantage of distributing the pumping operation across multiple interleaved phases, which reduces charge loss, enhances conduction time, and lowers ripple amplitude.

Figure 12 presents the trend of measured efficiency of both architectures. The proposed 8-phase CP achieves maximum efficiencies of 96.87% at 300 mV and 93.42% at 700 mV, outperforming the 2-phase solution throughout the range. Efficiency remains tightly regulated within a 6–8% variation, due to reduced switching losses and improved dynamic charge sharing. The multi-phase structure also minimizes reverse charge flow by ensuring more uniform capacitor charging and discharging intervals, which becomes particularly beneficial at near-threshold and sub-threshold input voltages. Figure 13 illustrates the efficiency variation as a function of pumping frequency for both the proposed 8-phase and conventional 2-phase charge-pump architectures. The efficiency initially increases with pumping frequency and reaches a maximum value before gradually decreasing at higher frequencies.

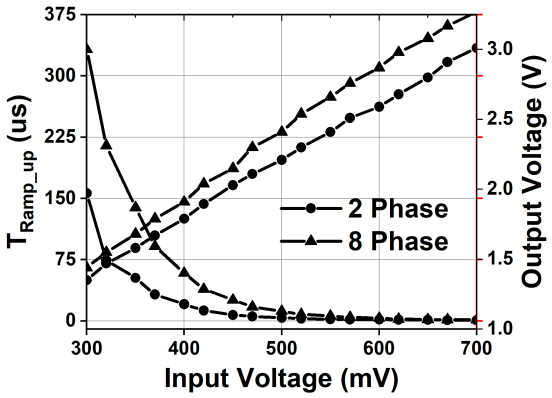


Fig. 11. The output voltage and ramp-up time as a function of the input voltage.

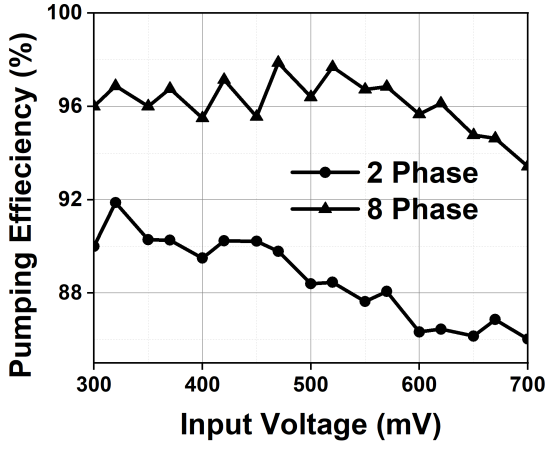


Fig. 12. Pumping efficiency with Two-Phase and Eight-Phase for different supply voltages.

The proposed 8-phase architecture consistently achieves higher efficiency than the 2-phase implementation over a wide frequency range. Peak efficiencies of approximately 25% and 38% are obtained at input voltages of 320 mV and 420 mV, respectively. Figure 14 shows the efficiency as a function of load current. The proposed 8-phase converter achieves peak efficiencies of approximately 31.5% and 37.4% for input voltages of 320 mV and 420 mV, respectively. Compared with the conventional 2-phase architecture, the proposed converter maintains superior efficiency across the entire load-current range. The efficiency decreases at higher load currents due to increased power dissipation in the charge-transfer path.

Figure 15 presents the efficiency as a function of output power. The efficiency increases with output power and reaches a maximum value of approximately 37.4% at an output power of about 75 nW for an input voltage of 420 mV. Beyond this point, the efficiency gradually decreases as power losses become more significant.

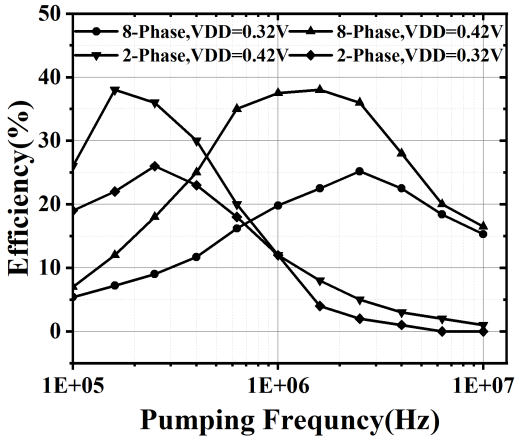


Fig. 13. The efficiency variation as a function of pumping frequency.

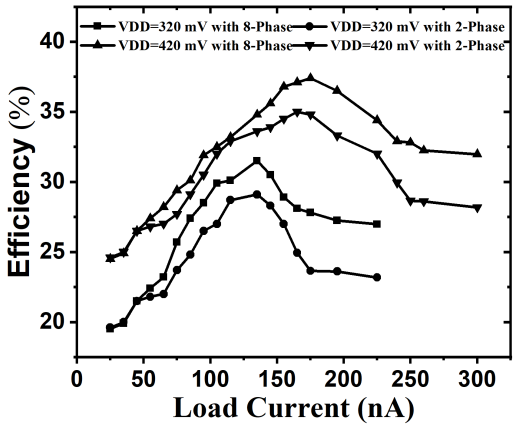


Fig. 14. The efficiency as a function of load current.

Circuit	V_{in} (mV)	V_{out} (V)	$T_{ramp\text{-}up}$ (µs)	V_{ripple} (mV)	Power (nW)	Efficiency (%)
2-Phase	320	1.47	138.8	15.5	80.1	91.87
	420	1.95	25.7	17.4	991.5	92.85
8-Phase	320	1.55	52.6	7.24	162.3	96.87
	420	2.04	7.1	7.34	2130	97.14

Tab. 2. Simulation results of the proposed charge pump structures.

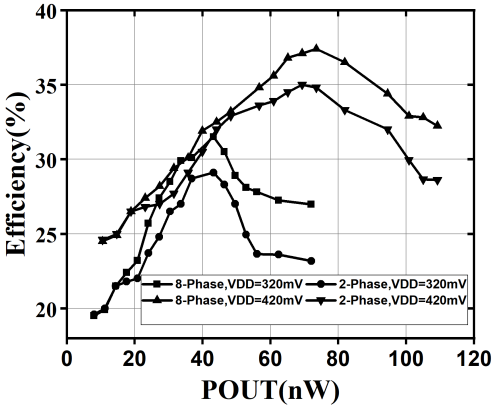


Fig. 15. The efficiency as a function of output power.

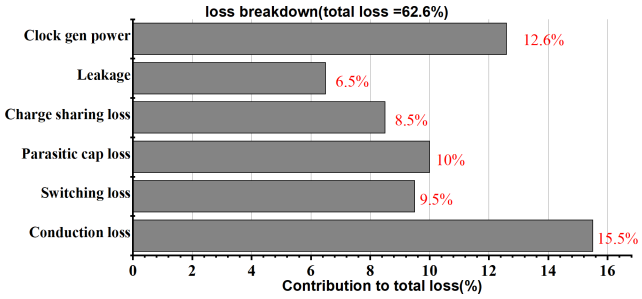


Fig. 16. The estimated loss breakdown.

To further analyze the converter performance, Figure 16 presents the estimated loss breakdown of the proposed 8-phase charge pump at the peak-efficiency operating point. The total power loss is approximately 62.6%, corresponding to a peak power-conversion efficiency of 37.4%. Conduction loss is the dominant loss mechanism, contributing approximately 15.5 percentage points to the overall efficiency degradation. This loss primarily arises from the finite on-resistance of the charge-transfer switches during energy transfer.

Clock-generation power represents the second largest contributor, accounting for approximately 12.6 percentage points of the total loss, followed by parasitic-capacitance loss and switching loss, which contribute approximately 10% and 9.5%, respectively. Charge-sharing loss accounts for approximately 8.5% of the total loss and is significantly reduced by the proposed 8-phase interleaving architecture, which improves charge-transfer continuity and minimizes voltage redistribution among the flying capacitors. Leakage loss contributes approximately 6.5% of the total loss and remains relatively small due to the ultra-low-voltage operating conditions.

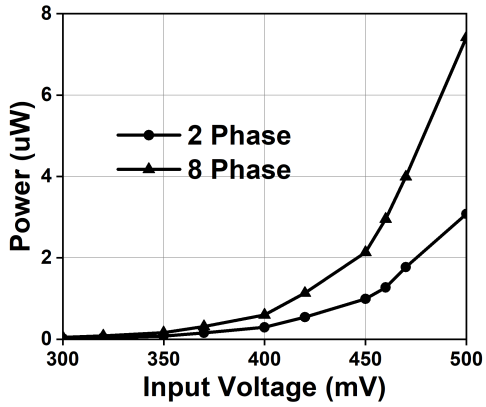


Fig. 17. The power consumption for two-phase and eight-phase CP circuits for various input voltage.

The loss analysis indicates that conduction, clock-generation, switching, and parasitic-capacitance losses are the primary factors limiting the overall efficiency of the converter. Nevertheless, the proposed multi-phase architecture effectively suppresses charge-sharing losses and improves charge-transfer efficiency compared with conventional two-phase implementations. These results provide valuable insight into the dominant loss mechanisms and identify potential directions for further efficiency enhancement in future designs.

Figure 17 displays the comparison of power consumption for two-phase and eight-phase CP circuits for various power supplies. It shows that power consumption increases as the power supply increases. Even with the same switching frequency and load capacitance, the eight-phase CP has higher power consumption than the two-phase CP at a higher supply voltage due to a large number of circuit components.

Table 2 presents the simulation results of the proposed two-phase and eight-phase charge pump (CP) circuits under different input voltages. The data indicate that the eight-phase architecture consistently outperforms the two-phase design in terms of start-up time, output voltage, ripple voltage, power consumption, and pumping efficiency. At an input voltage of 320 mV, the eight-phase CP achieves a higher output voltage of 1.55 V compared to 1.47 V for the two-phase CP, while reducing the ramp-up time from 138.8 µs to 52.6 µs and the output ripple from 15.5 mV to 7.24 mV. Similarly, at 420 mV input, the eight-phase CP provides a faster start-up of 7.1 µs versus 25.7 µs, a higher output voltage of 2.04 V, and improved pumping efficiency of 97.14% compared to 92.85% for the two-phase circuit. These results demonstrate that increasing the number of interleaved phases

significantly enhances transient performance, output stability, and overall efficiency of the CP circuit. To evaluate the performance of the proposed charge pump (CP) circuits, simulations were performed across different process corners and temperature values.

Figure 18 shows the variation of the output voltage for different process corners, including slow-slow (SS), typical-typical (TT), and fast-fast (FF). For both two-phase and eight-phase configurations, the FF corner exhibits the shortest ramp-up time ($T_{\text{ramp-up}}$), whereas the SS corner results in the longest $T_{\text{ramp-up}}$ at an input voltage of 420 mV. Figures 19, and 20 illustrate the output voltage of the proposed CP circuit at three different temperatures, 0°C, 27°C, and 50°C, with a supply voltage of 0.42 V. Table 3 summarizes the corner analysis results at an operating voltage of 420 mV for both architectures evaluated at three different temperatures. The results show that the output power consistently remains below 1.61 µW and 3.11 µW for the one-stage and four-stage CP circuits, respectively, under the TT corner at 75°C. Furthermore, the circuits achieve settling times of 4.03 µs and 8.28 µs for the one-stage and four-stage configurations, respectively, in the TT corner at the elevated temperature of 75°C.

To demonstrate the suitability of the proposed converter for practical energy-harvesting applications, additional simulations were performed under realistic source and load conditions. Figure 21 illustrates the minimum startup voltage as a function of source resistance. In practical energy-harvesting systems, such as thermoelectric generators and photovoltaic cells, the energy source exhibits a non-negligible internal resistance that limits the available startup current. As the source resistance increases from 0 Ω to 200 Ω, the minimum startup voltage increases from approximately 320 mV to 378 mV. This behavior is attributed to the increased voltage drop across the source resistance during startup, which reduces the effective voltage available to the charge pump. Nevertheless, the proposed converter is able to achieve self-startup at input voltages as low as 320 mV under ideal source conditions, demonstrating its suitability for ultra-low-voltage energy-harvesting environments. To further evaluate the converter under realistic IoT operating conditions, Figure 22 presents the transient response under a dynamic load profile. Initially, the converter operates under a no-load condition and generates an output voltage of approximately 1.6 V from a 320 mV input supply. At the load transition instant, the load current increases abruptly from 0 nA to 90 nA, emulating sensor node or wireless communication activation.

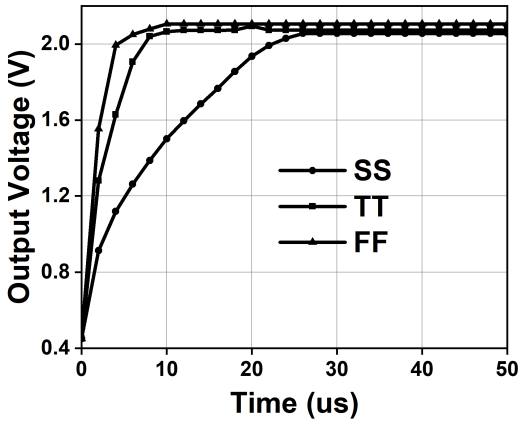


Fig. 18. Output voltage with Eight-Phase for different process corners.

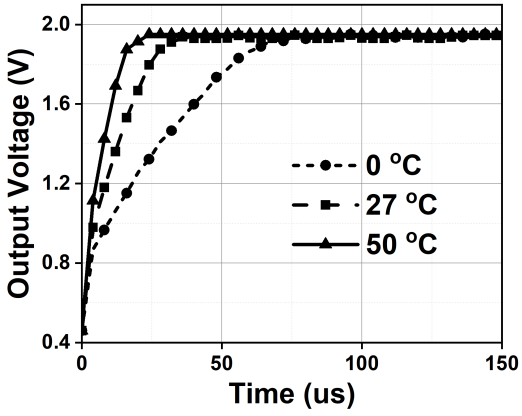


Fig. 19. Output voltage with Two-Phase for different temperature.

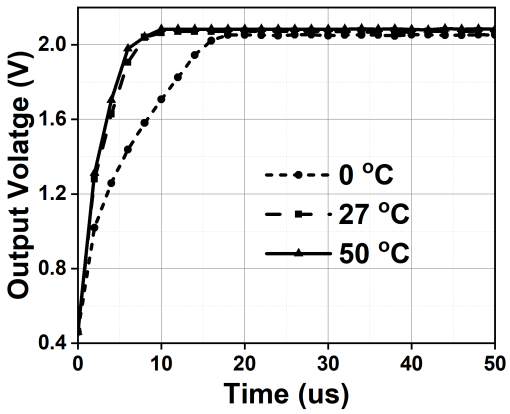


Fig. 20. Output voltage with Eight-Phase for different temperature.

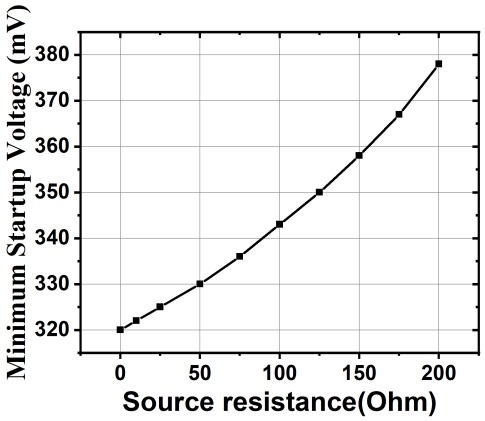


Fig. 21. The minimum startup voltage as a function of source resistance.

Parameter	Corner	2-Phase			8-Phase		
		Temperature (°C)			Temperature (°C)		
		0	27	75	0	27	75
Time (μ s)	SS	166.6	68.12	23.57	36.7	18.6	10.34
	TT	50.04	22.01	8.28	7.02	7.94	4.03
	FF	14.6	8.25	4.09	4.91	3.17	1.98
	SF	35.54	17.25	9.25	13.45	7.64	4.48
	FS	94.72	39.12	12.27	26.84	12.86	5.9
Power (nW)	SS	63.1	137.3	697.7	76.18	190.1	788.3
	TT	251.8	481.2	1614	283.7	618.4	3112
	FF	922.2	1572	3894	1112	2019	7230
	SF	423.6	853.5	2423	678.2	1534.6	5534
	FS	172.3	355.5	1122	182.4	458.8	1875.3
Output Voltage (V)	SS	2.05	1.94	1.87	2.08	2.04	2.04
	TT	1.94	1.93	1.86	2.06	2.04	2.01
	FF	1.93	1.93	1.83	2.06	2.01	1.95
	SF	1.95	1.92	1.82	1.99	2.00	1.94
	FS	1.94	1.93	1.85	2.04	2.03	1.97

Fig. 3. Performance comparison across process corners and temperatures (V_{in} = 420 mV).

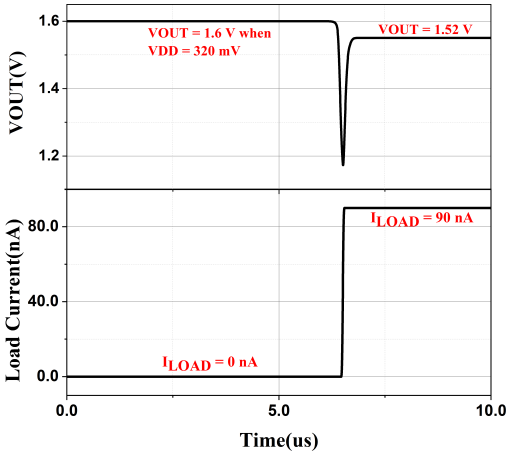


Fig. 22. The transient response under a dynamic load profile.

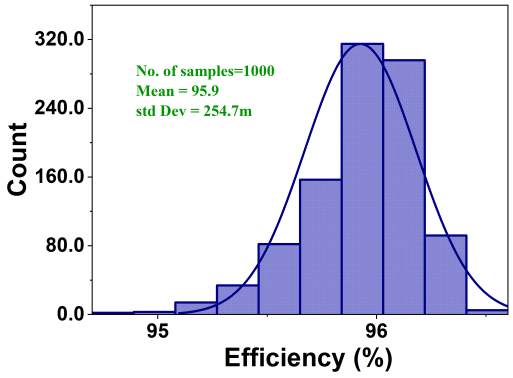


Fig. 23. Statistical distributions of efficiency.

As a result, the output voltage momentarily drops to approximately 1.15 V before recovering and settling to a steady-state value of approximately 1.52 V.

The transient response demonstrates the converter's ability to sustain load-current variations while maintaining a regulated output voltage with minimal steady-state degradation. These results confirm that the proposed converter can operate reliably under practical energy-harvesting conditions characterized by finite source impedance and time-varying load demands. Such conditions are commonly encountered in autonomous IoT sensor nodes, where harvested energy sources exhibit limited drive capability and load currents vary according to sensing, processing, and wireless-transmission activities.

To evaluate the robustness of the proposed converter against process and mismatch variations, a 1000-point Monte Carlo analysis was performed. Figures 23 show the statistical distributions of efficiency. The efficiency exhibits a mean value of 95.9% with a standard deviation of only 0.255%. The narrow distributions observed in Fig. 23 indicate low sensitivity to process variations and device mismatches. The results demonstrate that the proposed converter maintains high efficiency across manufacturing tolerances, confirming its robustness for practical ultra-low-voltage energy-harvesting applications.

The results indicate that the CP circuit reaches its steady-state output more rapidly at higher temperatures. Consequently, the ramp-up time decreases with increasing temperature, highlighting the temperature-dependent performance of the CP circuit.

Post-layout simulations confirm the robustness of the proposed architecture. Figure 24 illustrates the layout implementation of the proposed boost converter. The single-stage charge pump (CP) occupies an area of 166×110 μm^2, whereas the four-stage CP occupies 298.5×234.7 μm^2. Finally, Table 4 compares the proposed charge pump with prior state-of-the-art designs. For fair evaluation, the figure of merit (FOM) is defined as

$$\text{FOM} = \frac{P[\mu m] \times \left(\frac{\text{VCE}(\%)}{V_{\text{IN}}}\right) \times CR}{N \times V_{\text{min}}} \tag{46}$$

Ref	2018 [23]	2024 [24]	2021 [22]	This Work	
Tech. (nm)	180	65	180	180	180
Topology	Latched CP	Latched CP	Latched CP	Latched CP	Latched CP
# stages	4	4	4	4	4
V_{IN} (mV)	400	400	400	320	420
T_S (µs)	30	33.5	33	52.5	7.1
Frequency (MHz)	4	4	4	7.8	7.8
VCE (%)	95.7	87.8	99	96.8	97.14
Conversion Ratio	4.7	4.95	4.95	4.96	4.95
Load Cap. (pF)	1	160	1	1	1
Area (mm^2)	0.018	0.021	0.017	0.07	0.07
Output Power (nW)	N/A	793.6	240	27	75
Power Density (nW/mm^2)	N/A	37790	14118	386	1071
Area Efficiency (nW/mm^2)	N/A	37790	14118	386	1071
FOM	1.24	0.49	1.36	2.11	1.23

Fig. 4. Performance comparison with previously reported charge-pump architectures.

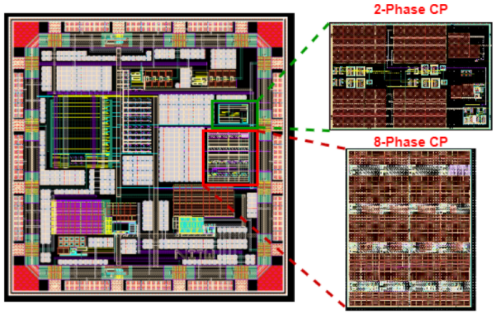


Fig. 24. Layout of the proposed converter.

where $P[\mu m]$, VCE, CR, N, and $V_{\min}$ represent the technology node, voltage conversion efficiency, conversion ratio, number of stages, and minimum start-up voltage, respectively. Although the proposed converter achieves a slightly lower FOM of 1.23 at 420 mV compared to [18] (1.36) and [19] (1.24), it attains a significantly shorter settling time of 7.1 µs. Furthermore, the eight-phase interleaved architecture effectively reduces output-voltage ripple while maintaining a high peak voltage conversion efficiency of 97.14%. The proposed design achieves the lowest startup voltage among all compared works, operating from an input voltage as low as 320 mV, whereas the other designs require a minimum input voltage of 400 mV. This characteristic makes the proposed converter particularly suitable for ultra-low-voltage energy-harvesting applications.

The proposed converter achieves a voltage conversion efficiency (VCE) of 96.8% at 320 mV and 97.14% at 420 mV, which is comparable to the best reported values in the literature. Although the design in [18] reports a slightly higher VCE of 99%, it requires a higher minimum input voltage of 400 mV. The proposed architecture also achieves a conversion ratio of 4.96, comparable to previously reported charge pumps.

To provide a standardized comparison, output power density and area efficiency are included. The proposed converter delivers output powers of 27 nW and 75 nW at input voltages of 320 mV and 420 mV, corresponding to power densities of 386 nW/mm^2 and 1071 nW/mm^2, respectively. Although these values are lower than those reported in some prior works, the proposed design operates from a significantly lower startup voltage and is optimized for ultra-low-power energy-harvesting applications.

Overall, the results demonstrate that the proposed converter achieves competitive efficiency while extending operation to lower input voltages. Its key advantage is reliable self-startup from a 320 mV input supply while maintaining a VCE exceeding 96%, making it well suited for self-powered IoT and energy-harvesting systems.

5. Conclusion

This paper presented a fully integrated low-voltage self-startup switched-capacitor boost converter for ultra-low-power energy-harvesting and battery-less IoT applications. The architecture combines an eight-phase interleaved charge-pump topology with a pre-charge node technique, dynamic body biasing, and a bootstrap-assisted multi-phase clock generator to improve startup capability and charge-transfer efficiency under ultra-low-voltage conditions. Post-layout simulations in a 180-nm CMOS process demonstrate reliable self-startup from an input voltage of 320 mV without the need for an auxiliary power source. Compared with a conventional two-phase implementation, the eight-phase architecture achieves faster startup, lower output-voltage ripple, and higher pumping efficiency over a wide input-voltage range. At input voltages of 320 mV and 420 mV, the converter generates output voltages of 1.55 V and 2.04 V, respectively, while attaining peak pumping efficiencies of 96.87% and 97.14%. In addition, the startup time is reduced by up to 72%. These results demonstrate the effectiveness of the proposed techniques for self-powered energy-harvesting systems operating from ultra-low input voltages.

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